DATA SHEET

PCK2010

CK98 (100/133MHz) Spread Spectrum System Clock Generator

Preliminary specification

1999 Mar 01

Philips Semiconductors

PHILIPS

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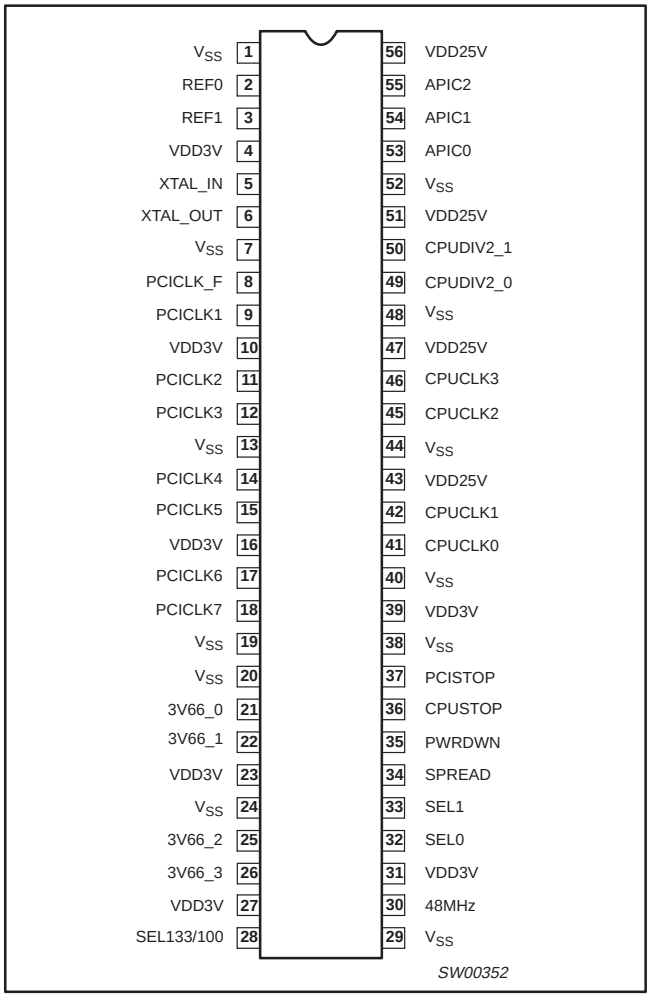
PCK2010

FEATURES

- Mixed 2.5V and 3.3V operation
- Four CPU clocks at 2.5V
- Eight PCI clocks at 3.3V, one free-running (synchronous with CPU clocks)
- Four 3.3V fixed clocks @ 66MHz
- Two 2.5V CPUDIV2 clocks @ ½ CPU clock frequency
- Three 2.5V IOAPIC clocks @ 16.67 MHz
- One 3.3V 48MHz USB clock
- Two 3.3V reference clocks @ 14.318 MHz
- Reference 14.31818 MHz Xtal oscillator input
- 133 MHz or 100 MHz operation
- Power management control input pins
- LOW CPU clock jitter ≤ 250 ps cycle-cycle
- LOW skew outputs
- 0.0ns – 1.5ns CPU - 3V66 delay
- 1.5ns – 4.0ns 3V66 - PCI delay
- 1.5ns – 4.0 ns CPU - IOAPIC delay
- Available in 56-pin SSOP package
- ±0.5% center spread spectrum capability via select pins; –0.5% down spread spectrum capability via select pins

PIN CONFIGURATION



DESCRIPTION

The PCK2010 is a clock synthesizer/driver chip for a PentiumII and other similar processors.

The PCK2010 has four CPU clock outputs at 2.5V, two CPUDIV2 clock outputs running at ½ CPU clock frequency (66MHz or 50MHz depending on the state of SEL133/100) and four 3V66 clocks running at 66MHz. There are eight PCI clock outputs running at 33MHz. One of the PCI clock outputs is free-running. Additionally, the part has three 2.5V IOAPIC clock outputs at 16.67MHz and two 3.3V reference clock outputs at 14.318MHz. All clock outputs meet Intel's drive strength, rise/fall time, jitter, accuracy, and skew requirements.

The part possesses dedicated power-down, CPUSTOP, and PCISTOP input pins for power management control. These inputs are synchronized on-chip and ensure glitch-free output transitions. When the CPUSTOP input is asserted, the CPU clock outputs and 3V66 clock outputs are driven LOW. When the PCISTOP input is asserted, the PCI clock outputs are driven LOW.

Finally, when the PWRDWN input pin is asserted, the internal reference oscillator and PLLs are shut down, and all outputs are driven LOW.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
56-Pin Plastic SSOP	0°C to +70°C	PCK2010 DL	PCK2010 DL	SOT371-1

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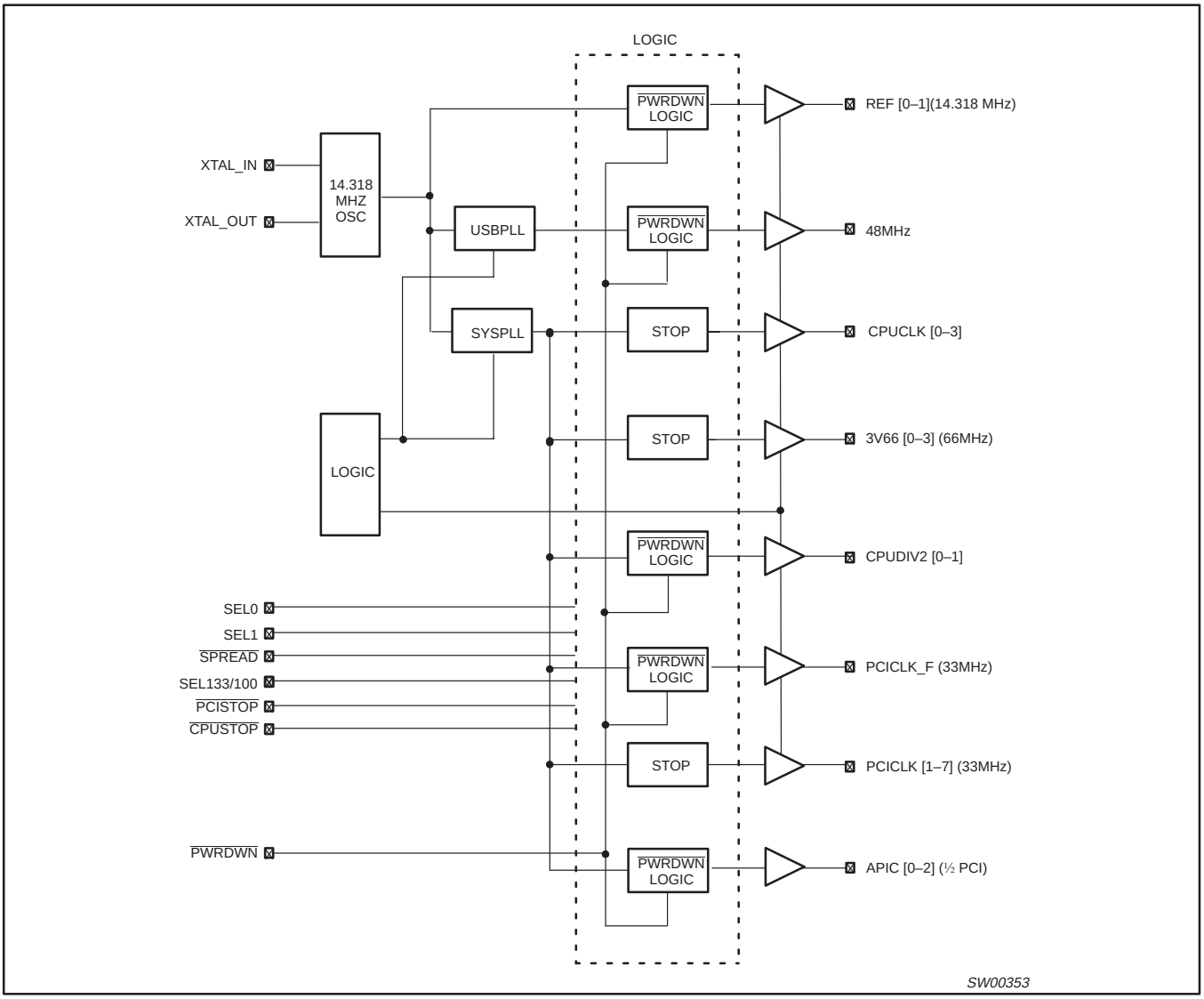
PIN DESCRIPTION

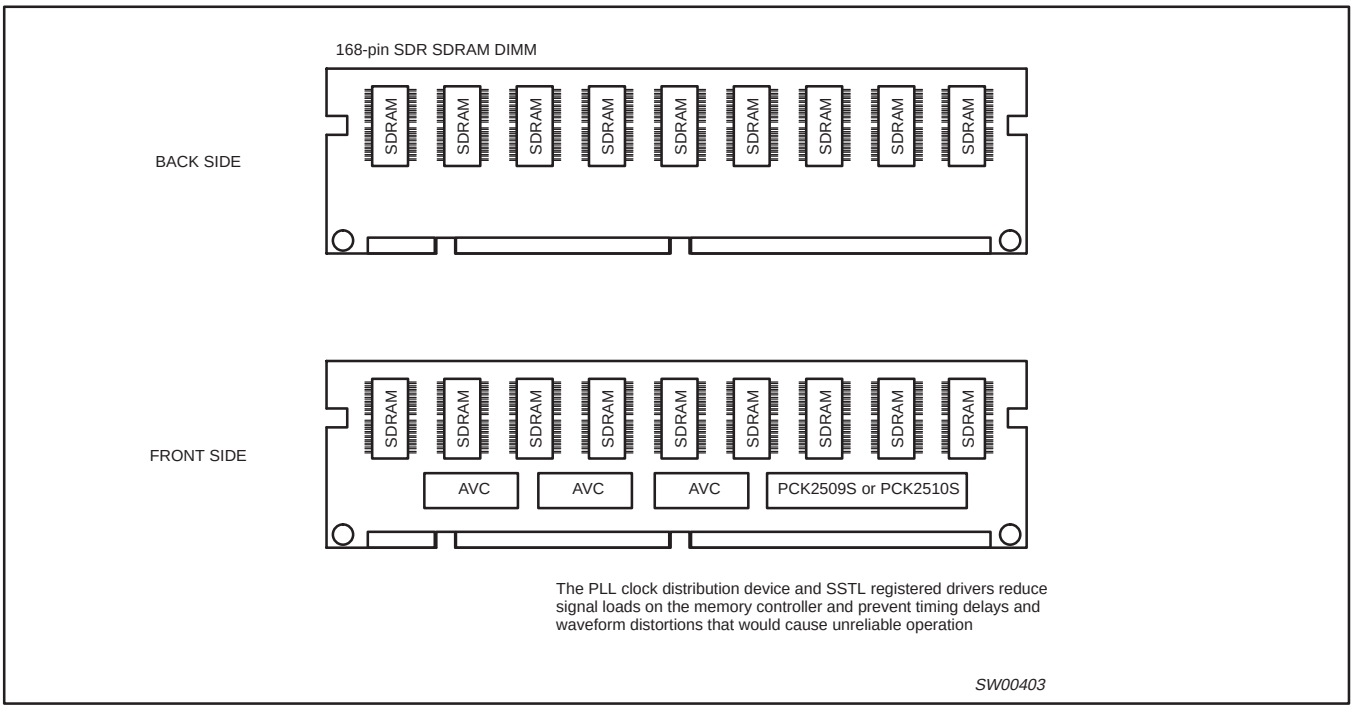
PIN NUMBER	SYMBOL	FUNCTION
2,3	REF [0–1]	3.3V 14.318 MHz clock output
5	XTAL_IN	14.318 MHz crystal input
6	XTAL_OUT	14.318 MHz crystal output
8	PCICLK_F	3.3V free running PCI clock
9, 11, 12, 14, 15, 17, 18	PCICLK [1–7]	3.3V PCI clock outputs
21, 22, 25, 26	3V66 [0–3]	3.3V fixed 66MHz clock outputs
28	SEL133/100	Select input pin for enabling 133MHz or 100MHz CPU outputs. H = 133MHz, L = 100MHz
30	48MHz	3.3V fixed 48MHZ clock output
32, 33	SEL [0–1]	Logic select pins. TTL levels.
34	SPREAD	3.3V LVTTL input. Enables spread spectrum mode when held LOW.
35	PWRDWN	3.3V LVTTL input. Device enters powerdown mode when held LOW.
36	CPUSTOP	3.3V LVTTL input. Stops all CPU clocks and 3V66 clocks when held LOW. CPUDIV_2 output remains on all the time.
37	PCISTOP	3.3V LVTTL input. Stops all PCI clocks except PCICLK_F when held LOW.
41, 42, 45, 46	CPUCLK [0–3]	2.5V CPU output. 133MHz or 100MHz depending on state of input pin SEL133/100.
49, 50	CPUDIV_2 [0–1]	2.5V output running at 1/2 CPU clock frequency. 66MHz or 50MHz depending on state of input pin SEL133/100.
53, 54, 55	IOAPIC [0–2]	2.5V clock outputs running divide synchronous with the CPU clock frequency. Fixed 16.67 MHz limit.
4, 10, 16, 23, 27, 31, 39	V_{DD3V}	3.3V power supply.
1, 7, 13, 19, 20, 24, 29, 38, 40, 44, 48, 52	V_{SS}	Ground
43, 47, 51, 56	V_{DD25V}	2.5V power supply

NOTES:

1. V_{DD3V}, V_{DD25V} and V_{SS} in the above tables reflects a likely internal POWER and GROUND partition to reduce the effects of internal noise on the performance of the device. In reality, the platform will be configured with the V_{DD25V} pins tied to a 2.5V supply, all remaining V_{DD} pins tied to a common 3.3V supply and all V_{SS} pins being common.

BLOCK DIAGRAM





FUNCTION TABLE

SEL 133/100	SEL1	SEL0	CPU	CPUDIV2	3V66	PCI	48MHz	REF	IOAPIC	NOTES
0	0	0	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	1
0	0	1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	2
0	1	0	100MHz	50MHz	66MHz	33MHz	HI-Z	14.318MHz	16.67MHz	3
0	1	1	100MHz	50MHz	66MHz	33MHz	48MHz	14.318MHz	16.67MHz	4, 7, 8
1	0	0	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	TCLK/16	5, 6
1	0	1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	2
1	1	0	133MHz	66MHz	66MHz	33MHz	HI-Z	14.318MHz	16.67MHz	3
1	1	1	133MHz	66MHz	66MHz	33MHz	48MHz	14.318MHz	16.67MHz	4, 7, 8

NOTES:
1. Required for board level “bed-of-nails” testing.
2. Used to support Intel confidential application.
3. 48MHz PLL disabled to reduce component jitter. 48MHz outputs to be held Hi-Z instead of driven to LOW state.
4. “Normal” mode of operation.
5. TCLK is a test clock over driven on the XTALIN input during test mode. TCLK mode is based on 133MHz CPU select logic.
6. Required for DC output impedance verification.
7. Frequency accuracy of 48MHz must be +167 PPM to match USB default.
8. Range of reference frequency allowed is MIN = 14.316MHz, NOMINAL = 14.31818MHz, MAX = 14.32MHz

CLOCK OUTPUT	TARGET FREQUENCY (MHz)	ACTUAL FREQUENCY (MHz)	PPM
USBCLK[7]	48.0	48.008	167

CLOCK ENABLE CONFIGURATION

CPUSTOP	PWRDWN	PCISTOP	CPUCLK	CPUDIV2	APIC	3V66	PCI	PCIF	REF 48MHz	OSC	VCOs
X	0	X	LOW	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
0	1	0	LOW	ON	ON	LOW	LOW	ON	ON	ON	ON
0	1	1	LOW	ON	ON	LOW	ON	ON	ON	ON	ON
1	1	0	ON	ON	ON	ON	LOW	ON	ON	ON	ON
1	1	1	ON	ON	ON	ON	ON	ON	ON	ON	ON

NOTES:
1. LOW means outputs held static LOW as per latency requirement below
2. ON means active.
3. PWRDWN pulled LOW, impacts all outputs including REF and 48MHz outputs.
4. All 3V66 clocks as well as CPU clocks should stop cleanly when CPUSTOP is pulled LOW.
5. CPUDIV2, IOAPIC, REF, 48MHz signals are not controlled by the CPUSTOP functionality and are enabled all in all conditions except when PWRDWN is LOW.

POWER MANAGEMENT REQUIREMENTS

SIGNAL	SIGNAL STATE	LATENCY
		NO. OF RISING EDGES OF FREE RUNNING PCICLK
CPUSTOP	0 (DISABLED)	1
	1 (ENABLED)	1
PCISTOP	0 (DISABLED)	1
	1 (ENABLED)	1
PWRDWN	1 (NORMAL OPERATION)	3ms
	0 (POWER DOWN)	2 MAX

NOTES:
1. Clock ON/OFF latency is defined as the number of rising edges of free running PCICLKs between the clock disable goes HIGH/LOW to the first valid clock that comes out of the device.
2. Power up latency is when PWRDWN goes inactive (HIGH) to when the first valid clocks are driven from the device.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to V_{SS} (V_{SS} = 0V)

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{DD3}	DC 3.3V core supply voltage		–0.5	+4.6	V
V_{DDQ3}	DC 3.3V I/O supply voltage		–0.5	+4.6	V
V_{DDQ2}	DC 2.5V I/O supply voltage		–0.5	+3.6	V
I_{IK}	DC input diode current	V_I < 0		–50	mA
V_I	DC input voltage	Note 2	–0.5	5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or V_O < 0		±50	mA
V_O	DC output voltage	Note 2	–0.5	V_{CC} + 0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}		±50	mA
T_{STG}	Storage temperature range		–65	+150	°C
P_{TOT}	Power dissipation per package plastic medium-shrink (SSOP)	For temperature range: –40 to +125°C above +55°C derate linearly with 11.3mW/K		850	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{DD3V}	DC 3.3V core supply voltage		3.135	3.465	V
V_{DD25V}	DC 2.5V I/O supply voltage		2.375	2.625	V
C_L	Capacitive load on: CPUCLK PCICLK CPUDIV2 3V66 48MHz clock REF IOAPIC	 1 device load, possible 2 loads Must meet PCI 2.1 requirements 1 device load, possible 2 loads 1 device load, possible 2 loads 1 device load 1 device load 1 device load	 10 10 10 10 10 10 10	 20 30 20 30 20 20 20	pF
V_I	DC input voltage range		0	V_{DD3V}	V
V_O	DC output voltage range		0	V_{DD25V} V_{DD3V}	V
f_{REF}	Reference frequency, oscillator nominal value		14.31818	14.31818	MHz
T_{amb}	Operating ambient temperature range in free air		0	+70	°C

POWER MANAGEMENT

CK133 CONDITION	MAXIMUM 2.5V SUPPLY CONSUMPTION MAXIMUM DISCRETE CAP LOADS, V_{DD25V} = 2.625V ALL STATIC INPUTS = V_{DD3V} OR V_{SS}	MAXIMUM 3.3V SUPPLY CONSUMPTION MAXIMUM DISCRETE CAP LOADS, V_{DD25V}= 3.465V ALL STATIC INPUTS = V_{DD3V} OR V_{SS}
Power-down mode ($\overline{PWRDWN}$ = 0)	100µA	200µA
Full active 100MHz SEL133/100# = 0 SEL1, 0 = 1 1 CPUSTOP, PCISTOP = 1	75mA	160mA
Full active 133MHz SEL133/100# = 1 SEL1, 0 = 1 1 CPUSTOP, PCISTOP = 1	90mA	160mA

DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS T_{amb} = 0°C to +70°C			UNIT
		V_{DD} (V)	OTHER		MIN	TYP	MAX	
V_{IH}	HIGH level input voltage	3.135 to 3.465		V_{DD25V} = 2.5V ±5%	2.0		V_{DD} + 0.3	V
V_{IL}	LOW level input voltage	3.135 to 3.465		V_{DD3V} = 3.3V ±5%	V_{SS} – 0.3		0.8	V
V_{OH2}	2.5V output HIGH voltage CPUCLK, IOAPIC, CPUDIV2	2.375 to 2.625	I_{OH} = –1mA		2.0		–	V
V_{OL2}	2.5V output LOW voltage CPUCLK, IOAPIC, CPUDIV2	2.375 to 2.625	I_{OL} = 1mA		–		0.4	V
V_{OH3}	3.3V output HIGH voltage REF, 48MHz	3.135 to 3.465	I_{OH} = –1mA		2.0		–	V
V_{OL3}	3.3V output LOW voltage REF, 48MHz	3.135 to 3.465	I_{OL} = 1mA		–		0.4	V
V_{OH3}	3.3V output HIGH voltage PCI, 3V66	3.135 to 3.465	I_{OH} = –1mA		2.4		–	V
V_{OL3}	3.3V output LOW voltage PCI, 3V66	3.135 to 3.465	I_{OL}= 1mA		–		0.55	V
I_{OH}	CPUCLK output HIGH current	2.375	V_{OUT} = 1.0V		–27		–	mA
		2.625	V_{OUT} = 2.375V		–		–27	
I_{OH}	48MHz, REF output HIGH current	3.135	V_{OUT} = 1.0V		–29		–	mA
		3.465	V_{OUT} = 3.135V		–		–23	
I_{OH}	PCI, 3V66 output HIGH current	3.135	V_{OUT} = 1.0V		–33		–	mA
		3.465	V_{OUT} = 3.135V		–		–33	
I_{OL}	CPUCLK output LOW current	2.375	V_{OUT} = 1.2V		27		–	mA
		2.625	V_{OUT} = 0.3V		–		30	
I_{OL}	48MHz, REF output LOW current	3.135	V_{OUT} = 1.95V		29		–	mA
		3.465	V_{OUT} = 0.4V		–		27	
I_{OL}	PCI, 3V66 output LOW current	3.135	V_{OUT} = 1.95V		30		–	mA
		3.465	V_{OUT} = 0.4V		–		38	
$\pm I_I$	Input leakage current	3.465			–		5	µA
$\pm I_{OZ}$	3-State output OFF-State current	3.465	V_{OUT} = V_{dd} or GND	I_O = 0	–		10	µA
Cin	Input pin capacitance						5	pF
Cxtal	Xtal pin capacitance, as seen by external crystal					18		pF
Cout	Output pin capacitance						6	pF
I_{dd3}	Operating supply current	3.465	100MHz mode	Outputs loaded[1]			160	mA
			133MHz mode	Outputs loaded[1]			160	mA
	Powerdown supply current		All static inputs to V_{DD} or GND				200	µA
I_{dd2}	Operating supply current	2.625	100MHz mode	Output loaded[1]			160	mA
			133MHz mode	Output loaded[1]			160	mA
	Powerdown supply current		All static inputs to V_{DD} or GND				100	µA

NOTE:
1. All clock outputs loaded with maximum lump capacitance test load specified in AC characteristics section.

AC CHARACTERISTICS

V_{DD3V} = 3.3V ± 5%; VDDAPIC = V_{DD25V} = 2.5V ± 5%; $f_{crystal}$ = 14.31818 MHz

CPU CLOCK OUTPUTS, CPU(0–3) (LUMP CAPACITANCE TEST LOAD = 20pF)

SYMBOL	PARAMETER	LIMITS T_{amb} = 0°C to +70°C		LIMITS T_{amb} = 0°C to +70°C		UNIT	NOTES
		133MHz MODE		100MHz MODE			
		MIN	MAX	MIN	MAX		
T_{HKP}	CPUCLK period	7.5	8.0	10.0	10.5	ns	2, 9
T_{HKH}	CPUCLK HIGH time	1.87	n/a	3.0	n/a	ns	5, 10
T_{HKL}	CPUCLK LOW time	1.67	n/a	2.8	n/a	ns	6, 10
T_{HRISE}	CPUCLK rise time	0.4	1.6	0.4	1.6	ns	8
T_{HFALL}	CPUCLK fall time	0.4	1.6	0.4	1.6	ns	8
T_{JITTER}	CPUCLK cycle-cycle jitter		250		250	ps	
DUTY CYCLE	Output Duty Cycle	45	55	45	55	%	1
T_{HSKW}	CPUCLK pin-pin skew		175		175	ps	2

CPUDIV2 CLOCK OUTPUTS, CPUDIV2 (0–1) (LUMP CAPACITANCE TEST LOAD = 20pF)

SYMBOL	PARAMETER	LIMITS T_{amb} = 0°C to +70°C		LIMITS T_{amb} = 0°C to +70°C		UNIT	NOTES
		133MHz MODE		100MHz MODE			
		MIN	MAX	MIN	MAX		
T_{HKP}	CPUDIV2 CLK period	15.0	16.0	20.0	21.0	ns	2, 9
T_{HKH}	CPUDIV2 CLK HIGH time	5.25	n/a	7.5	n/a	ns	5, 10
T_{HKL}	CPUDIV2 CLK LOW time	5.05	n/a	7.3	n/a	ns	6, 10
T_{HRISE}	CPUDIV2 CLK rise time	0.4	1.6	0.4	1.6	ns	8
T_{HFALL}	CPUDIV2 CLK fall time	0.4	1.6	0.4	1.6	ns	8
T_{JITTER}	CPUDIV2 CLK cycle-cycle jitter		250		250	ps	
DUTY CYCLE	CPUDIV2 CLK Duty Cycle	45	55	45	55	%	1
T_{HSKW}	CPUDIV2 CLK pin-pin skew		175		175	ps	2

PCI CLOCK OUTPUTS, PCI(0–7) (LUMP CAPACITANCE TEST LOAD = 30pF)

SYMBOL	PARAMETER	LIMITS T_{amb} = 0°C to +70°C		LIMITS T_{amb} = 0°C to +70°C		UNIT	NOTES
		133MHz MODE		100MHz MODE			
		MIN	MAX	MIN	MAX		
T_{HKP}	PCICLK period	30.0	n/a	30.0	n/a	ns	2, 9
T_{HKH}	PCICLK HIGH time	12.0	n/a	12.0	n/a	ns	5, 10
T_{HKL}	PCICLK LOW time	12.0	n/a	12.0	n/a	ns	6, 10
T_{HRISE}	PCICLK rise time	0.5	2.0	0.5	2.0	ns	8
T_{HFALL}	PCICLK fall time	0.5	2.0	0.5	2.0	ns	8
T_{JITTER}	PCICLK cycle-cycle jitter		500		500	ps	
DUTY CYCLE	PCICLK Duty Cycle	45	55	45	55	%	1
T_{HSKW}	PCICLK pin-pin skew		500		500	ps	2

APIC(0–1) CLOCK OUTPUT (LUMP CAPACITANCE TEST LOAD = 20pF)

SYMBOL	PARAMETER	LIMITS T_{amb} = 0°C to +70°C		LIMITS T_{amb} = 0°C to +70°C		UNIT	NOTES
		133MHz MODE		100MHz MODE			
		MIN	MAX	MIN	MAX		
T_{HKP}	IOAPIC CLK period	60.0	64.0	60.0	64.0	ns	2, 9
T_{HKH}	IOAPIC CLK HIGH time	25.5	n/a	25.5	n/a	ns	5, 10
T_{HKL}	IOAPIC CLK LOW time	25.3	n/a	25.3	n/a	ns	6, 10
T_{HRISE}	IOAPIC CLK rise time	0.4	1.6	0.4	1.6	ns	8
T_{HFALL}	IOAPIC CLK fall time	0.4	1.6	0.4	1.6	ns	8
T_{JITTER}	IOAPIC CLK cycle-cycle jitter		500		500	ps	
DUTY CYCLE	IOAPIC CLK Duty Cycle	45	55	45	55	%	1
T_{HSKW}	IOAPIC CLK pin-pin skew		250		250	ps	2

3V66 CLOCK OUTPUT, 3V66 (0–3) (LUMP CAPACITANCE TEST LOAD = 30 pF)

SYMBOL	PARAMETER	LIMITS T_{amb} = 0°C to +70°C		LIMITS T_{amb} = 0°C to +70°C		UNIT	NOTES
		133MHz MODE		100MHz MODE			
		MIN	MAX	MIN	MAX		
T_{HKP}	3V66 CLK period	15.0	16.0	15.0	16.0	ns	2, 9, 4
T_{HKH}	3V66 CLK HIGH time	5.25	n/a	5.25	n/a	ns	5, 10
T_{HKL}	3V66 CLK LOW time	5.05	n/a	5.05	n/a	ns	6, 10
T_{HRISE}	3V66 CLK rise time	0.4	1.6	0.4	1.6	ns	8
T_{HFALL}	3V66 CLK fall time	0.4	1.6	0.4	1.6	ns	8
T_{JITTER}	3V66 CLK cycle-cycle jitter		500		500	ps	
DUTY CYCLE	3V66 CLK Duty Cycle	45	55	45	55	%	1
T_{HSKW}	3V66 CLK pin-pin skew		250		250	ps	2

48MHZ(0–1) CLOCK OUTPUT (LUMP CAPACITANCE TEST LOAD = 20pF)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = 0°C to +70°C		UNIT
			NOTES	MIN	MAX	
f	Frequency, Actual	Determined by PLL divider ratio		48.008		MHz
f_D	Deviation from 48MHz	(48.008 – 48)/48		+167		ppm
T_{HRISE} (t_R)	Output rise edge rate			1	4	ns
T_{HFALL} (t_F)	Output fall edge rate			1	4	ns
DUTY CYCLE (t_D)	Duty Cycle			45	55	%
T_{JITTER}	CLK cycle-cycle jitter	133MHz		100MHz		ps
		MIN	MAX	MIN	MAX	
			500		500	
T_{HSTB} (f_{ST})	Frequency stabilization from Power-up (cold start)				3	ms

NOTES:
1. See Figure 3 for measure points.

AC CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS T_{amb} = 0°C to +70°C			UNIT	NOTES
		Measurement loads (lumped)	Measure points	MIN	TYP	MAX		
$T_{HPOFFSET}$	CPUCLK to 3V66 CLK, CPU leads	CPU@30pF, 3V66@30pF	CPU@1.25V, 3V66@1.5V	0.0		1.5	ns	1
$T_{HPOFFSET}$	3V66 CLK to PCICLK, 3V66 leads	3V66@30pF, PCI@30pF	3V66@1.5V, PCI@1.5V	1.5		3.5	ns	1
$T_{HPOFFSET}$	CPUCLK to IOAPIC, CPU leads	CPU@20pF, IOAPIC@20pF	3CPU@1.25V, IOAPIC@1.25V	1.5		4.0	ns	1
	PCICLK to CPUCLK, CPU leads	PCI@30pF CPU@30pF	PCI@1.5V CPU@1.25V		5.8		ns	
	CPUDIV2 to CPUCLK, CPUDIV2 leads	CPUDIV2@20pF CPU@30pF	CPUDIV2@ CPU@1.25V		1.6		ns	
	IOAPICCLK to CPUCLK, IOAPIC leads	IOAPIC@20pF CPU@30pF	IOAPIC@20pF CPU@1.25V		3.7		ns	
	3V66 CLK to CPUCLK, 3V66 leads	3V66@30pF CPU@30pF	3V66@1.5V CPU@1.25V		1.7		ns	

NOTES:
1. Output drivers must have monotonic rise/fall times through the specified V_{OL}/V_{OH} levels.
2. Period, jitter, offset and skew measured on rising edge @1.25V for 2.5V clocks and @ 1.5V for 3.3V clocks.
3. The PCICLK is the CPUCLK divided by four at CPUCLK = 133.MHz. The 3V66 CLK is internal VCO frequency divided by three at CPUCLK = 100MHz.
4. 3V66 CLK is internal VCO frequency divided by two at CPUCLK = 133MHz. The 3V66 CLK is internal VCO frequency divided by three at CPUCLK = 100MHz.
5. T_{HKH} is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs as shown in Figure 4.
6. T_{HKL} is measured at 0.4V for all outputs as shown in Figure 4.
7. The time is specified from when V_{DDQ} achieves its nominal operating level (typical condition V_{DDQ} = 3.3V) until the frequency output is stable and operating within specification.
8. T_{HRISE} and T_{HFALL} are measured as a transition through the threshold region V_{OL} = 0.4V and V_{OH} = 2.4V (1mA) JEDEC specification.
9. The average period over any 1 μs period of time must be greater than the minimum specified period.
10. Calculated at minimum edge-rate (1V/ns) to guarantee 45/55% duty-cycle. Pulse width is required to be wider at faster edge-rate to ensure duty-cycle specification is met.
11. Output (see Figure 3 for measure points).

PCK2010 SPREAD SPECTRUM FUNCTION TABLE

SPREAD#	SEL133/100#	SEL1	SEL0	Intel CK133	Intel CK133	Philips PCK2010	Philips PCK2010
pin 34	pin 28	pin 33	pin 32	Function	48MHz PLL	Function	48MHz PLL
0 (active)	0 (100MHz)	0	0	3-State to High Impedance	Inactive	3-State to High Impedance	Inactive
0 (active)	0 (100MHz)	0	1	(Reserved)	(Reserved)	100MHz, Center Spread ±0.5%	Active
0 (active)	0 (100MHz)	1	0	100MHz, Down Spread – 0.5%	Inactive	100MHz, Down Spread – 0.5%	Inactive
0 (active)	0 (100MHz)	1	1	100MHz, Down Spread – 0.5%	Active	100MHz, Down Spread – 0.5%	Active
0 (active)	1 (133MHz)	0	0	Test Mode	Active	Test Mode	Active
0 (active)	1 (133MHz)	0	1	(Reserved)	(Reserved)	133MHz, Center Spread ±0.5%	Active
0 (active)	1 (133MHz)	1	0	133Mhz, Down Spread – 0.5%	Inactive	133MHz, Down Spread – 0.5%	Inactive
0 (active)	1 (133MHz)	1	1	133Mhz, Down Spread – 0.5%	Active	133MHz, Down Spread – 0.5%	Active
1 (inactive)	0 (100MHz)	0	0	3-State to High Impedance	Inactive	3-State to High Impedance	Inactive

1 (inactive)	0 (100MHz)	0	1	(Reserved)	(Reserved)	100MHz, No Center Spread ±0.5%	Active
1 (inactive)	0 (100MHz)	1	0	100MHz, No Spread Spectrum	Inactive	100MHz, No Spread Spectrum	Inactive
1 (inactive)	0 (100MHz)	1	1	100MHz, No Spread Spectrum	Active	100MHz, No Down Spread – 0.5%	Active
1 (inactive)	1 (133MHz)	0	0	Test Mode	Active	Test Mode	Active
1 (inactive)	1 (133MHz)	0	1	(Reserved)	(Reserved)	133MHz, No Center Spread ±0.5%	Active
1 (inactive)	1 (133MHz)	1	0	133MHz, No Spread Spectrum	Inactive	133MHz, No Spread Spectrum	Inactive
1 (inactive)	1 (133MHz)	1	1	133MHz, No Spread Spectrum	Active	133MHz, No Down Spread – 0.5%	Active

AC WAVEFORMS

V_M = 1.25V @ V_{DDQ2} and 1.5V @ V_{DDQ3}
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} – 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

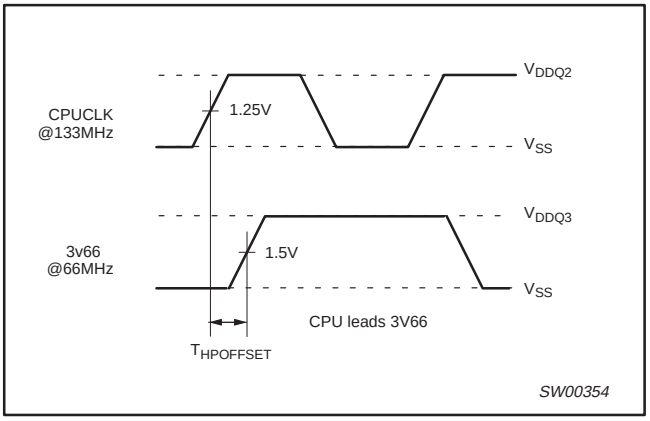


Figure 1. CPUCLK to 3V66 offset

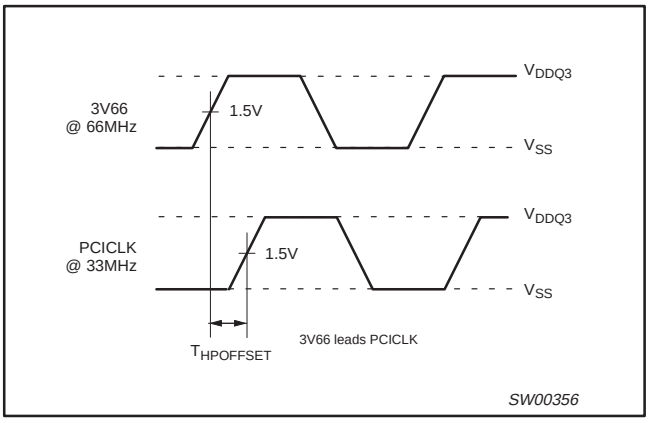


Figure 2. 3V66 to PCI offset

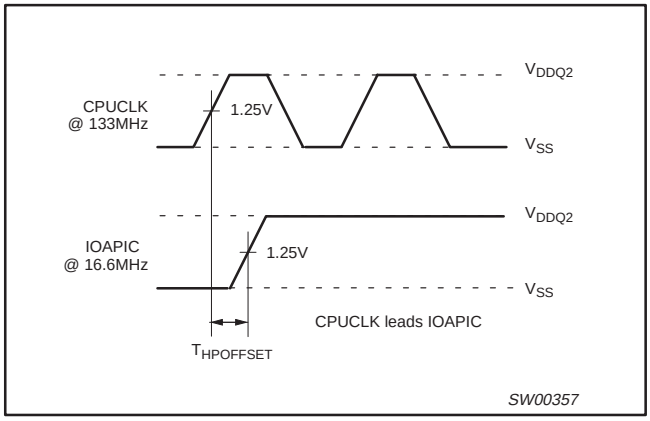


Figure 3. CPU to IOAPIC offset

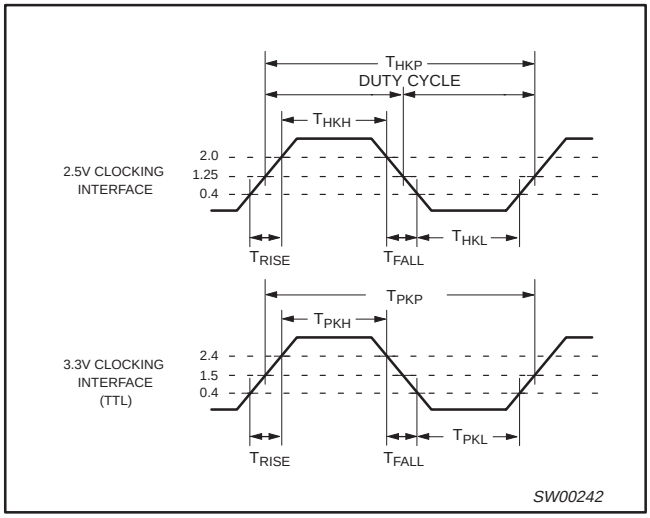


Figure 4. 2.5V/3.3V clock waveforms

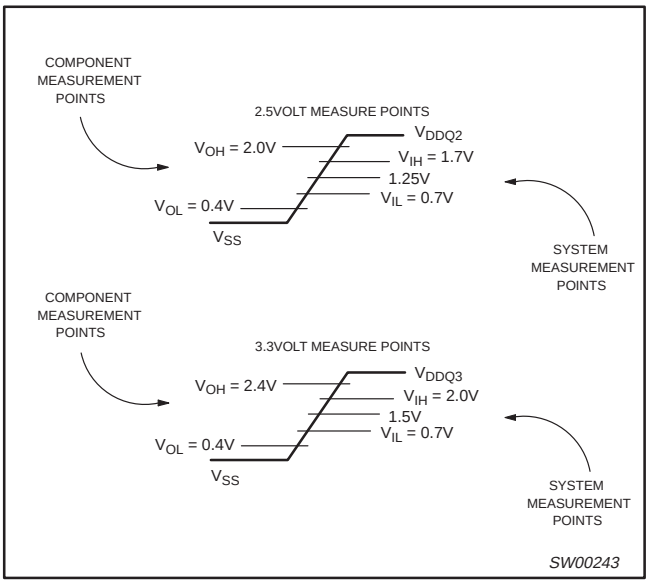


Figure 5. Component versus system measure points

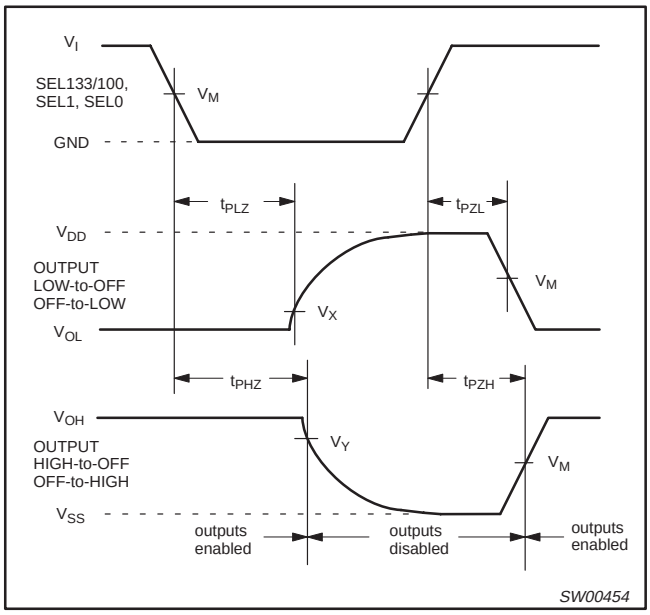
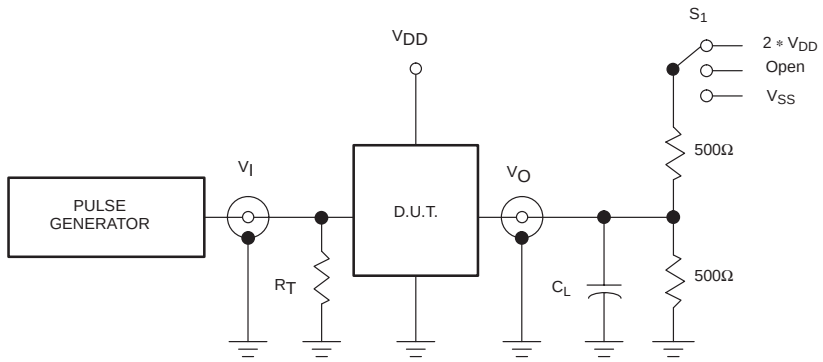


Figure 6. 3-State enable and disable times

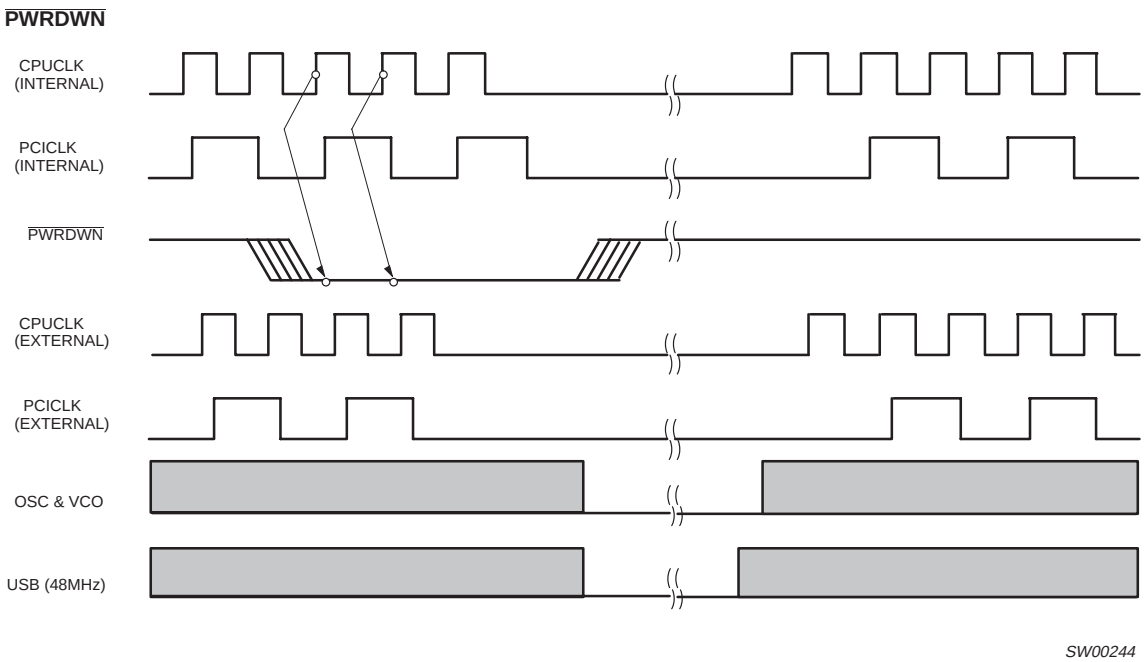


TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 * V_{DD}$
t_{PHZ}/t_{PZH}	V_{SS}

$V_{DD} = V_{DDQ2}$ or V_{DDQ3}, DEPENDS ON THE OUTPUT

SW00238

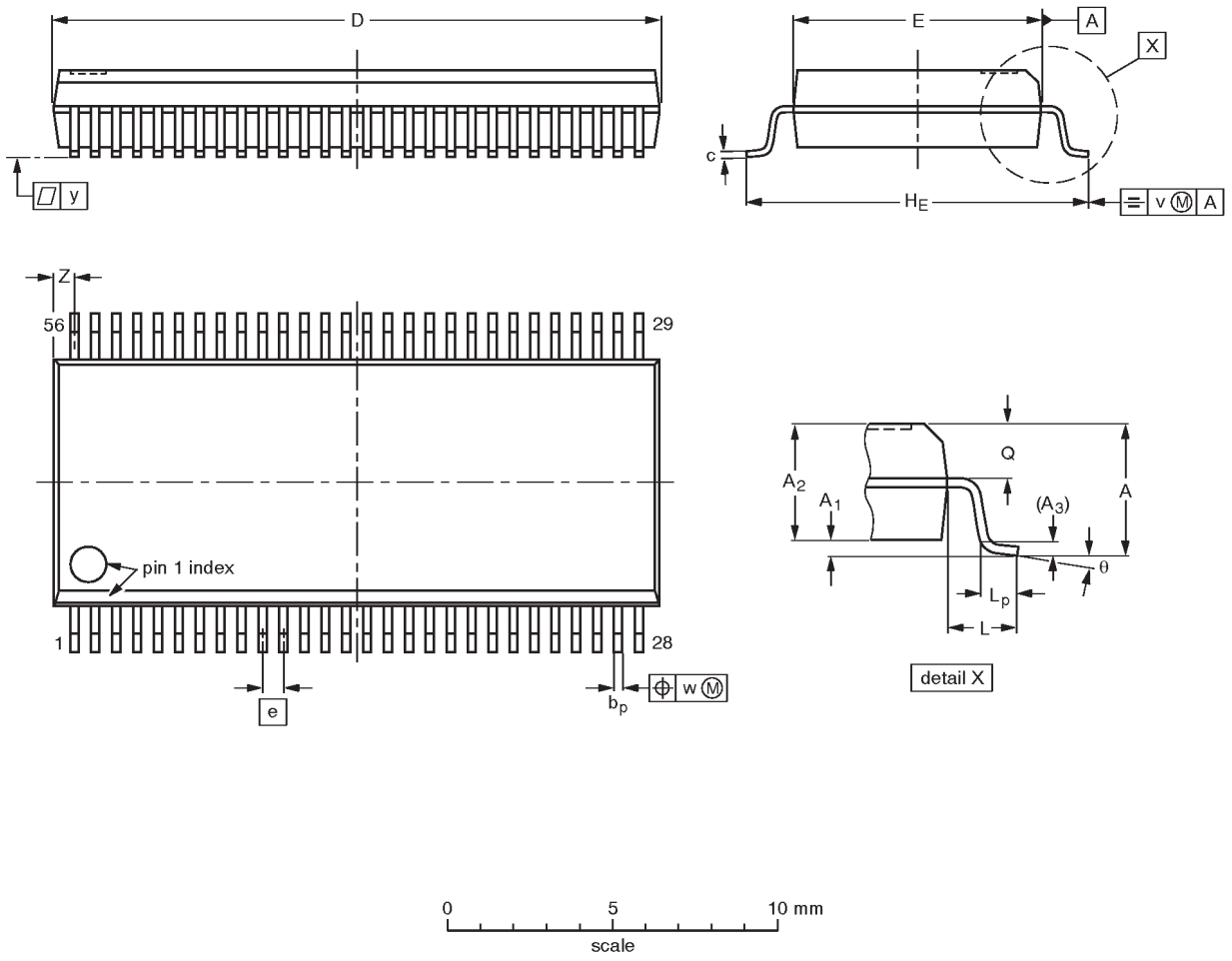
Figure 7. Load circuitry for switching times



SW00244

Figure 8. Power Management

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

CK98 (100/133MHz) Spread Spectrum System Clock Generator PCK2010

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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