
PAS005B SXGA Color/Mono Digital CMOS Image Sensor

General Description

The PAS005B is a highly integrated CMOS active-pixel image sensor that has a SXGA resolution of 1280(H) x 1024(V). To have an excellent image quality, the PAS005B outputs 10-bit RGB raw data through a parallel data bus. It is available in color or monochrome in 48-pin LCC.

The PAS005B can be programmed to set the exposure time for different luminance conditions via I²CTM serial control bus. By programming the internal register sets, it performs on-chip frame rate adjustment, offset correction DAC, programmable gain control, 10-bits ADC, 8-bits output companding, interpolated sub-sampling and defect compensation.

Features

- SXGA(1280x1024 pixels) resolution, 1/2" Lens
- Bayer-RGB color filter array
- On-chip 10-bit pipelined A/D converter
- User selectable digital output formats:
 - ❑ 10-bit parallel RGB raw data
 - ❑ Formatted data output
- On-chip 9-bit background compensation DAC
- On-chip programmable gain amplifier
 - ❑ 4-bit color gain amplifier (x3)
 - ❑ 5-bit global gain amplifier (x4)
- Continuous variable frame time(1/2sec~1/30sec)
- Continuous variable exposure time
- I²CTM Interface
- External synchronization support
- Single 3.3V supply voltage
- 150 mW low power dissipation(<100mW@VGA, 30fps)
- 200 uW low power down dissipation
- Support flash light timing
- Mirror readout (vertical & horizontal)
- Windowing
- Interpolated Sub-sampling: 1/2, 1/4, 1/8

Key Specification

| | |
|-----------------|-----------------------------|
| Supply voltage | 3.3V ± 10% |
| Array format | 1280(H) x 1024(V) |
| Optical format | 1/2 " |
| Pixel size | 5.4µmX5.4µm |
| Frame rate | ~10 fps @ full video |
| System clock | Up to 48 MHz |
| Max. pixel rate | 16 MHz |
| FPN | 7.05 level |
| Sensitivity | 553 level/Lux*sec |
| PGA gain | 26dB(Max.) |
| Color filter | RGB Bayer Pattern |
| Exposure time | ~ Frame time to 1 pixel CLK |
| Scan mode | Progressive |
| S/N Ratio | 45dB |
| Power | < 150 mW @ 10fps |
| Package | 48-pin LCC |

1. Pin Assignment

| Pin# | Name | Type | Description |
|------|---------|------|-----------------------------|
| 1 | CSB | I | Chip Select Bar |
| 2 | VDDD | P | Digital Power |
| 3 | VSSD | P | Digital Ground |
| 4 | VSS_ESD | P | ESD Ground |
| 5 | VDDA | P | Analog Power |
| 6 | X_VDDD | I/O | Internal digital power |
| 7 | VLRST | I/O | VLRST |
| 8 | I_PXON | I/O | Analog test output N |
| 9 | I_PXOP | I/O | Analog test output P |
| 10 | I_PXIN | I/O | Analog test input N |
| 11 | I_PXIP | I/O | Analog test input P |
| 12 | VSSX | P | Regulator Ground |
| 13 | VDDX | P | Regulator Power |
| 14 | X_VRB | O | Voltage Reference Bottom |
| 15 | X_VRT | O | Voltage Reference Top |
| 16 | X_VCM | O | Voltage Common Mode |
| 17 | VSSX | P | Regulator Ground |
| 18 | X_VCM | O | Voltage Common Mode |
| 19 | EXTRESN | I | External R_N_node |
| 20 | EXTRESP | I | External R_P_node |
| 21 | X_VREF | O | Voltage Reference testpoint |
| 22 | VSSA | P | Analog Ground |
| 23 | VDDA | P | Analog Power |
| 24 | NC | - | Not connected |
| 25 | X_VDDAY | I/O | Array Power |
| 26 | VSSAY | P | Array Ground |
| 27 | VSSD | P | Digital Ground |
| 28 | VDDD | P | Digital Power |
| 29 | SCL | I | I2C Serial Clock |
| 30 | SDA | I/O | I2C Serial Data |
| 31 | PX0 | O | Dataout bit 0 |
| 32 | PX1 | O | Dataout bit 1 |
| 33 | PX2 | O | Dataout bit 2 |
| 34 | PX3 | O | Dataout bit 3 |
| 35 | PX4 | O | Dataout bit 4 |
| 36 | VDDQ | P | I/O Driver Power |
| 37 | VSSQ | P | I/O Driver Ground |
| 38 | PX5 | O | Dataout bit 5 |
| 39 | PX6 | O | Dataout bit 6 |
| 40 | PX7 | O | Dataout bit 7 |
| 41 | PX8 | O | Dataout bit 8 |
| 42 | PX9 | O | Dataout bit 9 |
| 43 | SYSCLK | I | System Clock |
| 44 | HSYNC | O | Horizontal Sync |
| 45 | PXCLK | O | Pixel Clock |
| 46 | SYNC | I | External Sync |
| 47 | NC | - | Not connected |
| 48 | VSYNC | O | Vertical Sync |

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2. Block Diagram

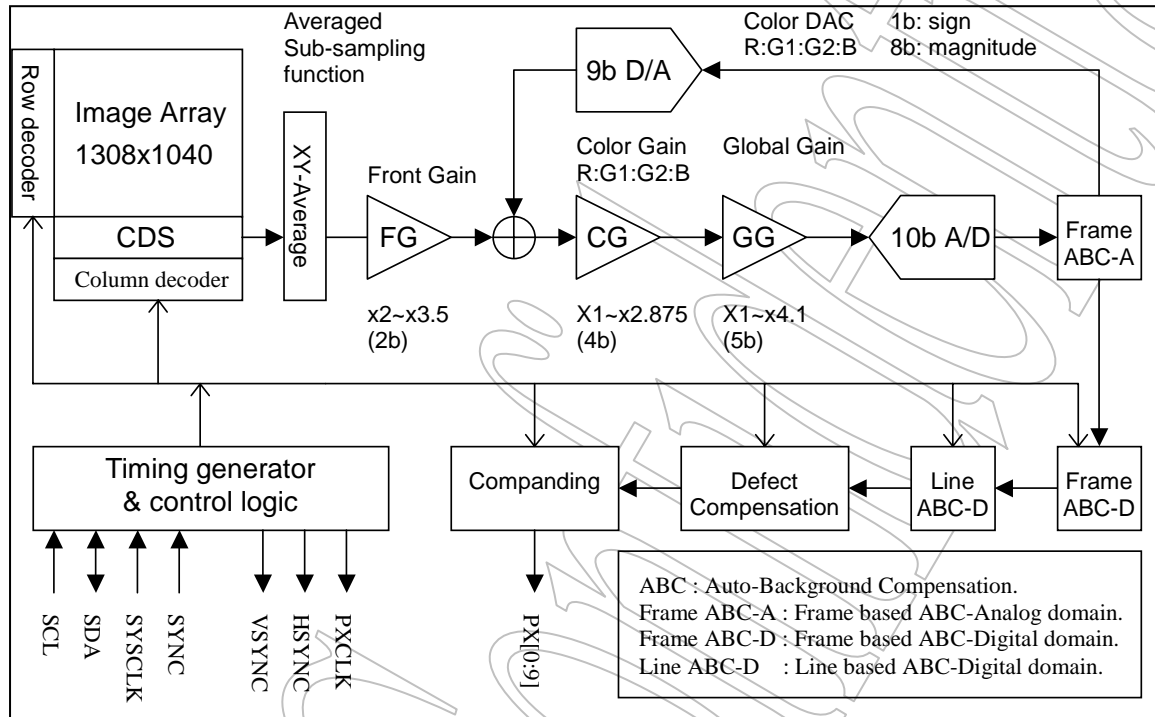


Figure 2.1. Shows the PAS005 sensor block diagram

The PAS005 is a 1/2 -inch CMOS imaging sensor with 1308x1040 physical pixels. The active region of sensor array is 1288x1028 as shown in Fig. 2.1. The sensor array is cover with Bayer pattern color filters and U-lens. The first pixel location <0,0> is programmable in 2 direction (X and Y) and the default value is at the left-down side of sensor array.

After a programmable exposure time, the image is sampled first with CDS (Correlated Double Sampling) block to improve S/N ration and reduce fixed pattern noise. The optional XY-averaged function is implemented to improve the sub-sampling image quality. It can reduce the sawtooth edge in VGA and CIF format output.

Three analog gain stages are implemented before signal transferred by the 10b ADC. The front gain stage (FG) can be programmed to fit the saturation level of sensor to the full-range input of ADC. The programmable color gain stage (CG) is used to balance the luminance response difference between B/G/R. The global gain stage (GG) is programmed to adapt the gain to the image luminance.

The fine gained signal will be digitized by the on-chip 10b ADC. After the image data has been digitized,

further alteration to the signal can be applied before the data is output:

2.2 Automatic Background Compensation (ABC)

The ABC function is implemented by 3 steps : ABC-A, Frame-based ABC-D, and Line-based ABC-D. The ABC-A is implemented in analog domain with an on-chip 9b DAC. The Frame-based ABC-D is implemented in digital domain to automatically compensate the leakage current with 2 dark reference lines on top of sensor array. The Line-based ABC-D is implemented in digital domain to automatically compensate the leakage with 4 dark reference columns surround the sensor array. These three blocks can be enable/disable separately by user.

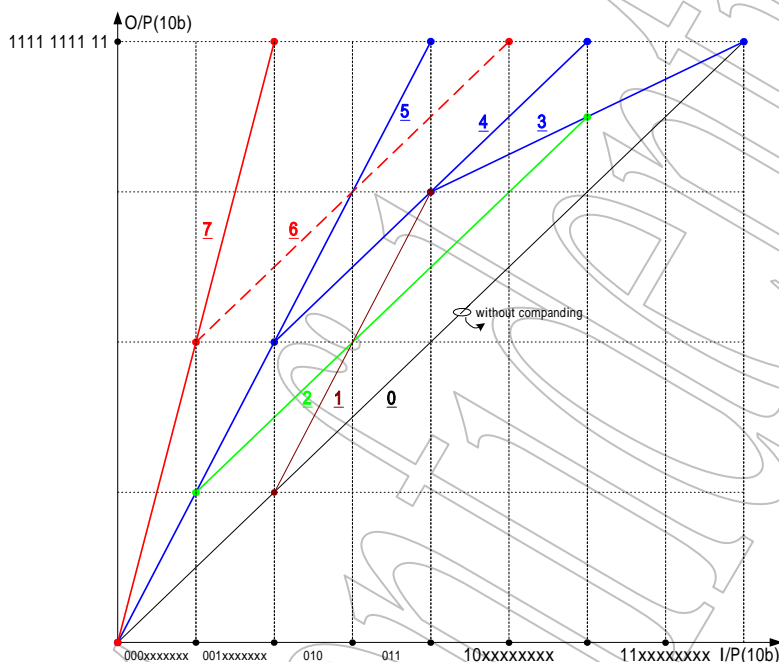
2.3 Defect Compensation

The Defect Compensation block can detect the possible defect pixel and replace it with average output of like-colored pixels on either side of defective pixel. There is no limitation in the capability of defect number. This function is also enable/disable by user.

2.4 Companding

The companding function is used to simulate the gamma curve and do non-linear transformation before the data is output. There are 8 curves selected by setting register `comp_crv[2:0]` as shown in Fig. 2.4. The default value [00] is a linear curve.

Figure 2.4 Companding curves program by comp_crv[2:0]



3. Register and Function

3.1. Register list

| Register | Register | R/W | Default (Decimal) | Description |
|------------|-------------|-----|-------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| Reg_2[3:0] | Np_i2c[3:0] | R/W | 1 | I2C sampling frequency = frequency of I_sysclk / Np_i2c Programming range of Np_i2c: 1~15 |
| Reg_3[5:0] | Np[5:0] | R/W | 2 | Pixel rate = frequency of I_sysclk / Np Programming range of Np: 1~63 |
| Reg_4[7] | single_path | R/W | 0 | Analog signal processing single or double path 0: double path, 1: single path |
| Reg_4[6] | cm | R/W | 1 | Color mode or Mono mode(used only in sub-sampling mode) 0: Mono mode, 1: color mode |
| Reg_4[5] | rrc | R/W | 0 | reverse read column 0: forward readout, 1: reverse readout |
| Reg_4[4] | rrr | R/W | 0 | reverse read row 0: forward readout, 1: reverse readout |
| Reg_4[3:2] | cf[1:0] | R/W | 0 | column frequency 00: Normal readout without sub-sampling, 01: 1/2 sub-sampling 10: 1/4 sub-sampling, 11: 1/8 sub-sampling |
| Reg_4[1:0] | rf[1:0] | R/W | 0 | row frequency 00: Normal readout without sub-sampling, 01: 1/2 sub-sampling |

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| | | | | 10: 1/4 sub-sampling, 11: 1/8 sub-sampling |
| Reg_5[2:0] | wcp_in[10:8] | R/W | 0 | window column pointer |
| Reg_6[7:0] | wcp_in[7:0] | R/W | 0 | window column pointer |
| Reg_7[2:0] | wcw_in[10:8] | R/W | 1287 | window column width |
| Reg_8[7:0] | wcw_in[7:0] | R/W | 1287 | window column width |
| Reg_9[2:0] | wrp[10:8] | R/W | 0 | window row pointer |
| Reg_10[7:0] | wrp[7:0] | R/W | 0 | window row pointer |
| Reg_11[2:0] | wrd | R/W | 1027 | window row depth |
| Reg_12[7:0] | wrd | R/W | 1027 | window row depth |
| Reg_13[5] | CDS_ext2_in | R/W | 0 | CDS timing extension to 2 times of normal CDS timing for 48M pixel rate |
| Reg_13[4] | row_ave | R/W | 0 | row average for row sub-sampling |
| Reg_13[3] | dir_ave | R/W | 0 | direction of average 0: the same direction of rrc 1: reverse direction of rrc |
| Reg_13[2] | mono_ave | R/W | 0 | used for mono color filter 0: row<i> & row<i+2> average 1: row<i> & row<i+1> average |
| Reg_13[1] | Seq_exp | R/W | 1 | |
| Reg_13[0] | Snap_ena | R/W | 0 | |
| Reg_14[2:0] | cov[10:8] | R/W | 0 | column overhead: used to increase line time |
| Reg_15[7:0] | cov[7:0] | R/W | 0 | column overhead: used to increase line time |

| | | | | |
|-------------|------------------|-----|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reg_16[0] | mode_chg_reg | R/W | 0 | It is used to reset the full sensor array and exposure address when critical operation mode is changed(useful only that register "flag" is set to 1 and reset of the full sensor array and exposure address will start till the first new frame is readout after register "flag" is set to 1) . It will be reset by the same mechanism that flag register be reset. |
| Reg_17[5:0] | LPF[13:8] | R/W | 1027 | Line per frame: total frame time = (LPF+1)+2 lines |
| Reg_18[7:0] | LPF[7:0] | R/W | 1027 | Line per frame: total frame time = (LPF+1)+2 lines |
| Reg_19[5:0] | ny[13:8] | R/W | 0 | Exposure time start point offset in line resolution |
| Reg_20[7:0] | ny[7:0] | R/W | 0 | Exposure time start point offset in line resolution |
| Reg_21[2:0] | Ne[10:8] | R/W | 0 | Exposure time start point offset in pixel resolution |
| Reg_22[7:0] | ne[7:0] | R/W | 0 | Exposure time start point offset in pixel resolution |
| Reg_23[6:5] | Frnt_gain[1:0] | R/W | 0 | Front gain |
| Reg_23[4:0] | Global_gain[4:0] | R/W | 0 | Global gain |
| Reg_24[3] | Dac_B_sign | R/W | 1 | The Dac sign of color B |
| Reg_24[2] | Dac_G1_sign | R/W | 1 | The Dac sign of color G1 |
| Reg_24[1] | Dac_G0_sign | R/W | 1 | The Dac sign of color G0 |
| Reg_24[0] | Dac_R_sign | R/W | 1 | The Dac sign of color R |
| Reg_25[7:0] | Dac_B[7:0] | R/W | 0 | The Dac value of color B (Dac setting is done by signed-magnitude) |
| Reg_26[7:0] | Dac_G1[7:0] | R/W | 0 | The Dac value of color G1 |
| Reg_27[7:0] | Dac_G0[7:0] | R/W | 0 | The Dac value of color G0 |
| Reg_28[7:0] | Dac_R[7:0] | R/W | 0 | The Dac value of color R |
| Reg_29[3:0] | Cg_B[3:0] | R/W | 0 | Color gain of color B |

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| Reg_30[3:0] | Cg_G1[3:0] | R/W | 0 | Color gain of color G1 |
| Reg_31[3:0] | Cg_G0[3:0] | R/W | 0 | Color gain of color G0 |
| Reg_32[3:0] | Cg_R[3:0] | R/W | 0 | Color gain of color R |
| Reg_33[2:0] | acc1_B[10:8] | R/W | 0 | 2's complement value for digital calibration of color B |
| Reg_34[7:0] | acc1_B[7:0] | R/W | 0 | 2's complement value for digital calibration of color G1 |
| Reg_35[2:0] | acc1_G1[10:8] | R/W | 0 | 2's complement value for digital calibration of color G1 |
| Reg_36[7:0] | acc1_G1[7:0] | R/W | 0 | 2's complement value for digital calibration of color G1 |
| Reg_37[2:0] | acc1_G0[10:8] | R/W | 0 | 2's complement value for digital calibration of color G0 |
| Reg_38[7:0] | acc1_G0[7:0] | R/W | 0 | 2's complement value for digital calibration of color G0 |
| Reg_39[2:0] | acc1_R[10:8] | R/W | 0 | 2's complement value for digital calibration of color R |
| Reg_40[7:0] | acc1_R[7:0] | R/W | 0 | 2's complement value for digital calibration of color R |
| Reg_41[0] | flag | R/W | 0 | used to synchronize register update by frame when fast_i2c is set 0 It will be reset to 0 till the first new frame is readout after it is set to 1 |

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|-------------|----------------------|-----|----|--------------------------------------------------------------------------------------------------------------------------------------------------|
| Reg_42[2] | mode_chg_ena | R/W | 1 | when it is set to 1, the mode related registers will be updated only after mode_chg is set to 1 |
| Reg_42[1] | dac_pg_lag | R/W | 0 | DAC & PGA update delay 1 frame automatically |
| Reg_42[0] | fast_i2c | R/W | 0 | fast update of synchronized i2c registers |
| Reg_43[7] | sfrst_ena | R/W | 0 | source follower reset enable |
| Reg_43[6:5] | shr_ext[1:0] | R/W | 1 | SHR extension CDS_rst1: 00 : 9 ck12 01 : 14 ck12 10 : 19 ck12 11 : 24 ck12 |
| Reg_43[4:2] | comp_crv[2:0] | R/W | 0 | companding curve |
| Reg_43[1] | Vsync_p | R/W | 0 | Vsync polarity |
| Reg_43[0] | Hsync_p | R/W | 0 | Hsync polarity |
| Reg_44[7:6] | dacor[1:0] | R/W | 0 | DAC output range 00 : x1/8 01 : x1/4 10 : x1/2 11 : x1 |
| Reg_44[5:0] | offset[5:0] | R/W | 1 | offset value for ABC |
| Reg_45[7:0] | Threshold_1_by4[7:0] | R/W | 25 | Threshold_1 divided by 4 for defect compensation |
| Reg_46[7:0] | Threshold_2_by4[7:0] | R/W | 13 | Threshold_2 divided by 4 for defect compensation |
| Reg_47[5] | Defect_EnH | R/W | 0 | 0 : Defect compensation disable 1 : Defect compensation enable |
| Reg_47[4] | ABC_EnH | R/W | 0 | ABC enable high |
| Reg_47[3] | Line_Avg_EnH | R/W | 0 | Line based digital calibration enable high |
| Reg_47[2] | Frm_Avg_EnH | R/W | 0 | Frame based digital calibration enable high |
| Reg_47[1:0] | Avg_num_index[1:0] | R/W | 1 | Number of pixels for Frame based digital calibration 00 : 4 pixels 01 : 8 pixels 10 : 16 pixels 11 : 32 pixels |
| Reg_48[6] | DSC_pd | R/W | 0 | Digital timing(column address, CDS timing) disable |

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| | | | | in redundancy rows |
| Reg_48[5] | CDS_pd | R/W | 0 | Analog CDS disable in redundancy rows |
| Reg_48[4] | ASP_pd | R/W | 0 | Analog signal path disable in redundancy rows |
| Reg_48[3] | path_chg | R/W | 0 | Combination of (single_path, path_chg): 00 : even pixels processed by even signal path, odd pixels processed by odd signal path 01 : even pixels processed by odd signal path, odd pixels processed by even signal path 10 : all pixels are processed by the even signal path 11 : all pixels are processed by the odd signal path |
| Reg_48[2] | even_path | R/W | 0 | Useful only when mono mode and double path readout, even pixels and odd pixels are all processed, but just only either even or odd pixels are readout 0: for readout even path 1: for readout odd path |
| Reg_48[1] | csbE | R/W | 0 | 1 for closing the even analog signal path |
| Reg_48[0] | csbO | R/W | 0 | 1 for closing the odd analog signal path |
| Reg_49[5] | Test_EnH | R/W | 0 | Test enable high |
| Reg_49[4] | dqio_EnL | R/W | 0 | dqio enable low |
| Reg_49[3] | scan_Dac | R/W | 0 | scan DAC(useful only when Test_EnH=1) |
| Reg_49[2] | scan_Color | R/W | 0 | scan Color Gain(useful only when Test_EnH=1) |
| Reg_49[1] | scan_Global | R/W | 0 | scan Global Gain(useful only when Test_EnH=1) |
| Reg_49[0] | pga_test_EnH | R/W | 0 | pga test enable high |
| Reg_50[5] | sfswt_EnH | R/W | 0 | Source follower dynamic switch enable high |
| Reg_50[4] | offset_EnL | R/W | 0 | Analog signal path offset enable low |
| Reg_50[3] | zdly_plus | R/W | 0 | Zeroing switch delay plus enable high |
| Reg_50[2] | cds_zero_EnH | R/W | 0 | Zeroing switch in CDS enable high |
| Reg_50[1] | vga_ave_EnH | R/W | 0 | VGA resolution averaged out enable high |
| Reg_50[0] | cif_ave_EnH | R/W | 0 | CIF resolution averaged out enable high |
| Reg_51[7] | cds_fast_EnH | R/W | 0 | CDS block fast enable high |
| Reg_51[6] | dac_fast_EnH | R/W | 0 | DAC block fast enable high |
| Reg_51[5] | pga_fast_EnH | R/W | 0 | PGA block fast enable high |
| Reg_51[4] | adc_fast_EnH | R/W | 0 | ADC block fast enable high |
| Reg_51[3] | cds_EnL | R/W | 0 | CDS block enable low |
| Reg_51[2] | dac_EnL | R/W | 0 | DAC block enable low |
| Reg_51[1] | pga_EnL | R/W | 0 | PGA block enable low |
| Reg_51[0] | adc_EnL | R/W | 0 | ADC block enable low |
| Reg_52[5:4] | cdsbias[1:0] | R/W | 0 | CDS bias current option |
| Reg_52[3:2] | vlrst[1:0] | R/W | 0 | VLRST voltage level option |
| Reg_52[1:0] | vdday[1:0] | R/W | 0 | VDDAY voltage level option |
| Reg_53[6] | reg_EnL | R/W | 0 | Regulator block enable low |
| Reg_53[5:4] | regfast[1:0] | R/W | 1 | Regulator current level option |
| Reg_53[3:2] | vrefLG[1:0] | R/W | 0 | Reference voltage (VRT-VRB) range option |
| Reg_53[1:0] | vddd[1:0] | R/W | 0 | Internal regulated digital power X_VDDD voltage level option |
| Reg_54[7] | T_gp1 | R/W | 0 | 0 : CDS clock = even path clock 1 : CDS clock = odd path clock |
| Reg_54[6] | T_gp2 | R/W | 0 | 0 : X_VDDD switch ON diode connect from VDDD 1 : X_VDDD switch OFF diode connect from VDDD |
| Reg_54[5] | extvdy_EnH | R/W | 0 | External VDDAY enable high |
| Reg_54[4] | vayNdrv_EnH | R/W | 0 | VDDAY with NMOS drive enable high |

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| Reg_54[3] | extR_EnH | R/W | 0 | Bias current generated by external resistor enable high |
| Reg_54[2] | bgp_EnH | R/W | 0 | Bandgap reference enable high |
| Reg_54[1] | ext2p5v_EnH | R/W | 0 | External 2.5V digital power enable high |
| Reg_54[0] | 2p5vNdrv_EnH | R/W | 0 | X_VDDD with NMOS drive enable high |
| Reg_55[0] | sfpd | R/W | 0 | software power down: Sensor core will be powered down if it is set to 1 but I2C interface will be live. |
| Reg_56[0] | soft_rst | R/W | 0 | software reset: It is used to reset the full registers to default value. |
| Reg_57[3] | Dac_B_sign_ABC | R | 0 | The converge sign of color B when ABC is enable |
| Reg_57[2] | Dac_G1_sign_ABC | R | 0 | The converge sign of color G1 when ABC is enable |
| Reg_57[1] | Dac_G0_sign_ABC | R | 0 | The converge sign of color G0 when ABC is enable |
| Reg_57[0] | Dac_R_sign_ABC | R | 0 | The converge sign of color R when ABC is enable |
| Reg_58[7:0] | Dac_B_ABC[7:0] | R | 0 | The converge value of color B when ABC is enabled |
| Reg_59[7:0] | Dac_G1_ABC[7:0] | R | 0 | The converge value of color G1 when ABC is enabled |
| Reg_60[7:0] | Dac_G0_ABC[7:0] | R | 0 | The converge value of color G0 when ABC is enabled |
| Reg_61[7:0] | Dac_R_ABC[7:0] | R | 0 | The converge value of color R when ABC is enabled |
| Reg_62[4:0] | acc1_B_FrmAvg[12:8] | R | 0 | The converge value of color B when frame based digital calibration is enabled. |
| Reg_63[7:0] | acc1_B_FrmAvg[7:0] | R | 0 | The converge value of color B when frame based digital calibration is enabled. |
| Reg_64[4:0] | acc1_G1_FrmAvg[12:8] | R | 0 | The converge value of color G1 when frame based digital calibration is enabled. |
| Reg_65[7:0] | acc1_G1_FrmAvg[7:0] | R | 0 | The converge value of color G1 when frame based digital calibration is enabled. |
| Reg_66[4:0] | acc1_G0_FrmAvg[12:8] | R | 0 | The converge value of color G0 when frame based digital calibration is enabled. |
| Reg_67[7:0] | acc1_G0_FrmAvg[7:0] | R | 0 | The converge value of color G0 when frame based digital calibration is enabled. |
| Reg_68[4:0] | acc1_R_FrmAvg[12:8] | R | 0 | The converge value of color R when frame based digital calibration is enabled. |
| Reg_69[7:0] | acc1_R_FrmAvg[7:0] | R | 0 | The converge value of color R when frame based digital calibration is enabled. |

| | | | | | | | |
|---|---------------|----|-----|-------|---------|--------------|-----|
| 0 | Part_ID[11:4] | | | | | | R |
| 1 | Part_ID[3:0] | | | VerID | | | R |
| 2 | | | | | | Np_i2c[3:0] | R/W |
| 3 | | | | | | Np[5:0] | R/W |
| 4 | single_path | cm | rrc | rrr | cf[1:0] | rf[1:0] | R/W |
| 5 | | | | | | wcp_in[10:8] | R/W |

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| 6 | wcp_in[7:0] | | | | | | | R/W | |
| 7 | | | | | | | wcw_in[10:8] | R/W | |
| 8 | wcw_in[7:0] | | | | | | | R/W | |
| 9 | | | | | | | wrp[10:8] | R/W | |
| 10 | wrp[7:0] | | | | | | | R/W | |
| 11 | | | | | | | wrd[10:8] | R/W | |
| 12 | wrd[7:0] | | | | | | | R/W | |
| 13 | | CDS_ext2_in | row_ave | dir_ave | mono_ave | seq_exp | snap_ena | R/W | |
| 14 | | | | | | | cov[10:8] | R/W | |
| 15 | cov[7:0] | | | | | | | R/W | |
| 16 | | | | | | | | mode_chg_reg | R/W |
| 17 | | | | | | | LPF[13:8] | R/W | |
| 18 | LPF[7:0] | | | | | | | R/W | |
| 19 | | | | | | | ny[13:8] | R/W | |
| 20 | ny[7:0] | | | | | | | R/W | |
| 21 | | | | | | | ne[10:8] | R/W | |
| 22 | ne[7:0] | | | | | | | R/W | |
| 23 | | Frnt_gain[1:0] | Global_gain[4:0] | | | | | R/W | |
| 24 | | | | | Dac_B_sign | Dac_G1_sign | Dac_G0_sign | Dac_R_sign | R/W |
| 25 | Dac_B[7:0] | | | | | | | R/W | |
| 26 | Dac_G1[7:0] | | | | | | | R/W | |
| 27 | Dac_G0[7:0] | | | | | | | R/W | |
| 28 | Dac_R[7:0] | | | | | | | R/W | |
| 29 | | | | | | | Cg_B[3:0] | R/W | |
| 30 | | | | | | | Cg_G1[3:0] | R/W | |
| 31 | | | | | | | Cg_G0[3:0] | R/W | |
| 32 | | | | | | | Cg_R[3:0] | R/W | |
| 33 | | | | | | | acc1_B[10:8] | R/W | |
| 34 | acc1_B[7:0] | | | | | | | R/W | |
| 35 | | | | | | | acc1_G1[10:8] | R/W | |
| 36 | acc1_G1[7:0] | | | | | | | R/W | |

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| | | | | | | | | | |
|----|-----------------|--------------|--------------|---------------|----------------|---------------------|--------------------|----------------|-----|
| 37 | | | | | | acc1_G0[10:8] | | | R/W |
| 38 | acc1_G0[7:0] | | | | | | | | R/W |
| 39 | | | | | | acc1_R[10:8] | | | R/W |
| 40 | acc1_R[7:0] | | | | | | | | R/W |
| 41 | | | | | | | | flag | R/W |
| 42 | | | | | | mode_chg_ena | dac_pg_lag | fast_i2c | R/W |
| 43 | sfrst_ena | shr_ext[1:0] | | comp_crv[2:0] | | Vsync_p | Hsync_p | | R/W |
| 44 | dacor[1:0] | | offset[5:0] | | | | | | R/W |
| 45 | Threshold_1_by4 | | | | | | | | R/W |
| 46 | Threshold_2_by4 | | | | | | | | R/W |
| 47 | | | Defect_EnH | ABC_EnH | Line_Avg_EnH | Frm_Avg_EnH | Avg_num_index[1:0] | | R/W |
| 48 | | DS_pd | CDS_pd | ASP_pd | path_chg | even_path | csbE | csbO | R/W |
| 49 | | | Test_EnH | dqio_EnL | scan_Dac | scan_Color | scan_Global | pga_test_EnH | R/W |
| 50 | | | sfswt_EnH | offset_EnL | zdly_plus | cds_zero_EnH | vga_ave_EnH | cif_ave_EnH | R/W |
| 51 | cds_fast_EnH | dac_fast_EnH | pga_fast_EnH | adc_fast_EnH | cds_EnL | dac_EnL | pga_EnL | adc_EnL | R/W |
| 52 | cdsbias[1:0] | | | vlrst[1:0] | | vdday[1:0] | | | R/W |
| 53 | | reg_EnL | regfast[1:0] | | vrefLG[1:0] | | vddd[1:0] | | R/W |
| 54 | | | extvdy_EnH | vayNdrv_EnH | extR_EnH | bgp_EnH | ext2p5v_EnH | 2p5vNdrv_EnH | R/W |
| 55 | | | | | | | | sfpd | R/W |
| 56 | | | | | | | | soft_rst | R/W |
| 57 | | | | | Dac_B_sign_ABC | Dac_G1_sign_ABC | Dac_G0_sign_ABC | Dac_R_sign_ABC | R |
| 58 | Dac_B_ABC[7:0] | | | | | | | | R |
| 59 | Dac_G1_ABC[7:0] | | | | | | | | R |
| 60 | Dac_G0_ABC[7:0] | | | | | | | | R |
| 61 | Dac_R_ABC[7:0] | | | | | | | | R |
| 62 | | | | | | acc1_B_FrmAvg[12:8] | | | R |

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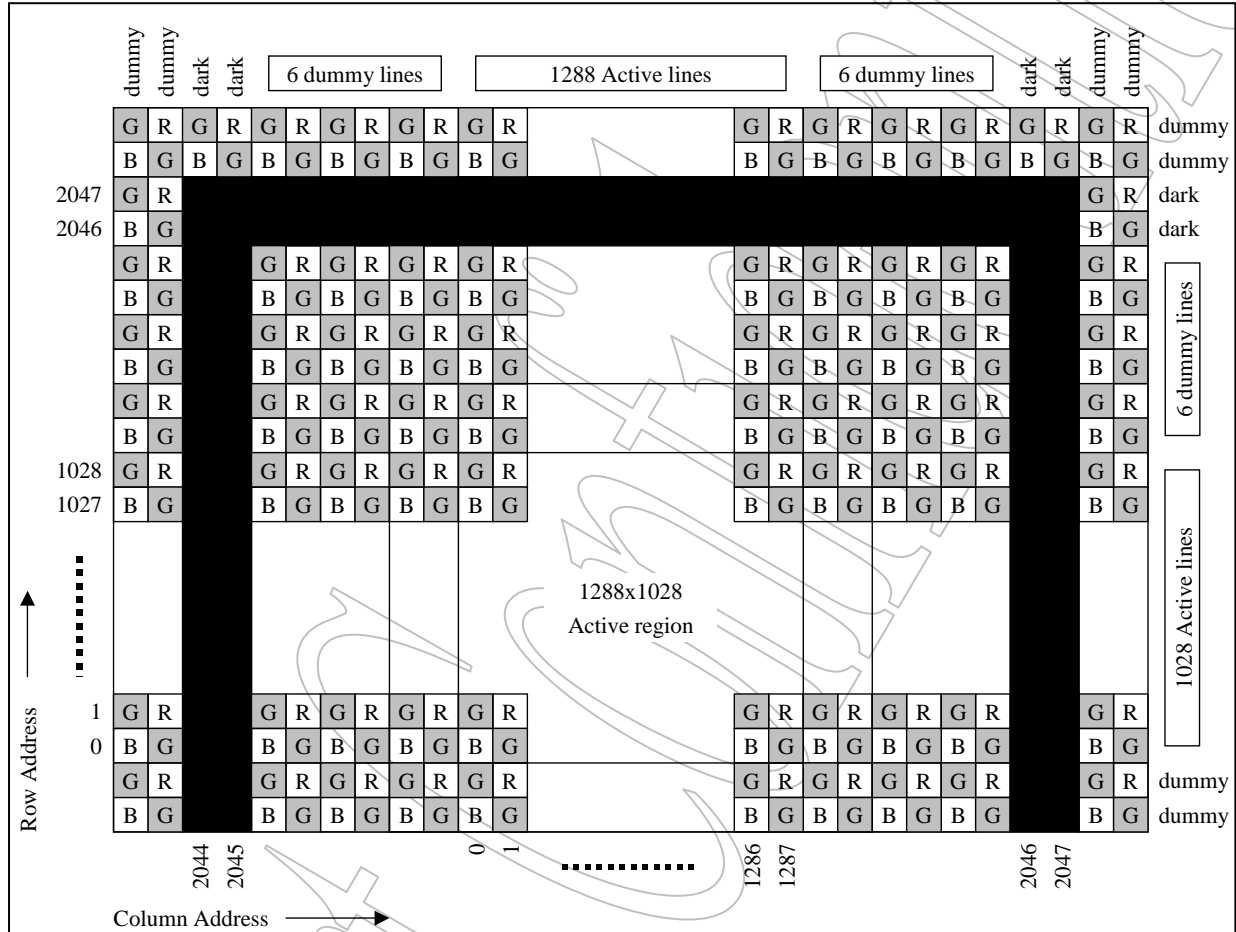
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| | | | |
|----|--|----------------------|---|
| 63 | | acc1_B_FrmAvg[7:0] | R |
| 64 | | acc1_G1_FrmAvg[12:8] | R |
| 65 | | acc1_G1_FrmAvg[7:0] | R |
| 66 | | acc1_G0_FrmAvg[12:8] | R |
| 67 | | acc1_G0_FrmAvg[7:0] | R |
| 68 | | acc1_R_FrmAvg[12:8] | R |
| 69 | | acc1_R_FrmAvg[7:0] | R |

4. Function description

4.1 Pixel array



4.1.1 Output Timing

1.3M(1280 X 1024)-pixel readout: (with 8 column and 4 row for color interpolation)

cf[1:0] = 0, rf[1:0]=0, cm =1, single_path = 0, row_ave= 0, CDS_ext2_in =1.

wcp[10:0]=0, wcw_in[10:0]=1287, wrp[10:0]=0, wrd[10:0]=1027,

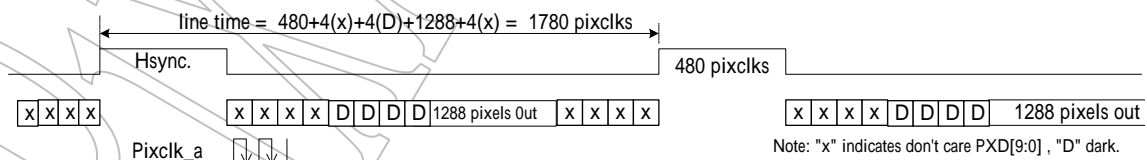


Fig 4.1.1-1 Inter-line timing (default)

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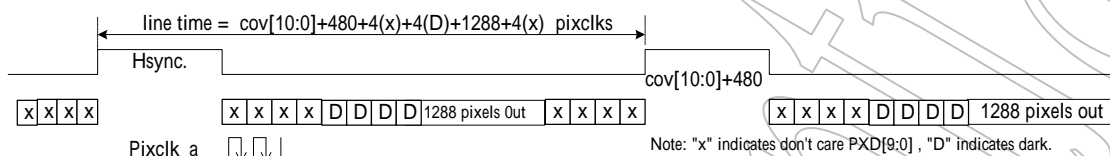


Fig 4.1.1-2 Inter-line timing (programmable)

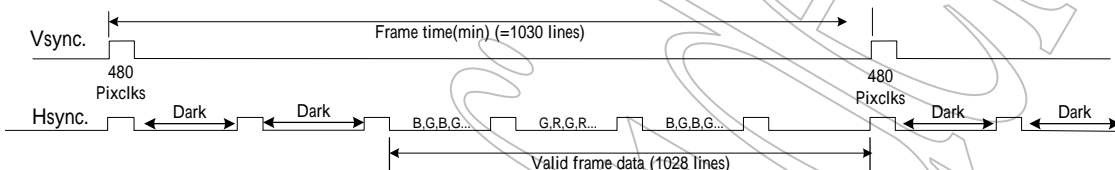


Fig 4.1.1-3 Inter-frame timing (default)

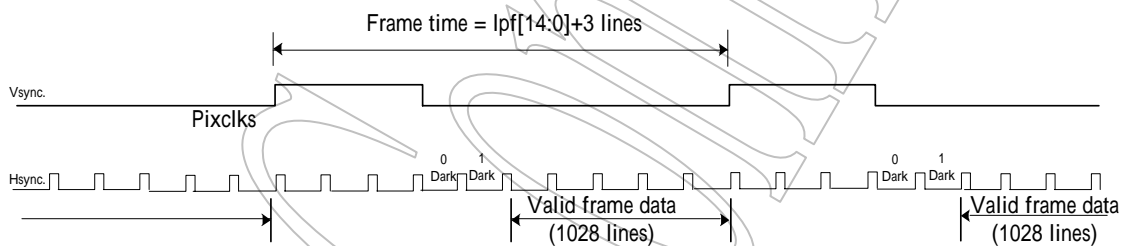


Fig 4.1.1-4 Inter-frame timing (programmable)

4.2 Windowing

Users are allowed to define window size as well as window location in PAS005B. Window size can range from 1x8 to 1288x1028. The location of window can be anywhere in the pixel array. Window size and window location is defined by register wcp_in, wew_in, wrp and wrd: the wcp_in defines the starting column while wrp defines the starting row of the window; the wew_in define the column width of the window and wrd define the row depth of the window.

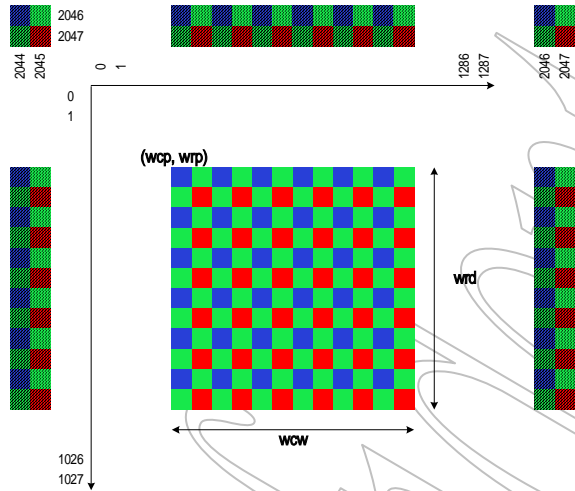


Fig. 4.2-1

4.2.1 Output timing of windowing

Hardware windowing VGA(640 X 480) pixels readout: (with 4 column and 2 row for color interpolation)

cf[1:0] = 0, rf[1:0]=0, cm =1, single_path = 0, row_ave= 0, CDS_ext2_in=1.

wcp[10:0]=0, wcw_in[10:0]=643,

wrp[10:0]=0, wrd[10:0]=481,

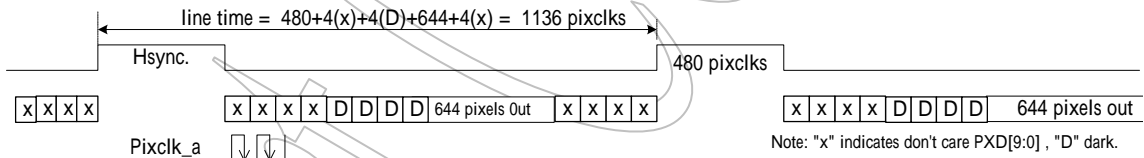


Fig 4.2.1-1 Inter-line timing (default)

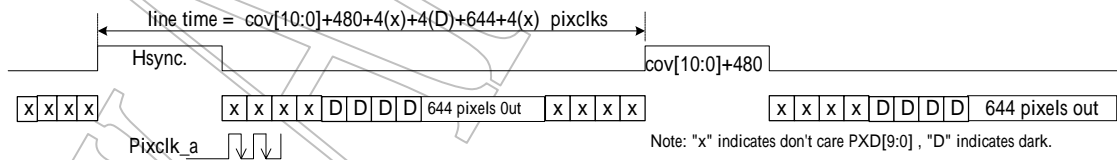


Fig 4.2.1-2 Inter-line timing (programmable)

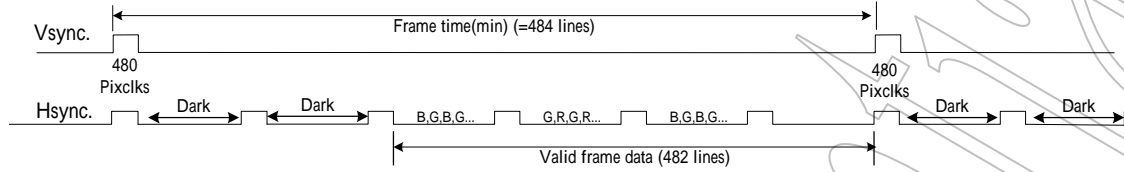


Fig 4.2.1-3 Inter-frame timing (default)

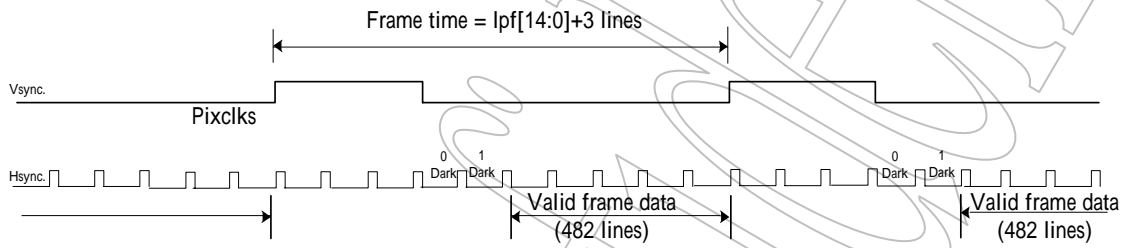


Fig 4.2.1-4 Inter-frame timing (programmable)

Hardware windowing CIF(352 X 288) pixels readout:(with 4 column and 2 row for color interpolation)

cf[1:0] = 0, rf[1:0]=0, cm = 1, single_path = 0, row_ave= 0, CDS_ext2_in = 1.

wcp[10:0]=0, wcw_in[10:0]=355,

wrp[10:0]=0, wrd[10:0]=289,

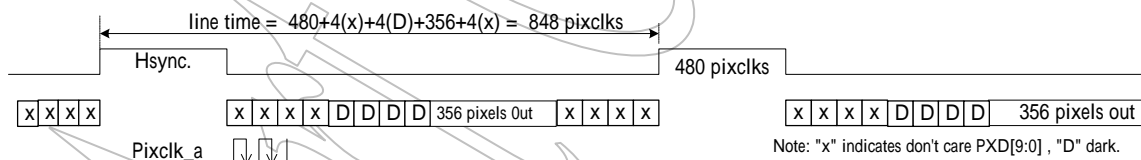


Fig 4.2.1-5 Inter-line timing (default)

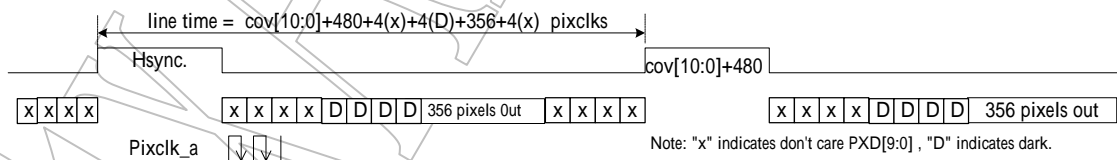


Fig 4.2.1-6 Inter-line timing (programmable)

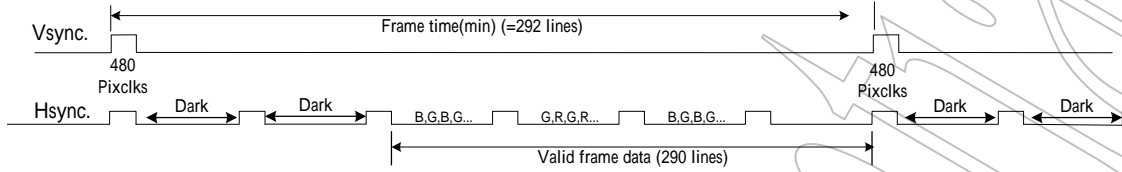


Fig 4.2.1-7. Inter-frame timing (default)

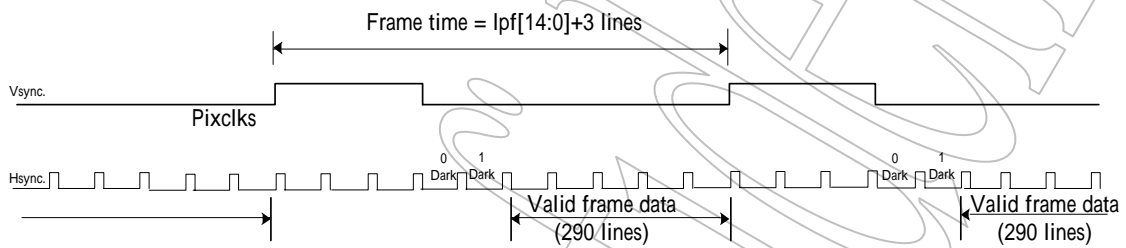
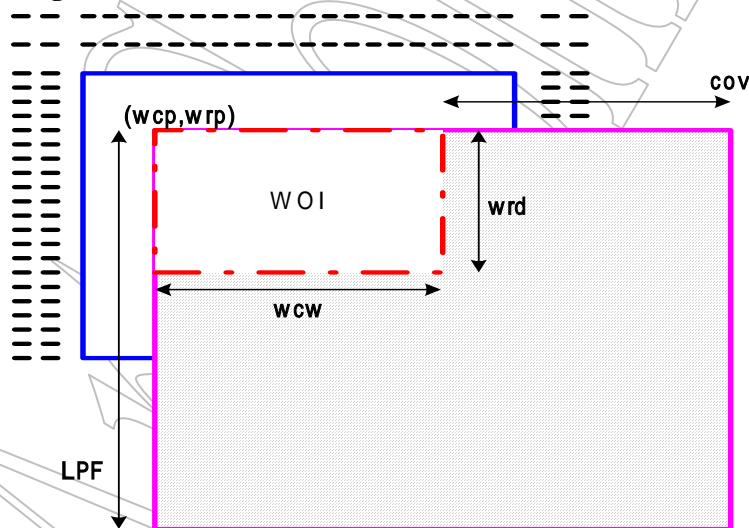


Fig 4.2.1-8 Inter-frame timing (programmable)

4.2.2 Y Programming



Frame time: $(LPF+1) + 2$ Line time

Fig 4.2.2-1

The Blue circle indicate the maximum 1288 X 1028 active pixels, Red circle the window of interest, and Pink circle the Virtual Frame. Virtual Frame represents the frame time and the size of it indicates that the frame time is the time to readout all the pixels in this Virtual Frame.

The readout row and column is programmed by WOI(wcp, wrp, wcw, wrd), Sub-sampling(cf, rf) and readout direction(rrc, rrr). The readout rows and columns are shown in the following figures.

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4.3 Sub-sampling

4.3.1 Sub-sampling—in color mode

PAS005B can be programmed to output in VGA and CIF size. In VGA sub-sampling mode, both vertical and horizontal pixels are sub-sampled at 1/2, while in CIF sub-sampling mode, sub-sampled at 1/4. By programming row frequency(rf), column frequency(cf) and color mode(cm), PAS005B performs sub-sampling. The maximum sub-sampling rate is 1/8. As shown in Fig. 4.3, by setting cm=1, rf=01 and cf=01, PAS005B outputs in VGA sub-sampling mode.

**In color mode PAS005B outputs in Bayer pattern while mono mode outputs mono data.

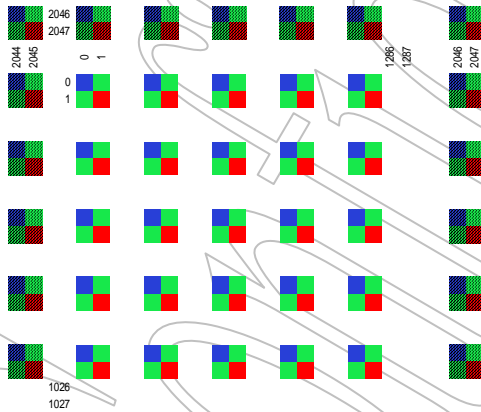


Fig 4.3.1

4.3.2 Sub-sampling—in mono mode

PAS005B can also be programmed to output in VGA and CIF size in mono mode. In VGA sub-sampling mode, both vertical and horizontal pixels are sub-sampled at 1/2, while in CIF sub-sampling mode sub-sampled at 1/4. By programming row frequency(rf), column frequency(cf) and color mode(cm), PAS005B performs sub-sampling. The maximum sub-sampling rate is 1/8.

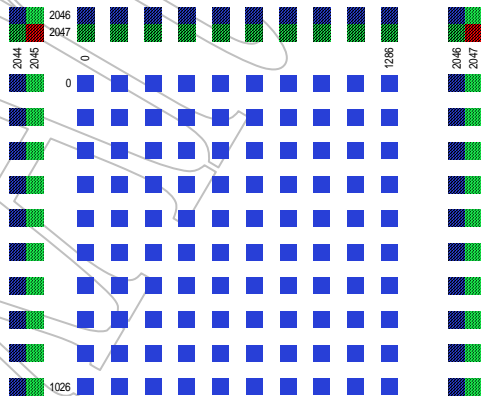


Fig 4.3.2

**Windowing and sub-sampling can be used independently.

4.3.3 Sub-sampling with average--in color mode

PAS005B supports average data output in sub-sampling mode in color mode. In this mode, the PAS005B averages the pixel data with surrounding pixels that are with the same color. For example, in VGA-sub-sampling, in which both vertical and horizontal pixels are sub-sampled at 1/2, the sub-sampled pixel data are

$$[i,j] = ([i,j] + [i,j+2] + [i+2,j] + [i+2,j+2]) / 4,$$

while in CIF-sub-sampling, the sub-sampled pixel data are

$$[i,j] = ([i,j] + [i,j+2] + [i,j+4] + [i,j+6] + [i+2,j] + [i+2,j+2] + [i+2,j+4] + [i+2,j+6]) / 8.$$

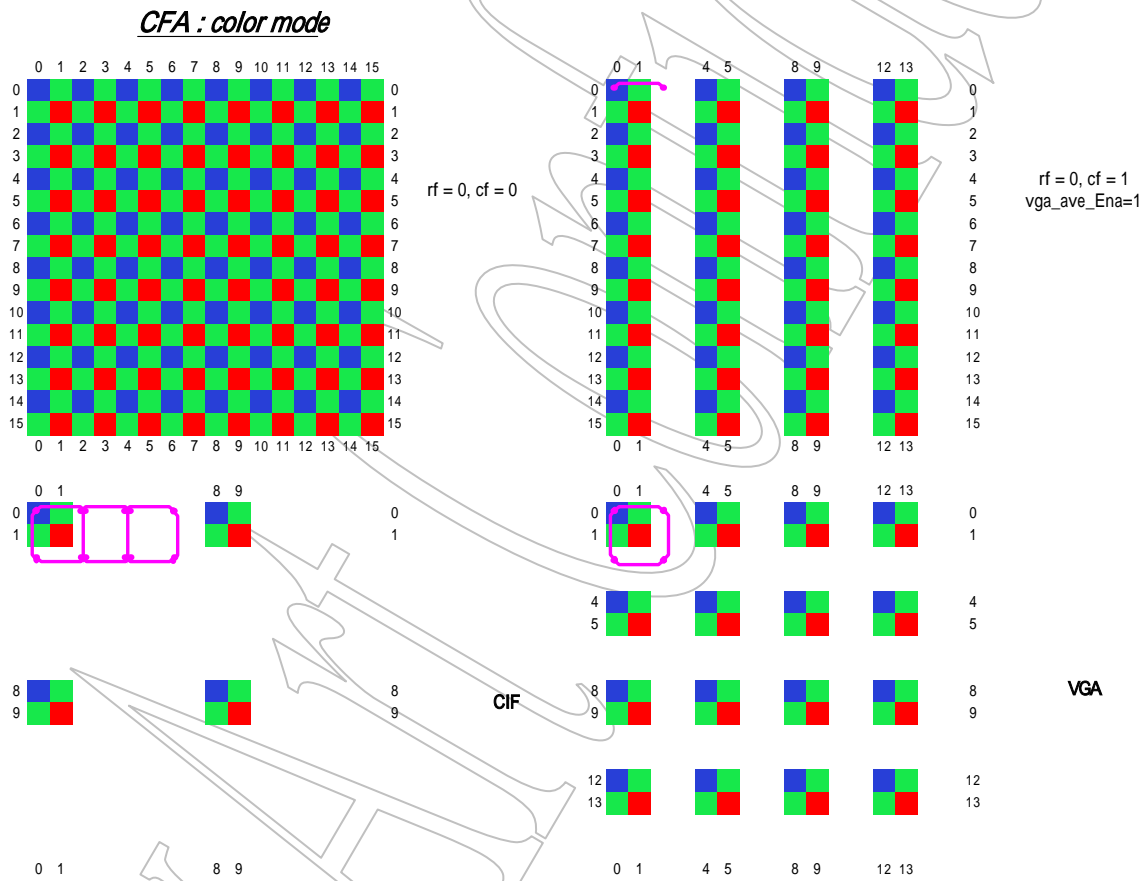


Fig 4.3.3

4.3.4 Sub-sampling with average—in mono mode

PAS005B supports average data output in sub-sampling mode in mono mode. In this mode, the PAS005B averages the pixel data with surrounding pixels that are with the same color. For example, in VGA-sub-sampling, in which both vertical and horizontal pixels are sub-sampled at 1/2, the sub-sampled pixel data are

$$[i,j] = ([i,j] + [i+1,j]) / 2,$$

while in CIF-sub-sampling, the sub-sampled pixel data are

$$[i,j] = ([i,j] + [i,j+2] + [i+2,j] + [i+2,j+2]) / 4,$$

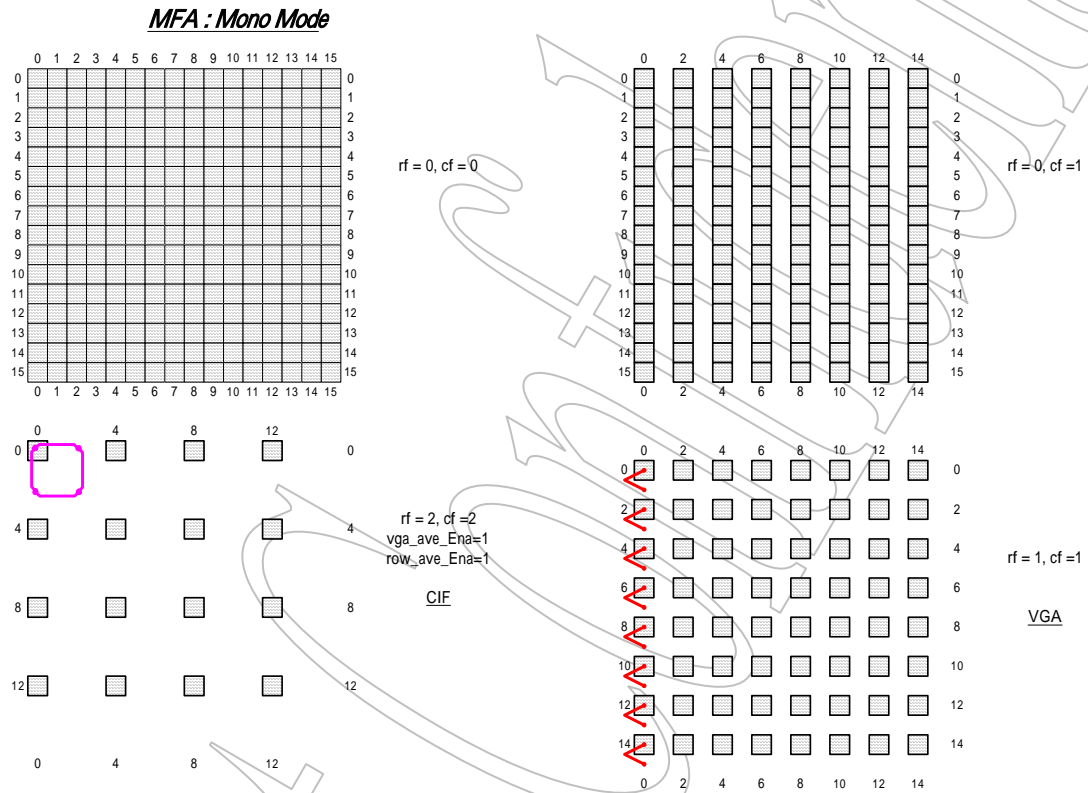


Fig 4.3.4

4.3.5 Output timing of sub-sampling

4.3.5.1 Sub-sampling VGA(640X480) from (1288 X 968) windowing:

(with 4 column and 2 row for color-interpolation)

$cf[1:0] = 1, rf[1:0]=1$, sub-sampling rate $(1/2,1/2)$,

$wcp[10:0]=0, wcw_in[10:0]=1287$, column pixels $644=(1287+1)/2$,

$wrp[10:0]=0, wrd[10:0]=963$, row pixel $484=(963+1)/2$,

$cm = 1, single_path = 1, row_ave = 1, CDS_ext2_in = 1$.

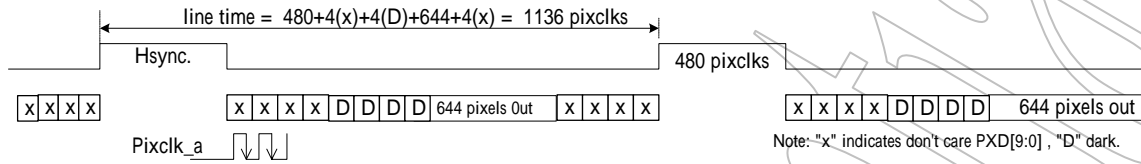


Fig 4.3.5.1-1 Inter-line timing (default)

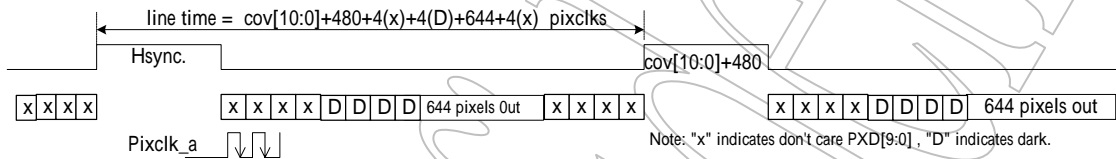


Fig 4.3.5.1-2 Inter-line timing (programmable)

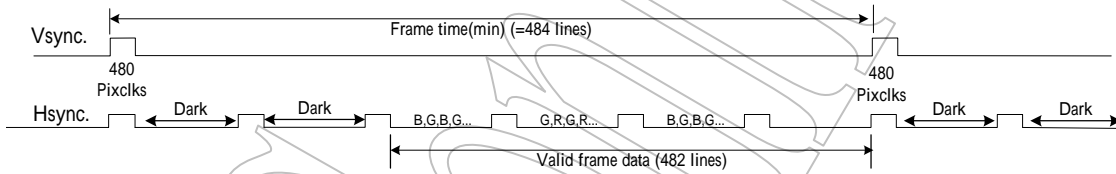


Fig 4.3.5.1-3 Inter-frame timing (default)

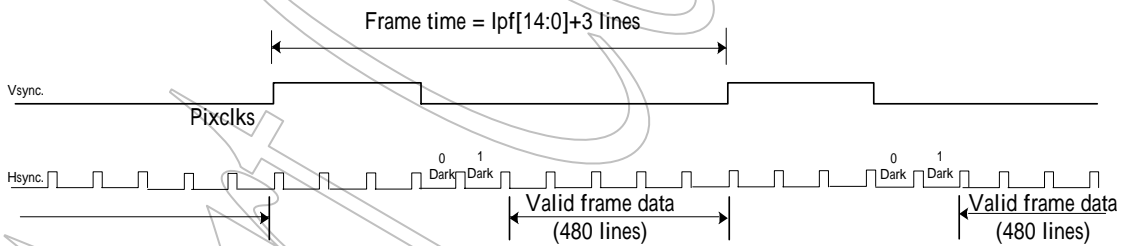


Fig 4.3.5.1-4 Inter-frame timing (programmable)

4.3.5.2. Sub-sampling QVGA(318X240) from (1288 X 968) windowing:

(with 4 column and 2 row for color interpolation)

cf[1:0]=2, rf[1:0]=2, sub-sampling rate (1/4,1/4),cm =1, single_path = 1, row_ave= 1, CDS_ext2_in =1.

wcp[10:0]=0, wcv_in[10:0]=1287, column pixels 322=(1287+1)/4,

wrp[10:0]=0, wrd[10:0]=967, row pixel 242=(967+1)/4,

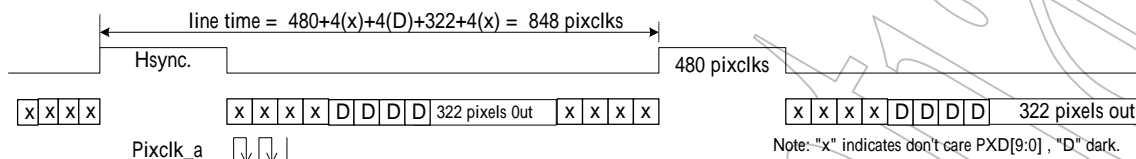


Fig .4.3.5.2-1. Inter-line timing (default)

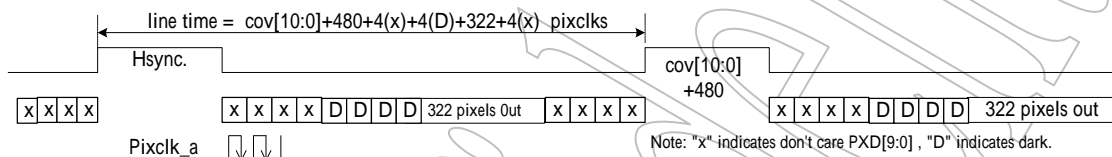


Fig 4.3.5.2-2 Inter-line timing (programmable)

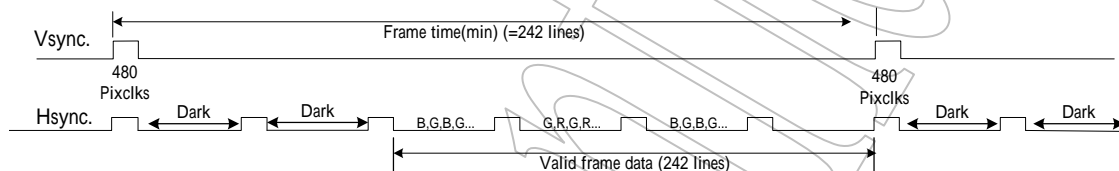


Fig 4.3.5.2-3 Inter-frame timing (default)

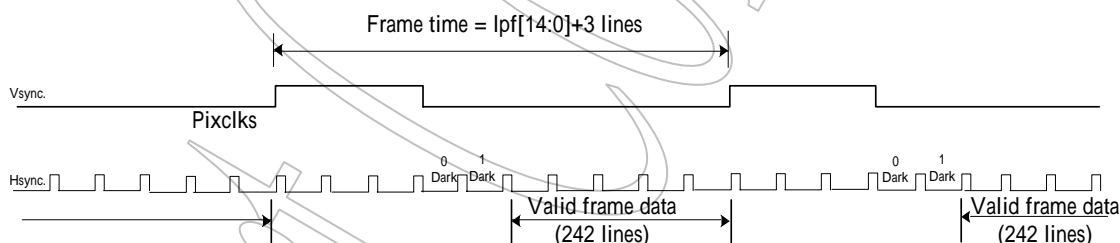


Fig .4.3.5.2-4 Inter-frame timing (programmable)

4.4 Snapshot mode

Typically, the snapshot mode must work with the aid of an external mechanical shutter. PAS005 support two types of snapshot mode to fit the different exposure time request.

Snapshot mode 1: register seq_exp=1

When the exposure time is longer than the mechanical shutter speed limitation, snapshot mode 1 is chosen. The exposure period is now controlled by the mechanisms of shutter opening and close as shown in Fig. 4. The mechanical shutter can be trigger by the clock edge of output signal Vsync and all pixels will be exposure

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concurrently. The shutter closing edge must be earlier than the Vsync edge by programming proper register value LPF (Line-per-Frame). The suggested setting of ny (ne) in this mode is 0 to guarantee simultaneous exposure in the shutter opening period. However, different setting is acceptable depend on application.

Snapshot mode 2: register seq_exp=0

When the exposure time is less than the mechanical shutter speed limitation, snapshot mode 2 is chosen. The exposure period is now controlled by exposure start point and shutter closing edge as shown in Fig. 5. The exposure starting point is setted by register ny and ne, and the sensor array will be started to exposure simultaneously. Again, the shutter closing edge must be earlier than the Vsync edge.

All these two snapshot modes can be external triggered by pin “Sync” as shown in Fig. 4.4-1 and 4.4-2.

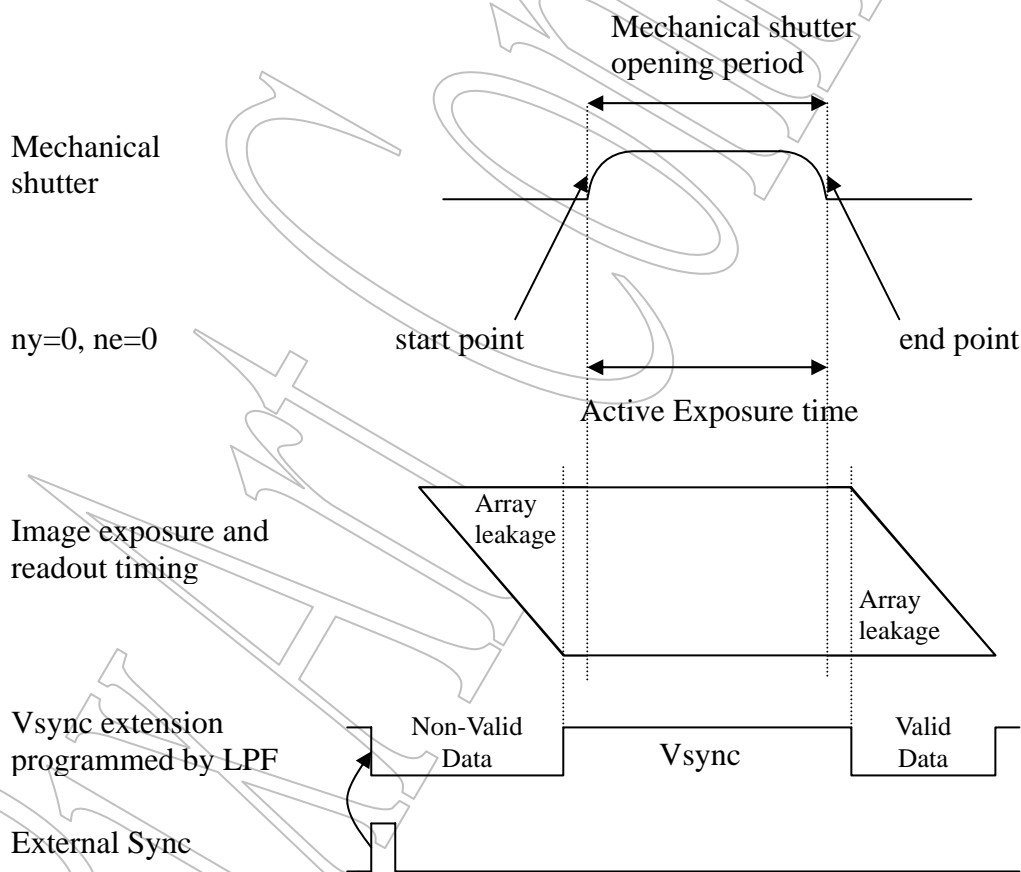


Fig. 4.4-1 Snapshot mode one – Exposure time controlled by shutter.

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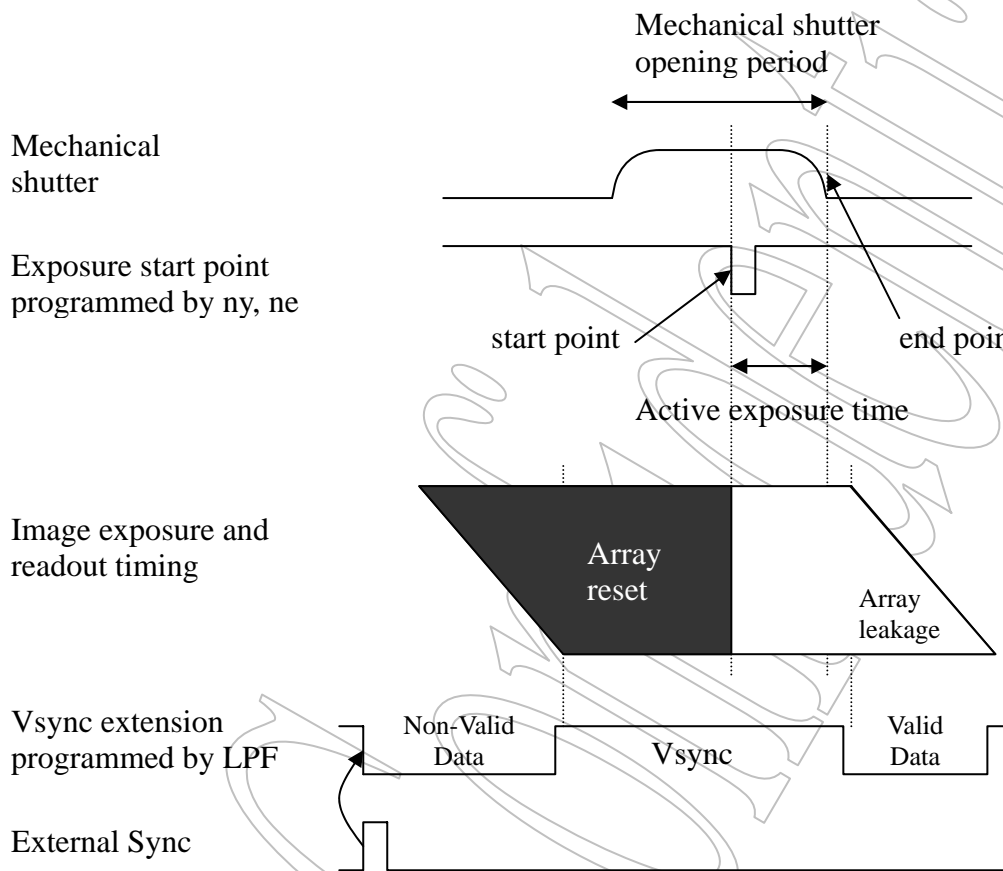


Fig. 4.4-2 Snapshot mode two – Exposure time smaller than shutter speed limitation.

4.5 External synchronization control

The sensor core timing can be reset by external “Sync” pin. The internal counter will start from initial point at the rising edge of trigger signal “Sync”. Meanwhile, Vsync signal is reset to zero. Waiting the coming of Vsync pulse, a valid frame will be output after the pulse with the programmed ny, ne and gain code, as shown in Figs. 4.4-1 and 4.4-2.

4.6 Frame rate

$$\text{Frame rate} = \frac{1}{(LPF + 1 + 2) \cdot t_line}$$

| | |
|-------------------------|---------------------------------------|
| Nov time | 10 us (240 ck @24M) |
| line time | t_line = 1534 ck |
| frame time | t_frame = 1030*1534 ck |
| Mega frame rate | = 24M/(1030*1534) = 15.2 fps |
| VGA(average) | = 24M/((654+240*2)*486) = 43.5 fps |
| VGA(non-average) | = 24M/((654+240*1)*486) = 55.2 fps |

X:
Int: 8
Dk: 4
Dummy: 2
Y:
Int: 4
Dk: 2

2 path:
t_line = x+8+4+2
= x+14
LPF = y+4+2
= y+6

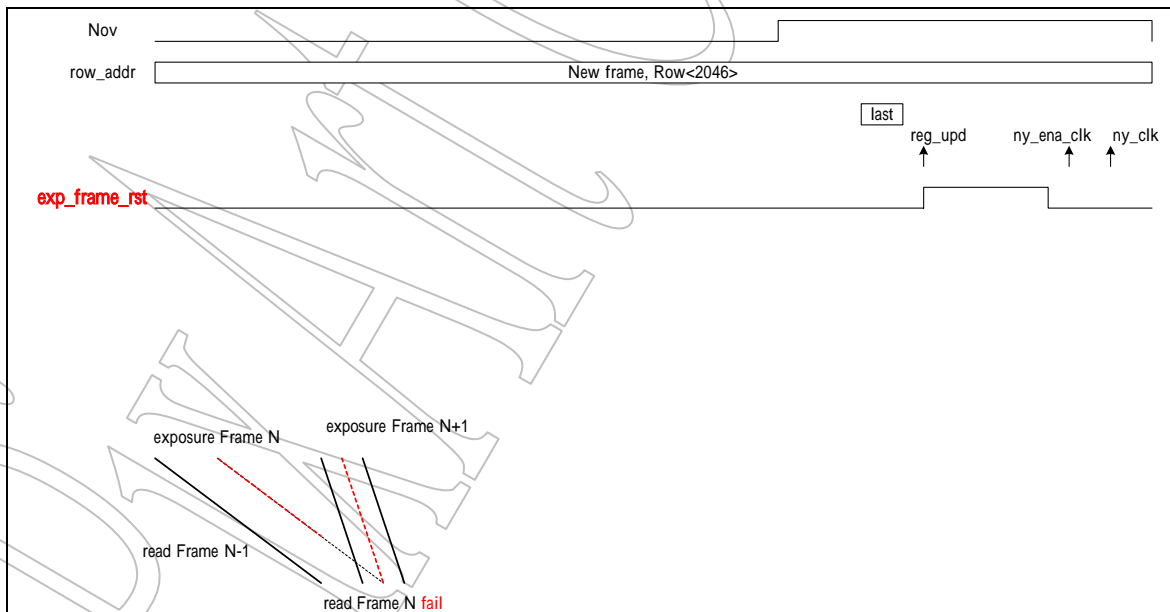
↑
Double_path

| | |
|----------------|-----------------------------------------|
| VGA(average) | Pixel clock = 16.5 M when 30 fps |
|----------------|-----------------------------------------|

↓
Single_path

| | |
|---------------------------------------|--------------------------------------|
| VGA(average) (single_path) | = 24M/((1306+480)*486) = 27.6 fps |
| VGA(non-average) (single_path) | = 24M/((1306+240)*486) = 32 fps |

1 path:
t_line = (x+8+4+1)*2
= 2*x+26
LPF = y+4+2
= y+6



In normal operating condition, register 3 ~ 40 are synchronized by frame. The programming method is

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writing the registers followed by setting “flag” register to 1. Registers 4 ~ 15 are some critical registers that influent the sensor cell array. If the readout pixels aare changed, register 16(mode_chg_reg) should be set to 1 to reset the full array. So the programming sequence is writing the registers, set mode_chg, than set flag. If mode_chg_ena register is 1, these registers will be protected unchanged till setting mode_chg followed by setting flag.

4.7 Exposure Programming

The Exposure Time calculation of PAS005 is based on the following sequence:

1. System clk
2. Pxclk
3. Frame rate
4. Exposure time
5. Equivalent exposure line and pixel number
6. Register (Ny)offset_ny,(Ne) offset_ne

For a given Sysclk, pxclk and EX-time:

$$N_p = \text{Sysclk} / \text{pxclk}.$$

The Exposure Time calculation of PAS005 is based on the following Register:

| Register | Register | R/W | Default (Decimal) | Description |
|------------|--------------|-----|-------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| Reg_3[5:0] | Np[5:0] | R/W | 2 | Pixel rate = frequency of I_Sysclk / Np Programming range of Np: 1~63 |
| Reg_4[7] | single_path | R/W | 0 | Analog signal processing single or double path 0: double path, 1: single path |
| Reg_4[6] | cm | R/W | 1 | Color mode or Mono mode(used only in sub-sampling mode) 0: Mono mode, 1: color mode |
| Reg_4[3:2] | cf[1:0] | R/W | 0 | column frequency 00: Normal readout without sub-sampling, 01: 1/2 sub-sampling 10: 1/4 sub-sampling, 11: 1/8 sub-sampling |
| Reg_4[1:0] | rf[1:0] | R/W | 0 | row frequency 00: Normal readout without sub-sampling, 01: 1/2 sub-sampling 10: 1/4 sub-sampling, 11: 1/8 sub-sampling |
| Reg_5[2:0] | wcp_in[10:8] | R/W | 0 | window column pointer |
| Reg_6[7:0] | wcp_in[7:0] | R/W | 0 | window column pointer |
| Reg_7[2:0] | wcw_in[10:8] | R/W | 1287 | window column width |
| Reg_8[7:0] | wcw_in[7:0] | R/W | 1287 | window column width |
| Reg_9[2:0] | wrp[10:8] | R/W | 0 | window row pointer |

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| | | | | |
|--------------------|--------------------|-----|------|-------------------------------------------------------------------------|
| Reg_10[7:0] | wrp[7:0] | R/W | 0 | window row pointer |
| Reg_11[2:0] | wrd | R/W | 1027 | window row depth |
| Reg_12[7:0] | wrd | R/W | 1027 | window row depth |
| Reg_13[5] | CDS_ext2_in | R/W | 0 | CDS timing extension to 2 times of normal CDS timing for 48M pixel rate |
| Reg_13[4] | row_ave | R/W | 0 | row average for row sub-sampling |
| Reg_13[0] | Snap_ena | R/W | 0 | |
| Reg_14[2:0] | Cov[10:8] | R/W | 0 | column overhead: used to increase line time |
| Reg_15[7:0] | Cov[7:0] | R/W | 0 | column overhead: used to increase line time |
| Reg_17[5:0] | LPF[13:8] | R/W | 1027 | Line per frame: total frame time = (LPF+1)+2 lines |
| Reg_18[7:0] | LPF[7:0] | R/W | 1027 | Line per frame: total frame time = (LPF+1)+2 lines |
| Reg_19[5:0] | ny[13:8] | R/W | 0 | Exposure time start point offset in line resolution |
| Reg_20[7:0] | ny[7:0] | R/W | 0 | Exposure time start point offset in line resolution |
| Reg_21[5:0] | ne[13:8] | R/W | 0 | Exposure time start point offset in pixel resolution |
| Reg_22[7:0] | ne[7:0] | R/W | 0 | Exposure time start point offset in pixel resolution |

EXAMPLE 1: MEGA Exposure time setting

when system clock 48M hz
 pxclk 24M hz
 exposure time 8/120 sec
 Please keep L_P_F = 1027
 And Calculate Ny = ? and Ne = ? ,

Application

| | |
|------------|----|
| System_clk | Np |
| 48 | 2 |

| |
|----------------|
| Pixel_clk(MHz) |
| 24 |

| | |
|-----------------|-----------------|
| Power frequency | EX_time (x/120) |
| 60HZ | 8 |
| L_P_F | cov |
| 1027 | 0 |

| |
|---------------|
| frame_rate<10 |
| |

Register setting

| | | | |
|------|-------------|-------|-------------|
| CM | row_average | CDSx2 | single_path |
| 1 | 0 | 1 | 0 |
| Wcw | Wrd | cf | rf |
| 1287 | 1027 | 0 | 0 |

Key in Register

| | | | |
|-------|-----|-----|--------|
| L_P_F | Ny | Ne | t_line |
| 1027 | 131 | 159 | 1780 |

1. Exposure Tim = { [(L_P_F+1+2) - Ny] * t_line - Ne' } / Pxclk
2. t_line = (active_line_pixel + t_nov + 12) = 1300 + 480 + 12 = **1780 Pxclk**

t_nov = **480 + Cov Pxclk**

3. Ny = INT[(L_P_F+3) - ((EX_Time * Pxclk) / t_line)]

131 = INT[(1027+3) - ((8/120 * 24 M) / 1780)]

4. Ne = Res[(L_P_F + 3) - ((EX_Time * Pixel_clk) / t_line)] * active_line_pixel

159 = Res[(1027 + 3) - ((8/120 * 24 M) / 1780)] * 1300

5. Frame rate = $\frac{1}{(L_P_F + 1 + 2) \cdot t_line}$ = 1/(1027+3)* 1780 = **13 (per/sec)**

EXAMPLE 2: VGA Exposure time setting

when system clock 48M hz
 pxclk 16M hz
 exposure time 4/120 sec
 Please keep L_P_F = 483
 and Calculate Ny = ? and Ne = ?,



Application

| | | |
|------------|----|-----------|
| System_clk | Np | Pixel_clk |
| 48 | 3 | 16 |

| | |
|-----------------|-----------------|
| Power frequency | EX_time (x/120) |
| 60HZ | 4 |
| L_P_F | C_nov |
| 483 | 0 |

| |
|---------------|
| frame_rate<30 |
| 28.98046717 |

Register setting

| | | | |
|------|-------------|-------|-------------|
| CM | row_average | CDSx2 | single_path |
| 1 | 1 | 1 | 1 |
| Wcw | Wrd | Cf | rf |
| 1287 | 967 | 1 | 1 |

Key in Register

| | | | |
|-------|----|-----|--------|
| L_P_F | Ny | Ne | t_line |
| 483 | 16 | 332 | 1136 |

- 1.Exposure Tim = { [(LPF+1+2) - Ny] * t_line - Ne } / Pxclk
2. t_line = (active_line_pixel + t_nov + 12) = 644 + 480 + 12 = 1136 Pxclk
 t_nov = 480 + Cov Pxclk
3. Ny = INT[(L_P_F+3) - ((EX_Time * Pxclk) / t_line)]
 16 = INT [(483+3) - ((4 /120 * 16 M) / 1136)]
- 4.Ne = Res[(L_P_F + 3) - ((EX_Time * Pixel_clk) / t_line)] * active_line_pixel
 332 = Res[(483 + 3) - ((4/120 * 16 M) / 1136)] * 644
5. Frame rate = $\frac{1}{(LPF + 1 + 2) \cdot t_line}$ = 1/(483+3)* 1136 = 29

EXAMPLE_3: QVGA Exposure time setting

when system clock 48M hz
 pxclk 12M hz
 exposure time 2/120 sec
 Please keep L_P_F = 241
 and Calculate Ny = ? and Ne = ?,



Application

| | | |
|------------|----|-----------|
| System_clk | Np | Pixel_clk |
| 48 | 4 | 12 |

| | |
|-----------------|-----------------|
| Power frequency | EX_time (x/120) |
| 60HZ | 2 |
| L_P_F | C_nov |
| 241 | 6 |

| |
|-----------------|
| frame_rate < 60 |
| 59.9760096 |

Register setting

| | | | |
|------|-------------|-------|-------------|
| CM | row_average | CDSx2 | single_path |
| 1 | 1 | 1 | 1 |
| Wcw | Wrd | cf | rf |
| 1287 | 967 | 2 | 2 |

Key in Register

| | | | |
|-------|----|----|--------|
| L_P_F | Ny | Ne | t_line |
| 241 | 0 | 31 | 820 |

1. Exposure Time = { [(LPF+1+2) - Ny] * t_line - Ne } / Pxclk
2. t_line = (active_line_pixel + t_nov + 12) = 322 + 486 + 12 = 820 Pxclk
 t_nov = 480 + Cov Pxclk = 486 Pxclk
3. Ny = INT[(L_P_F+3) - ((EX_Time * Pxclk) / t_line)]
 0 = INT [(241 + 3) - ((2/120 * 12 M) / 820)]
4. Ne = Res[(L_P_F + 3) - ((EX_Time * Pixel_clk) / t_line)] * active_line_pixel
 31 = Res[(241 + 3) - ((2/120 * 12 M) / 820)] * 322
5. Frame rate = $\frac{1}{(LPF + 1 + 2) \cdot t_line}$ = 1/(241+3)* 820 = 60

EXAMPLE_4: Sunlight mode Exposure time setting

MEGA setting

when system clock 48M hz
 pxclk 12M hz
 exposure time < one line pxclk (sec)
 Please keep L_P_F = 1027
 And Calculate Ny = ? and Ne = ? ,

Application

| | |
|------------|----|
| System_clk | Np |
| 48 | 4 |

| |
|----------------|
| Pixel_clk(MHz) |
| 12 |

| | |
|-----------------|-----------------|
| Power frequency | EX_time (x/120) |
| 60HZ | X_t |
| L_P_F | cov |
| 1027 | 0 |

| |
|--|
| |
| |

Register setting

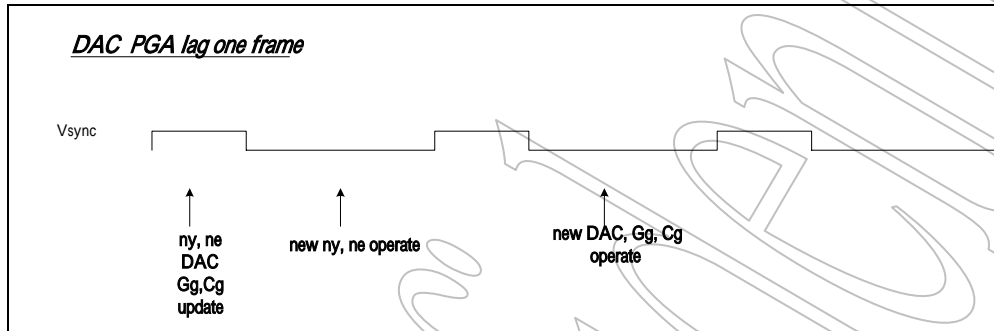
| | | | |
|------|-------------|-------|-------------|
| CM | row_average | CDSx2 | single_path |
| 1 | 0 | 1 | 0 |
| Wcw | Wrd | Cf | rf |
| 1287 | 1027 | 0 | 0 |

Key in Register

| | | | |
|-------|------|---------|--------|
| L_P_F | Ny | Ne<1300 | t_line |
| 1027 | 1029 | X_Ne | 1780 |

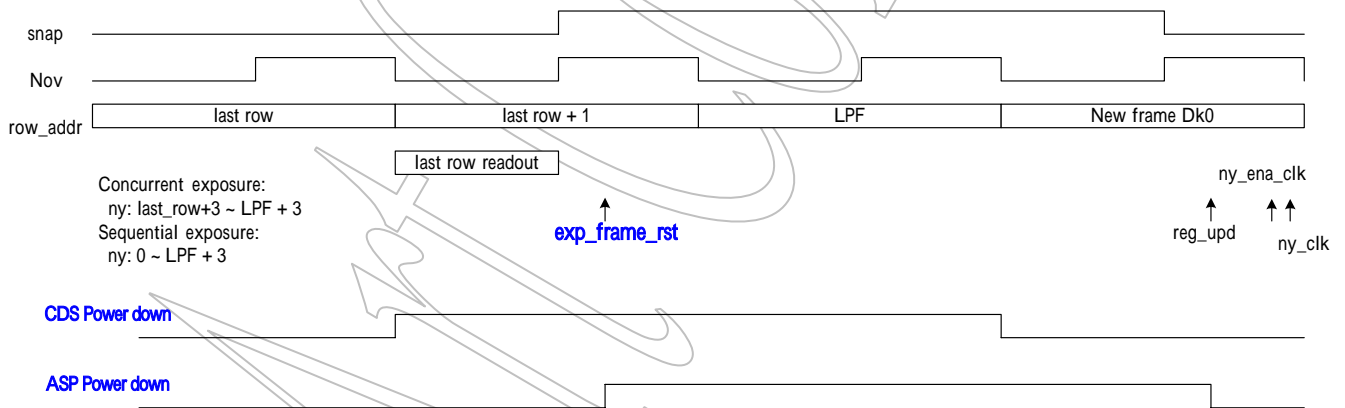
1. Exposure Tim (X_t) = [1030 – Ne (X_Ne)] /Pxclk (sec)
2. Frame rate = $\frac{1}{(LPF + 1 + 2) \cdot t_line}$ = 1 / (1027+3) * 1780 = 13

4.8 DAC & PGA lagging



Normally the readout of current frame will be exposed in the readout of the previous frame. To easily program the sensor, one can send exposure registers(ny, ne), dac and gain registers(Gg, Cg) followed by setting the “flag” register, the new updated DAC, Gg, Cg will operate 1 frame after new updated ny, ne automatically by programming the “dac_pg_lag” register.

4.9 Power down



Power down is classified as DSC_pd, CDS_pd and ASP_pd.

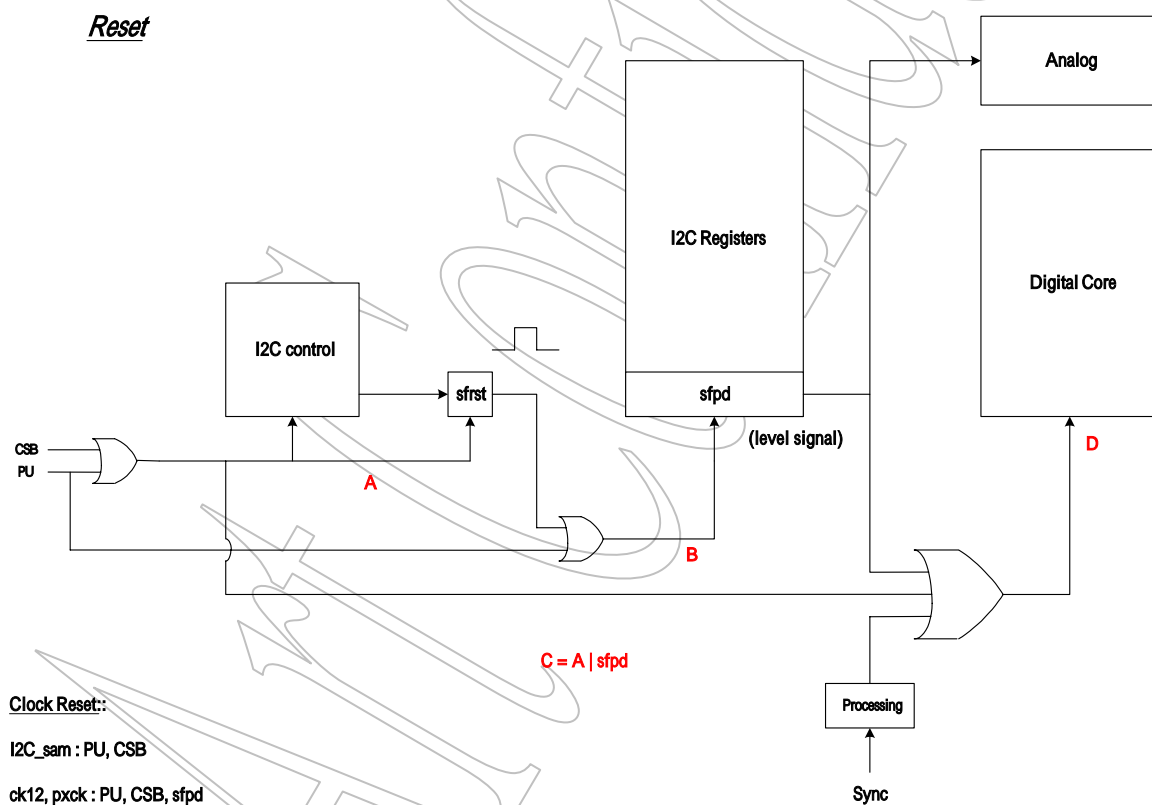
DSC_pd is to disable the digital timing(column address, CDS timing) in redundant rows.

CDS_pd pulls T_cds_EnL to 1 in redundant rows.

ASP_pd is to close DAC, PGA, and ADC in redundant rows.

4.10 Reset management

There are five kinds of reset: “pu”, “csb”, “sfpd”, “sfrst”, “sync”. “pu” is the most strong reset. It reset full chip. “csb” reset the full chip, but retain the register setting. “sfpd” reset the sensor core, but I2C interface is live. “sfrst” is an register signal. Every time it is programmed to “1”, all the I2C registers are reset. After that, it will be reset to zero. “sync” reset the sensor core timing. To avoid the recovering time problem, clock oscillating is designed to start a little time after “pu”, “csb” and “sfpd” reset is released.



5. I²C Bus

PAS005B supports I²C-bus transfer protocol and is acting as slave device. The 7 bits unique slave address is 1000000 and supports receiving / transmitting speed up to 400kHz.

5.1 I²C bus overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I²C bus. Normally both SDA and SCL lines are open collector structure and pull high by external pull-up resistors.
- Only the master can initiate a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition: A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Fig 5.1.
- Valid data: The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read/write control bit is the LSB of the first byte. Please refer to Fig 5.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge: The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

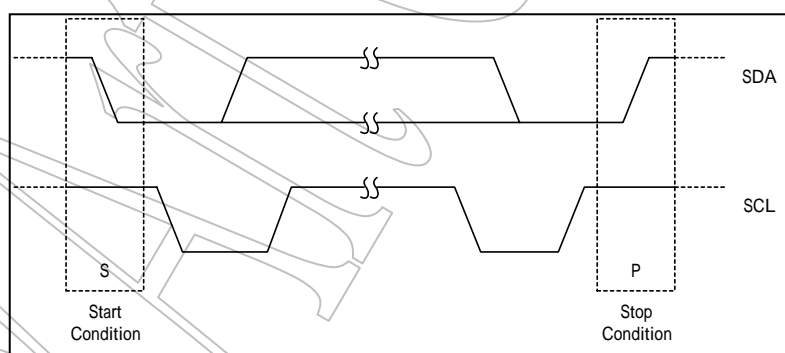


Fig 5.1 Start and Stop Conditions

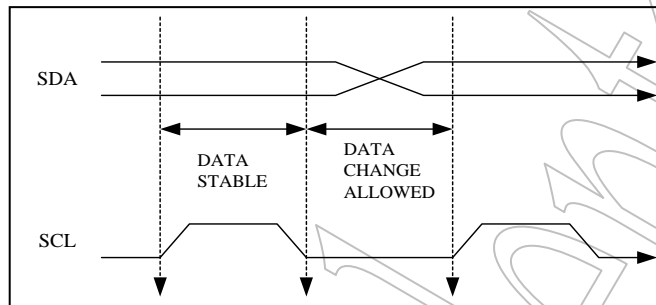


Fig 5.2 Valid Data

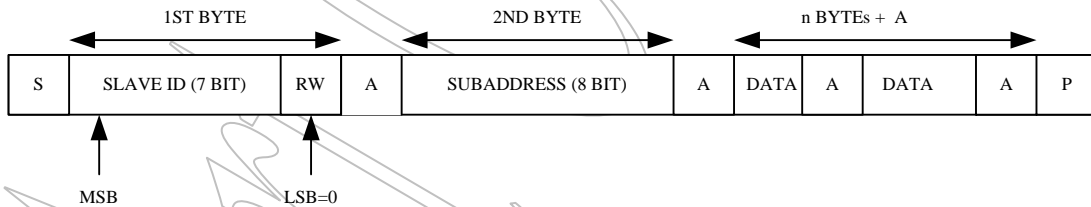
5.2 Data Transfer Format

5.2.1 Master transmits data to slave (write cycle)

- S : Start
- A : Acknowledge by slave
- P : Stop
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle.

RW=1 read cycle, RW=0 write cycle.

- SUBADDRESS : The address values of PAS005B internal control registers
(Please refer to PAS005B register description)



During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read/write control bit to SDA line. After slave(PAS005B) issues acknowledgment, the master places 2nd byte (sub-address) data on SDA line. Again follow the PAS005B acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS005B control register (address was assigned by 2nd byte). After PAS005B issue acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAS005B sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside PAS005B can be programming via this way. (Please refer to Fig 5.3.)

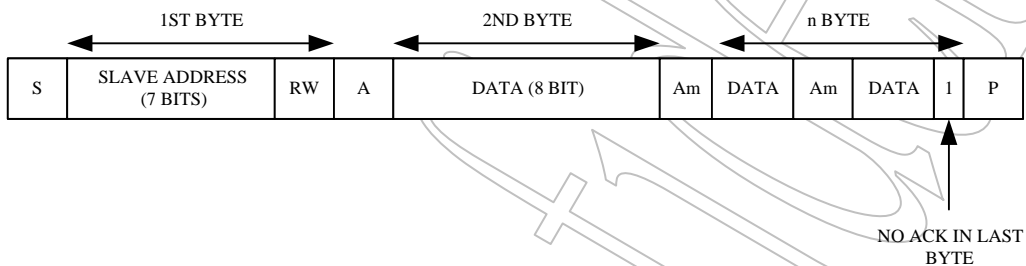
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5.2.2 Slave transmits data to master (read cycle)

- The sub-address was taken from previous write cycle
- The sub-address is automatically increment after each byte read
- Am : Acknowledge by master
- Note there is no acknowledgment from master after last byte read



During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read/write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAS005B. The 8 bit data was read from PAS005B internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAS005B place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAS005B) must releases SDA line to master to generate STOP condition. (Please refer to Fig 5.3.)

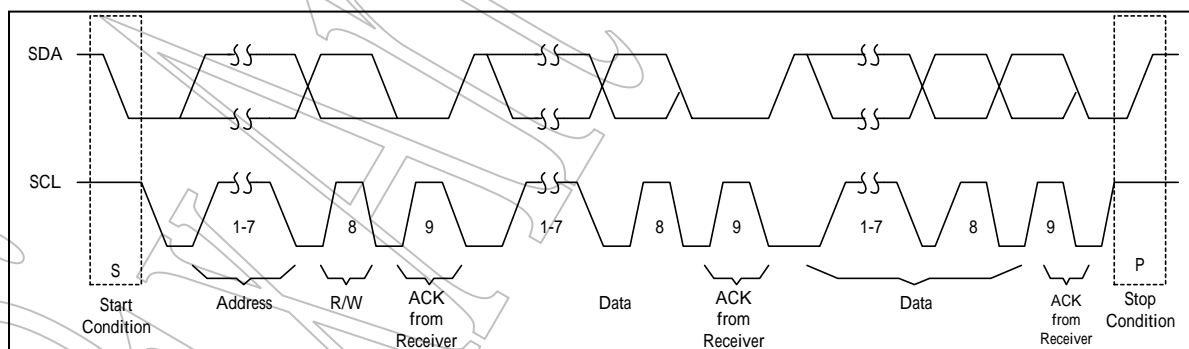


Fig 5.3 Data Transfer Format

5.3 I2C Bus Timing

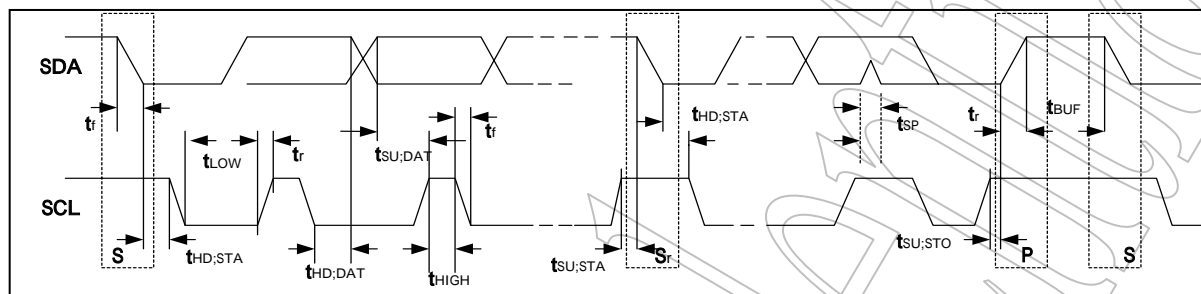


Fig 5.4 I2C Bus Timing

5.4 I2C Bus Timing Specification

| PARAMETER | SYMBOL | STANDARD-MODE | | UNIT |
|-------------------------------------------------------------------------------------------------|--------------|---------------|------|------------|
| | | MIN. | MAX. | |
| SCL clock frequency | f_{scl} | 10 | 400 | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD:STA}$ | 4.0 | - | us |
| Low period of the SCL clock | t_{LOW} | 4.7 | - | us |
| HIGH period of the SCL clock | t_{HIGH} | 0.75 | - | us |
| Set-up time for a repeated START condition | $t_{SU:STA}$ | 4.7 | - | us |
| Data hold time. For I2C-bus device | $t_{HD:DAT}$ | 0 | 3.45 | us |
| Data set-up time | $t_{SU:DAT}$ | 250 | - | ns |
| Rise time of both SDA and SCL signals | t_r | 30 | N.D. | ns(note 1) |
| Fall time of both SDA and SCL signals | t_f | 30 | N.D. | ns(note 1) |
| Set-up time for STOP condition | $t_{SU:STO}$ | 4.0 | - | us |
| Bus free time between a STOP and START | t_{BUF} | 4.7 | - | us |
| Capacitive load for each bus line | C_b | 1 | 15 | pF |
| Noise margin at LOW level for each connected device (including hysteresis) | V_{nL} | 0.1 V_{DD} | - | V |
| Noise margin at HIGH level for each connected device (including hysteresis) | V_{nH} | 0.2 V_{DD} | - | V |

Note: It depends on the "high" period time of SCL.

6. Specifications

Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Unit |
|--------|---------------------|------|---------|------|
| Vdd | DC supply voltage | -0.5 | 3.8 | V |
| Vin | DC input voltage | 0.5 | Vdd+0.5 | V |
| Vout | DC output voltage | -0.5 | Vdd+0.5 | V |
| Tstg | Storage temperature | TBD | TBD | |

DC Electrical Characteristics (VDD=3.0V±20%, Ta=10°C~40°C)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---------------------------------------------------------------------------------------------|--------------------------------------|---------|------|------|------|
| Type :PWR | | | | | |
| VDD | Analog and digital operating voltage | 2.4 | 3.0 | 3.6 | V |
| IDD | Operating Current | | 8 | | MA |
| Istby | Standby current | | 100 | | UA |
| Type :IN & I/O Reset and SYSCLK | | | | | |
| VIH | Input voltage HIGH | 2.0 | | VDD | V |
| VIL | Input voltage LOW | 0 | | 0.8 | V |
| Cin | Input capacitor | | | 10 | PF |
| I _{lkg} | Input leakage current | | TBD | | UA |
| Type : OUT & I/O for PXD0:7, PXCK, H/VSYNC & SDA, load 10pf, 1.2k , 3.0volts | | | | | |
| VOH | Output voltage HIGH | Vdd-0.2 | | | V |
| VOL | Output voltage LOW | | | 0.2 | V |

AC Operating Condition

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------|------------------------------|------|------|------|------|
| SYSCLK | Master clock frequency | 4.5 | | 48 | MHz |
| PXCK | Pixel clock output frequency | | | 1.5 | MHz |

Sensor Characteristics

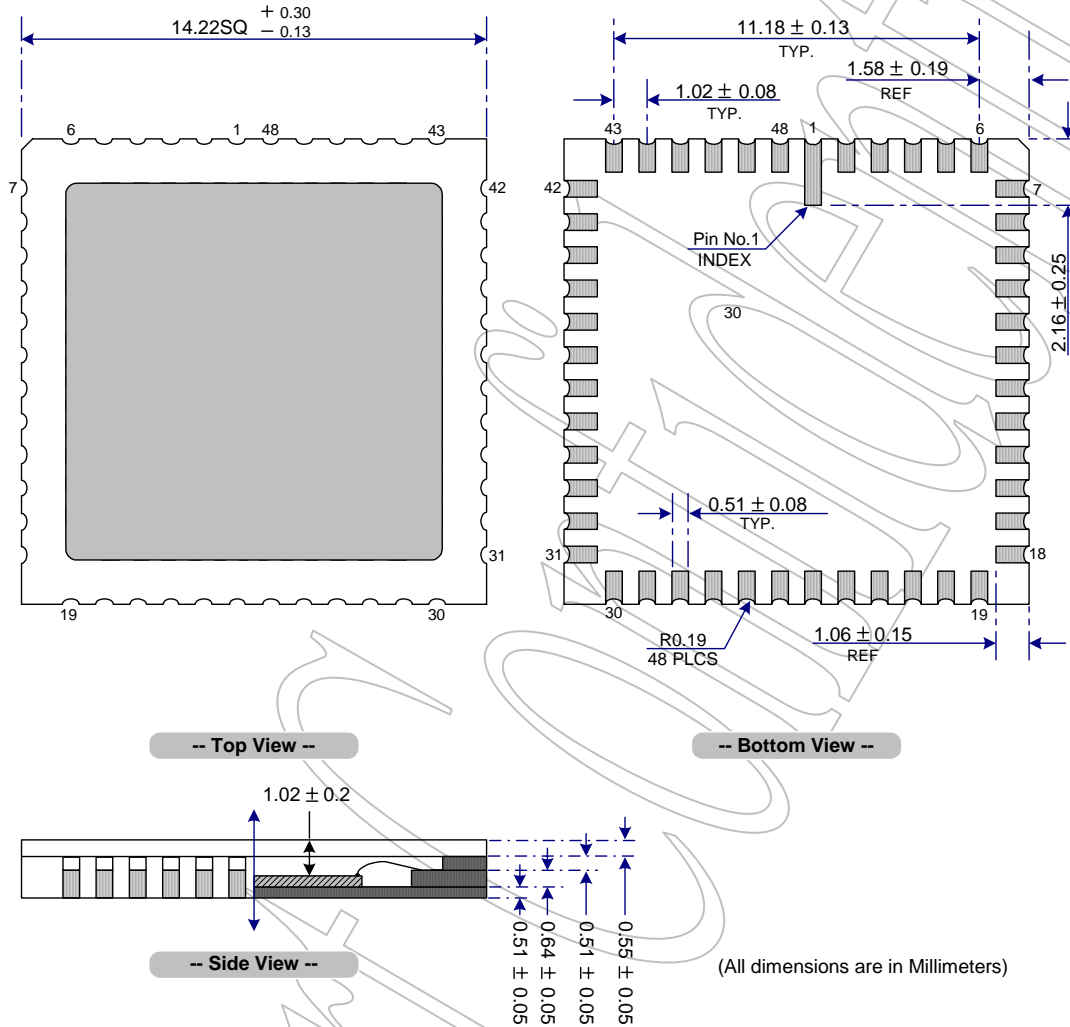
| Parameter | Symbol | Typ. | Unit | Note |
|-------------------------------|-------------------|------|-----------|------|
| Photo response non-uniformity | PRNU | 1.40 | % | |
| Saturation output voltage | Sat. | 696 | Level | |
| Dark output voltage | V _{dark} | 17 | Level/sec | |
| Dark signal non-uniformity | DSNU | 1.87 | Level | |
| Fixed Pattern Noise | FPN | 7.05 | Level | |
| Signal to Noise ratio | SNR | 42 | dB | |
| Dynamic range | DR | 48 | dB | |

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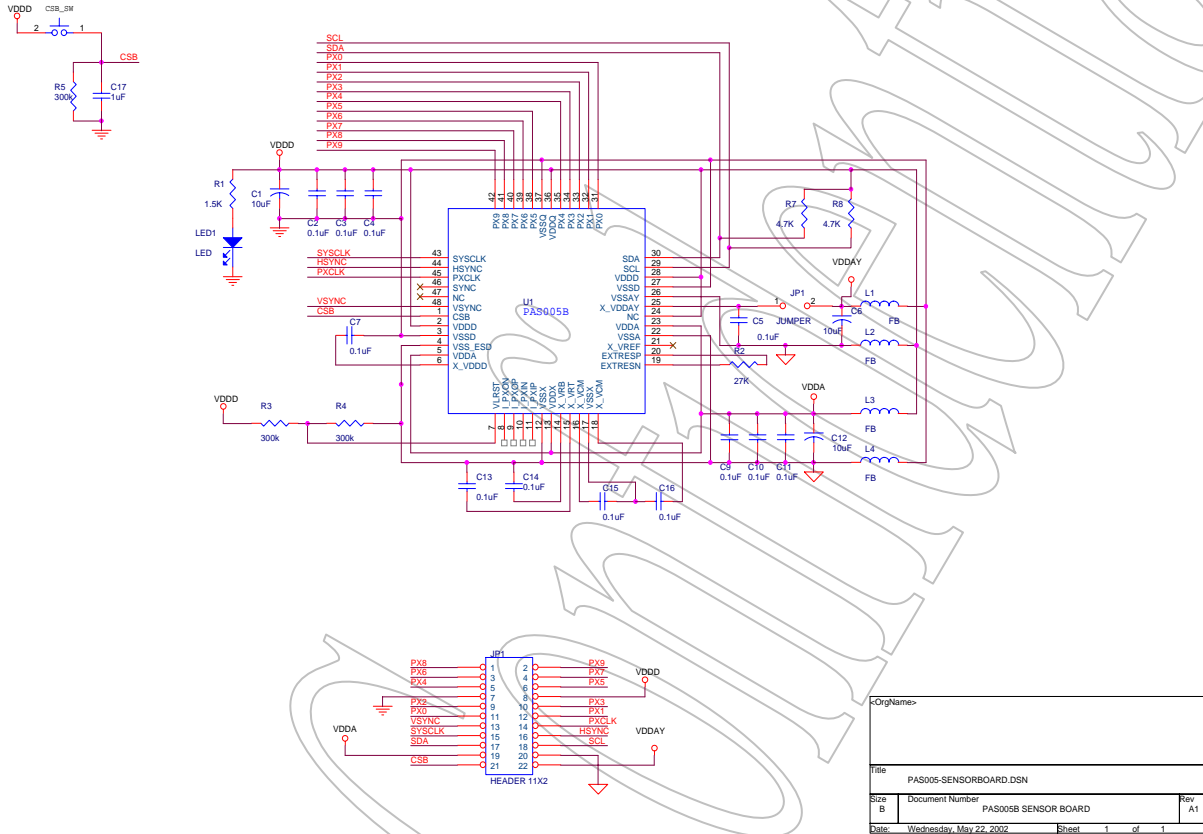
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7.2. Package Outline



8. Referencing application circuit



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