

# P4C163/P4C163L ULTRA HIGH SPEED 8K x 9 STATIC CMOS RAMS

## FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
  - 25/35ns (Commercial)
  - 25/35/45ns (Military)
- Low Power Operation (Commercial/Military)
- Output Enable and Dual Chip Enable Control Functions
- Single 5V±10% Power Supply
- Data Retention with 2.0V Supply, 10 µA Typical Current (P4C163L Military)
- Common I/O
- Fully TTL Compatible Inputs and Outputs
- Standard Pinout (JEDEC Approved)
  - 28-Pin 300 mil DIP, SOJ
  - 28-Pin 350 x 550 mil LCC
  - 28-Pin CERPACK

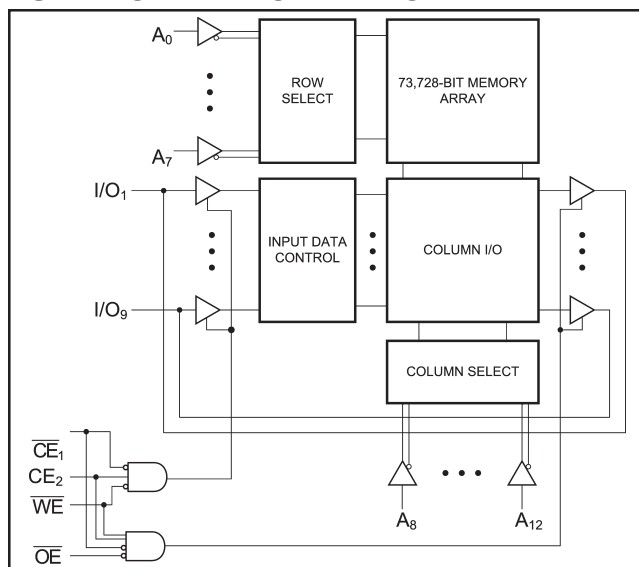
## DESCRIPTION

The P4C163 and P4C163L are 73,728-bit ultra high-speed static RAMs organized as 8K x 9. The CMOS memories require no clocks or refreshing and have equal access and cycle times. Inputs are fully TTL-compatible. The RAMs operate from a single 5V±10% tolerance power supply. With battery backup, data integrity is maintained for supply voltages down to 2.0V. Current drain is 10 µA from a 2.0V supply.

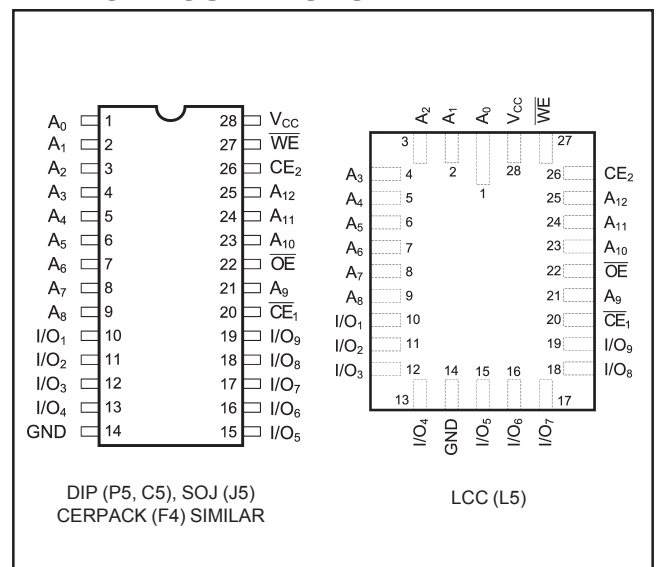
Access times as fast as 25 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is used to reduce power consumption in both active and standby modes.

The P4C163 and P4C163L are available in 28-pin 300 mil DIP and SOJ, 28-pin 350 x 550 mil LCC, and 28-pin CERPACK packages providing excellent board level densities.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATIONS



## MAXIMUM RATINGS<sup>(1)</sup>

| Symbol     | Parameter   | Value                  | Unit |
|------------|---|------------------------|------|
| $V_{CC}$   | Power Supply Pin with Respect to GND              | -0.5 to +7             | V    |
| $V_{TERM}$ | Terminal Voltage with Respect to GND (up to 7.0V) | -0.5 to $V_{CC} + 0.5$ | V    |
| $T_A$      | Operating Temperature                             | -55 to +125            | °C   |

| Symbol     | Parameter              | Value       | Unit |
|------------|------------------------|-------------|------|
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | °C   |
| $T_{STG}$  | Storage Temperature    | -65 to +150 | °C   |
| $P_T$      | Power Dissipation      | 1.0         | W    |
| $I_{OUT}$  | DC Output Current      | 50          | mA   |

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Grade <sup>(2)</sup> | Ambient Temperature | GND | $V_{CC}$   |
|----------------------|---------------------|-----|------------|
| Military             | -55 to +125°C       | 0V  | 5.0V ± 10% |

| Grade <sup>(2)</sup> | Ambient Temperature | GND | $V_{CC}$   |
|----------------------|---------------------|-----|------------|
| Commercial           | 0°C to +70°C        | 0V  | 5.0V ± 10% |

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage<sup>(2)</sup>

| Symbol    | Parameter                       | Test Conditions   | P4C163              |                | P4C163L             |                | Unit      |    |
|-----------|---------------------------------|---|---------------------|----------------|---------------------|----------------|-----------|----|
|           |                                 |   | Min                 | Max            | Min                 | Max            |           |    |
| $V_{IH}$  | Input High Voltage              |   | 2.2                 | $V_{CC} + 0.5$ | 2.2                 | $V_{CC} + 0.5$ | V         |    |
| $V_{IL}$  | Input Low Voltage               |   | -0.5 <sup>(3)</sup> | 0.8            | -0.5 <sup>(3)</sup> | 0.8            | V         |    |
| $V_{HC}$  | CMOS Input High Voltage         |   | $V_{CC} - 0.2$      | $V_{CC} + 0.5$ | $V_{CC} - 0.2$      | $V_{CC} + 0.5$ | V         |    |
| $V_{LC}$  | CMOS Input Low Voltage          |   | -0.5 <sup>(3)</sup> | 0.2            | -0.5 <sup>(3)</sup> | 0.2            | V         |    |
| $V_{CD}$  | Input Clamp Diode Voltage       | $V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$                                 |                     | -1.2           |                     | -1.2           | V         |    |
| $V_{OL}$  | Output Low Voltage (TTL Load)   | $I_{OL} = +8 \text{ mA}, V_{CC} = \text{Min.}$                                  |                     | 0.4            |                     | 0.4            | V         |    |
| $V_{OLC}$ | Output Low Voltage (CMOS Load)  | $I_{OLC} = +100 \mu\text{A}, V_{CC} = \text{Min.}$                              |                     | 0.2            |                     | 0.2            | V         |    |
| $V_{OH}$  | Output High Voltage (TTL Load)  | $I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min.}$                                  | 2.4                 |                | 2.4                 |                | V         |    |
| $V_{OHC}$ | Output High Voltage (CMOS Load) | $I_{OHC} = -100 \mu\text{A}, V_{CC} = \text{Min.}$                              | $V_{CC} - 0.2$      |                | $V_{CC} - 0.2$      |                | V         |    |
| $I_{LI}$  | Input Leakage Current           | $V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$                          | Mil.<br>Com'l.      | -10<br>-5      | +10<br>+5           | -5<br>N/A      | +5<br>N/A | μA |
| $I_{LO}$  | Output Leakage Current          | $V_{CC} = \text{Max.}, \overline{CE} = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$ | Mil.<br>Com'l.      | -10<br>-5      | +10<br>+5           | -5<br>N/A      | +5<br>N/A | μA |

## CAPACITANCES<sup>(4)</sup>

( $V_{CC} = 5.0\text{V}, T_A = 25^\circ\text{C}, f = 1.0\text{MHz}$ )

| Symbol   | Parameter         | Conditions           | Typ. | Unit |
|----------|-------------------|----------------------|------|------|
| $C_{IN}$ | Input Capacitance | $V_{IN} = 0\text{V}$ | 5    | pF   |

| Symbol    | Parameter          | Conditions            | Typ. | Unit |
|-----------|--------------------|-----------------------|------|------|
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0\text{V}$ | 7    | pF   |

### Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.

2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.  
 3. Transient inputs with  $V_{IL}$  and  $I_{IL}$  not more negative than -3.0V and -100mA, respectively, are permissible for pulse widths up to 20 ns.  
 4. This parameter is sampled and not 100% tested.

## POWER DISSIPATION CHARACTERISTICS

Over recommended operating temperature and supply voltage<sup>(2)</sup>

| Symbol    | Parameter  | Test Conditions   | P4C163         |        | P4C163L    |        | Unit       |    |
|-----------|--|---|----------------|--------|------------|--------|------------|----|
|           |  |   | Min            | Max    | Min        | Max    |            |    |
| $I_{CC}$  | Dynamic Operating Current – 25                   | $V_{CC} = \text{Max.}, f = \text{Max.},$<br>Outputs Open  | Mil.<br>Com'l. | —<br>— | 145<br>125 | —<br>— | 145<br>N/A | mA |
| $I_{CC}$  | Dynamic Operating Current – 35, 45               | $V_{CC} = \text{Max.}, f = \text{Max.},$<br>Outputs Open  | Mil.<br>Com'l. | —<br>— | 120<br>95  | —<br>— | 120<br>N/A | mA |
| $I_{SB}$  | Standby Power Supply Current (TTL Input Levels)  | $\overline{CE}_1 \geq V_{IH}$ or<br>$CE_2 \leq V_{IL}, V_{CC} = \text{Max.},$<br>$f = \text{Max.},$ Outputs Open  | Mil.<br>Com'l. | —<br>— | 40<br>35   | —<br>— | 40<br>N/A  | mA |
| $I_{SB1}$ | Standby Power Supply Current (CMOS Input Levels) | $\overline{CE}_1 \geq V_{HC}$ or<br>$CE_2 \leq V_{LC}, V_{CC} = \text{Max.},$<br>$f = 0,$ Outputs Open,<br>$V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ | Mil.<br>Com'l. | —<br>— | 20<br>18   | —<br>— | 1<br>N/A   | mA |

n/a = Not Applicable

## DATA RETENTION CHARACTERISTICS (P4C163L, Military Temperature Only)

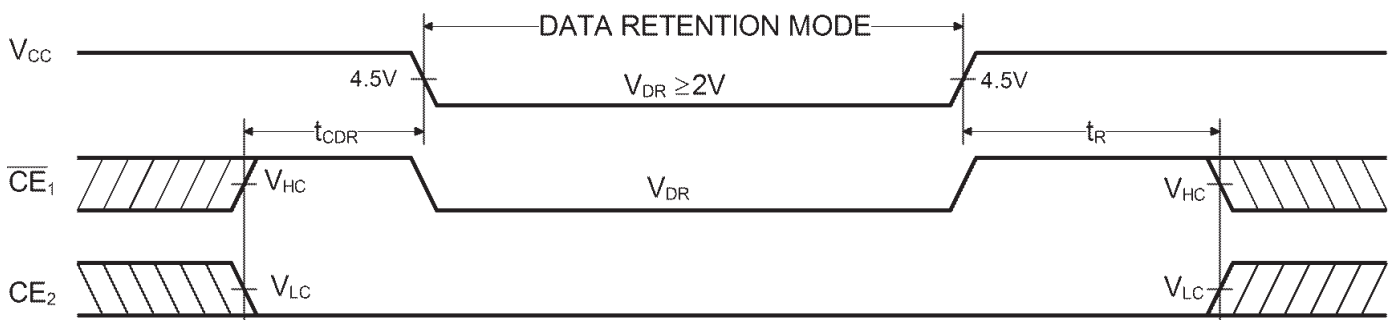
| Symbol        | Parameter                            | Test Condition  | Min           | Typ.*<br>$V_{CC} =$ |      | Max<br>$V_{CC} =$ |      | Unit    |
|---------------|--------------------------------------|---|---------------|---------------------|------|-------------------|------|---------|
|               |                                      |   |               | 2.0V                | 3.0V | 2.0V              | 3.0V |         |
| $V_{DR}$      | $V_{CC}$ for Data Retention          |   | 2.0           |                     |      |                   |      | V       |
| $I_{CCDR}$    | Data Retention Current               | $\overline{CE}_1 \geq V_{CC} - 0.2V$ or<br>$CE_2 \leq 0.2V, V_{IN} \geq V_{CC} - 0.2V$<br>or $V_{IN} \leq 0.2V$ |               | 10                  | 15   | 200               | 300  | $\mu A$ |
| $t_{CDR}$     | Chip Deselect to Data Retention Time |   | 0             |                     |      |                   |      | ns      |
| $t_R^\dagger$ | Operation Recovery Time              |   | $t_{RC}^{\S}$ |                     |      |                   |      | ns      |

\* $T_A = +25^\circ C$

$t_{RC}^{\S}$  = Read Cycle Time

$\dagger$ This parameter is guaranteed but not tested.

## DATA RETENTION WAVEFORM

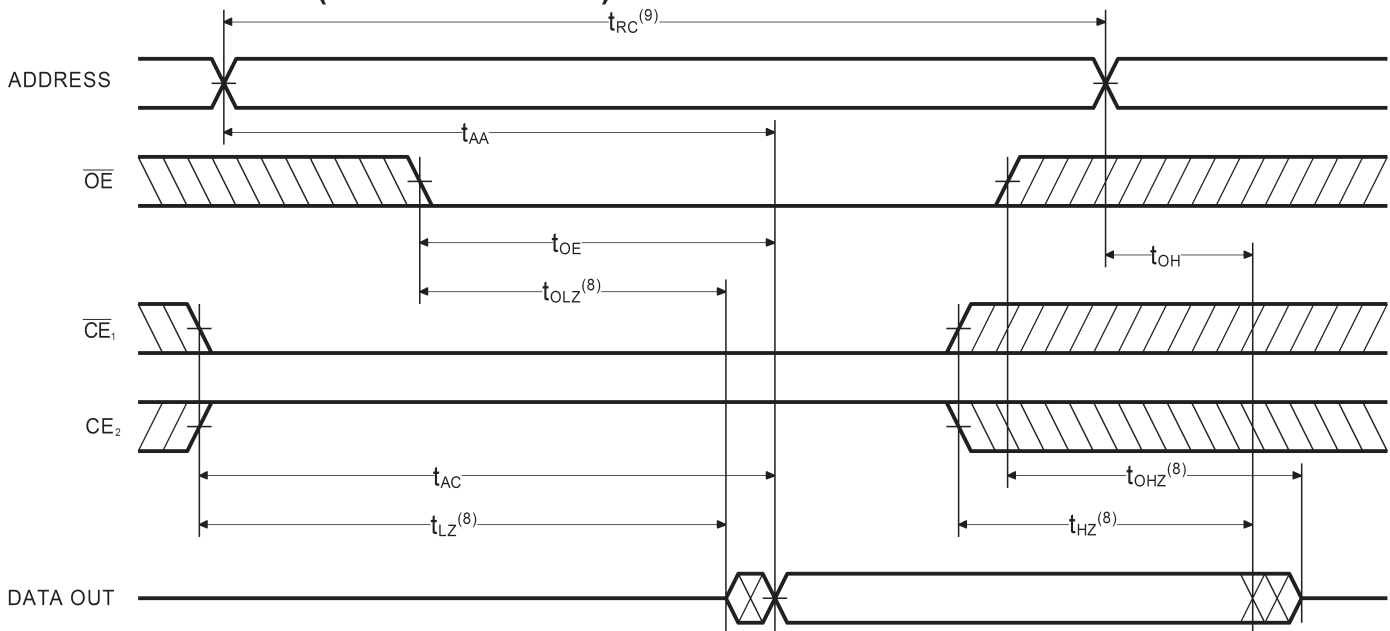


## AC ELECTRICAL CHARACTERISTICS—READ CYCLE

( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges)<sup>(2)</sup>

| Symbol    | Parameter                        | -25 |     | -35 |     | -45 |     | Unit |
|-----------|----------------------------------|-----|-----|-----|-----|-----|-----|------|
|           |                                  | Min | Max | Min | Max | Min | Max |      |
| $t_{RC}$  | Read Cycle Time                  | 25  |     | 35  |     | 45  |     | ns   |
| $t_{AA}$  | Address Access Time              |     | 25  |     | 35  |     | 45  | ns   |
| $t_{AC}$  | Chip Enable Access Time          |     | 25  |     | 35  |     | 45  | ns   |
| $t_{OH}$  | Output Hold from Address Change  | 3   |     | 3   |     | 3   |     | ns   |
| $t_{LZ}$  | Chip Enable to Output in Low Z   | 3   |     | 3   |     | 3   |     | ns   |
| $t_{HZ}$  | Chip Disable to Output in High Z |     | 10  |     | 15  |     | 20  | ns   |
| $t_{OE}$  | Output Enable Low to Data Valid  |     | 13  |     | 18  |     | 20  | ns   |
| $t_{OLZ}$ | Output Enable Low to Low Z       | 3   |     | 3   |     | 3   |     | ns   |
| $t_{OHZ}$ | Output Enable High to High Z     |     | 12  |     | 15  |     | 20  | ns   |
| $t_{PU}$  | Chip Enable to Power Up Time     | 0   |     | 0   |     | 0   |     | ns   |
| $t_{PD}$  | Chip Disable to Power Down Time  |     | 20  |     | 20  |     | 25  | ns   |

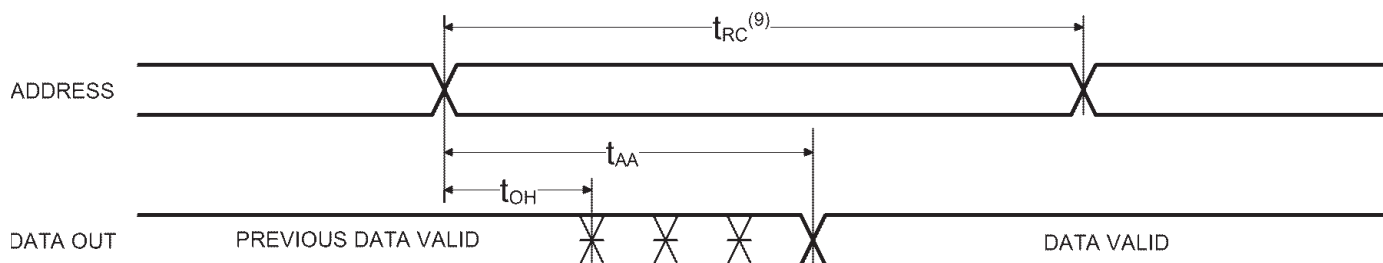
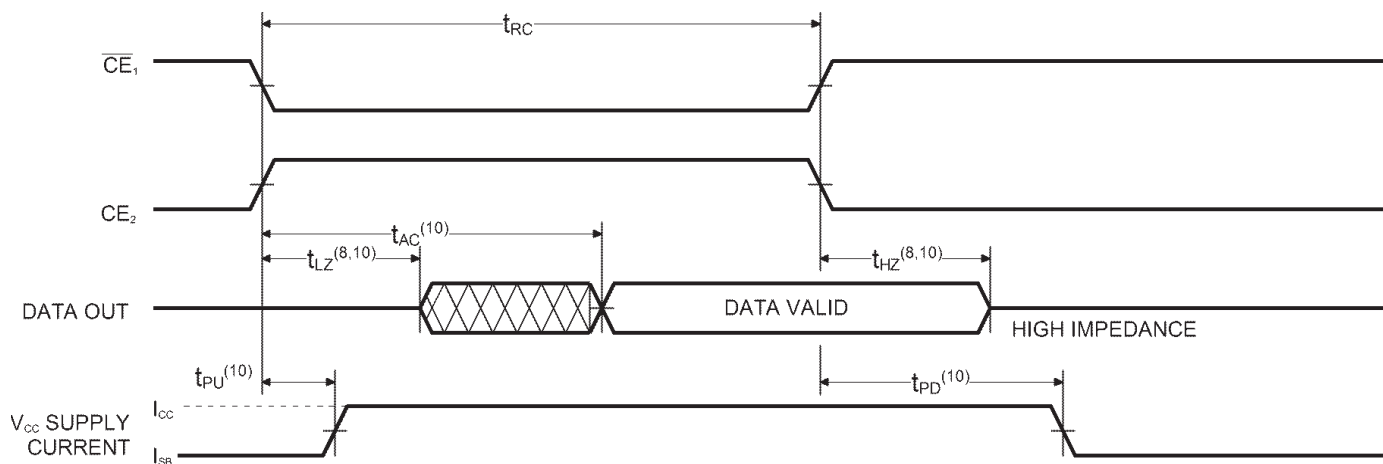
### READ CYCLE NO. 1 ( $\overline{OE}$ CONTROLLED)<sup>(5)</sup>



**Notes:**

- 5.  $\overline{WE}$  is HIGH for READ cycle.
- 6.  $\overline{CE}_1$  is LOW,  $CE_2$  is HIGH and  $\overline{OE}$  is LOW for READ cycle.
- 7. ADDRESS must be valid prior to, or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

- 8. Transition is measured  $\pm 200mV$  from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.

**READ CYCLE NO. 2 (ADDRESS CONTROLLED)<sup>(5,6)</sup>****READ CYCLE NO. 3 ( $\overline{CE}_1$ ,  $CE_2$  CONTROLLED)<sup>(5,7,10)</sup>****Notes:**

9. READ Cycle Time is measured from the last valid address to the first transitioning address.

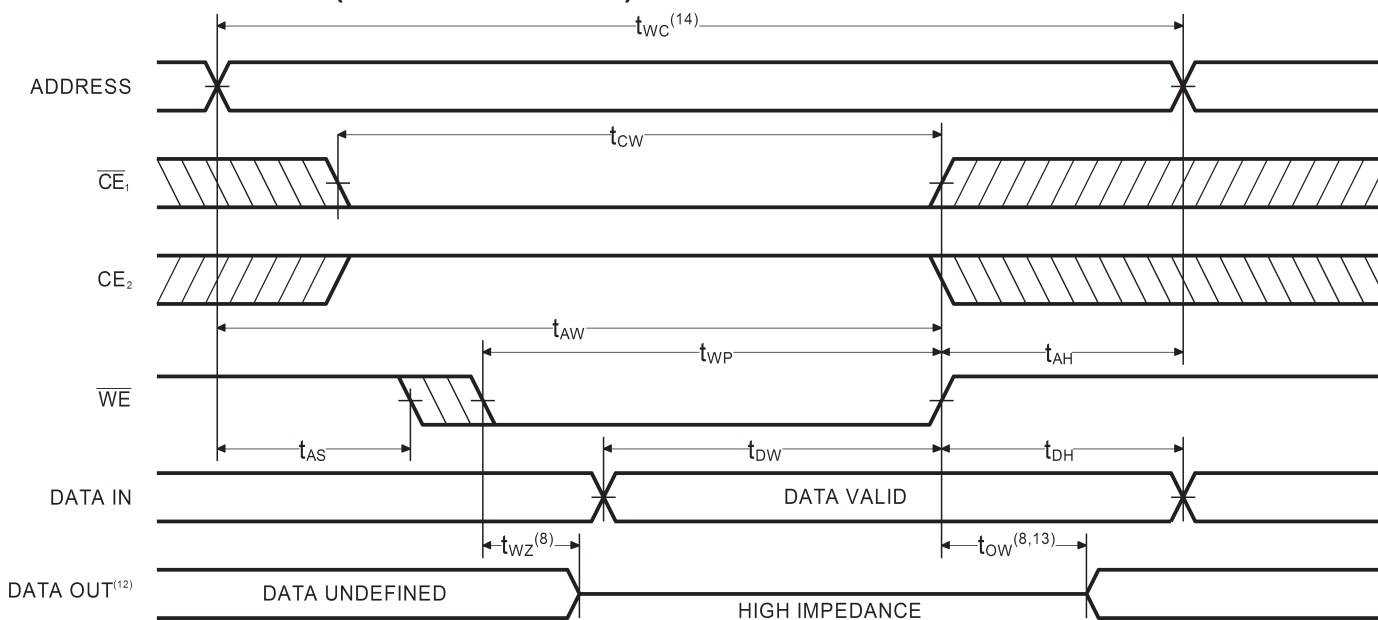
10. Transitions caused by a chip enable control have similar delays irrespective of whether  $\overline{CE}_1$  or  $CE_2$  causes them.

## AC CHARACTERISTICS—WRITE CYCLE

( $V_{CC} = 5V \pm 10\%$ , All Temperature Ranges)<sup>(2)</sup>

| Symbol   | Parameter                           | -25 |     | -35 |     | -45 |     | Unit |
|----------|-------------------------------------|-----|-----|-----|-----|-----|-----|------|
|          |                                     | Min | Max | Min | Max | Min | Max |      |
| $t_{WC}$ | Write Cycle Time                    | 25  |     | 35  |     | 45  |     | ns   |
| $t_{CW}$ | Chip Enable<br>Time to End of Write | 18  |     | 25  |     | 33  |     | ns   |
| $t_{AW}$ | Address Valid to<br>End of Write    | 18  |     | 25  |     | 33  |     | ns   |
| $t_{AS}$ | Address Set-up Time                 | 0   |     | 0   |     | 0   |     | ns   |
| $t_{WP}$ | Write Pulse Width                   | 18  |     | 20  |     | 25  |     | ns   |
| $t_{AH}$ | Address Hold Time                   | 0   |     | 0   |     | 0   |     | ns   |
| $t_{DW}$ | Data Valid to End<br>of Write       | 13  |     | 15  |     | 20  |     | ns   |
| $t_{DH}$ | Data Hold Time                      | 0   |     | 0   |     | 0   |     | ns   |
| $t_{WZ}$ | Write Enable to<br>Output in High Z |     | 10  |     | 14  |     | 18  | ns   |
| $t_{OW}$ | Output Active<br>from End of Write  | 3   |     | 5   |     | 5   |     | ns   |

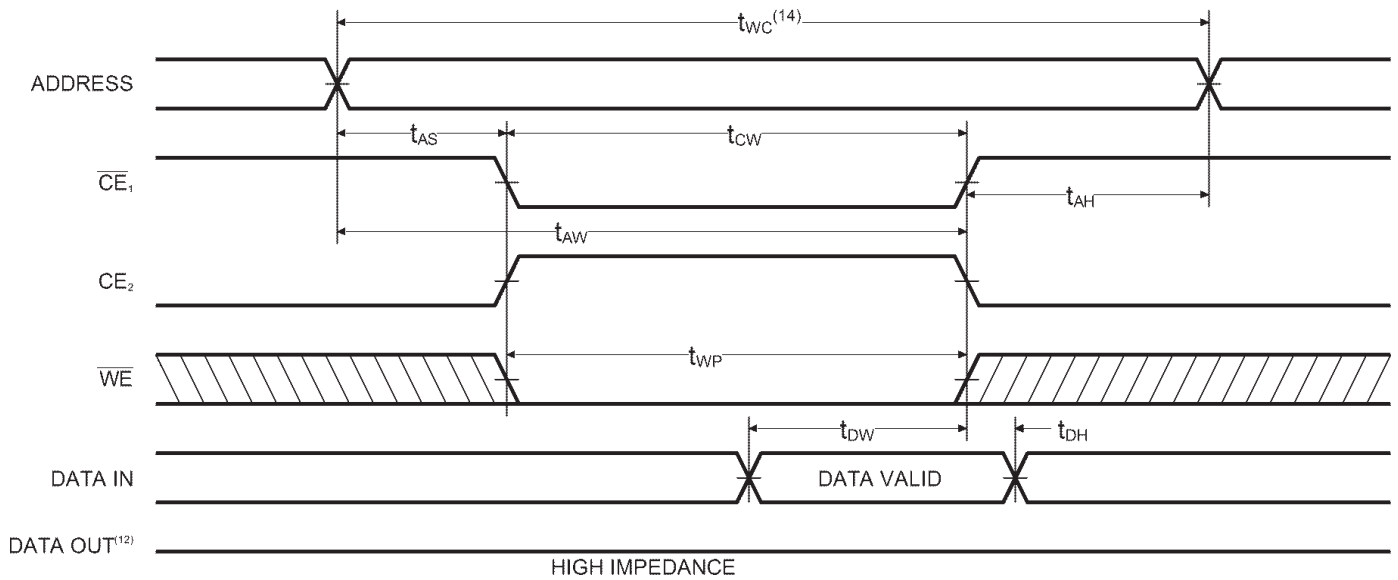
### WRITE CYCLE NO. 1 ( $\overline{WE}$ CONTROLLED)<sup>(11)</sup>



**Notes:**

11.  $\overline{CE}_1$  and  $\overline{WE}$  must be LOW, and  $\overline{CE}_2$  HIGH for WRITE cycle.
12.  $\overline{OE}$  is LOW for this WRITE cycle to show  $t_{WZ}$  and  $t_{OW}$ .
13. If  $\overline{CE}_1$  goes HIGH, or  $\overline{CE}_2$  goes LOW, simultaneously with  $\overline{WE}$  HIGH, the output remains in a low impedance state.
14. Write Cycle Time is measured from the last valid address to the first transitioning address.

**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CE}$  CONTROLLED)<sup>(11)</sup>**



**AC TEST CONDITIONS**

|                               |                     |
|-------------------------------|---------------------|
| Input Pulse Levels            | GND to 3.0V         |
| Input Rise and Fall Times     | 3ns                 |
| Input Timing Reference Level  | 1.5V                |
| Output Timing Reference Level | 1.5V                |
| Output Load                   | See Figures 1 and 2 |

**TRUTH TABLE**

| Mode               | $\overline{CE}_1$ | $CE_2$ | $\overline{OE}$ | $\overline{WE}$ | I/O       | Power   |
|--------------------|-------------------|--------|-----------------|-----------------|-----------|---------|
| Standby            | H                 | X      | X               | X               | High Z    | Standby |
| Standby            | X                 | L      | X               | X               | High Z    | Standby |
| $D_{OUT}$ Disabled | L                 | H      | H               | H               | High Z    | Active  |
| Read               | L                 | H      | L               | H               | $D_{OUT}$ | Active  |
| Write              | L                 | H      | X               | L               | $D_{IN}$  | Active  |

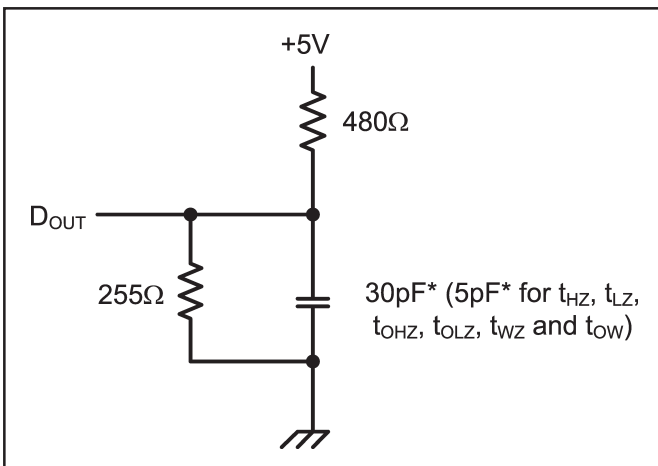


Figure 1. Output Load

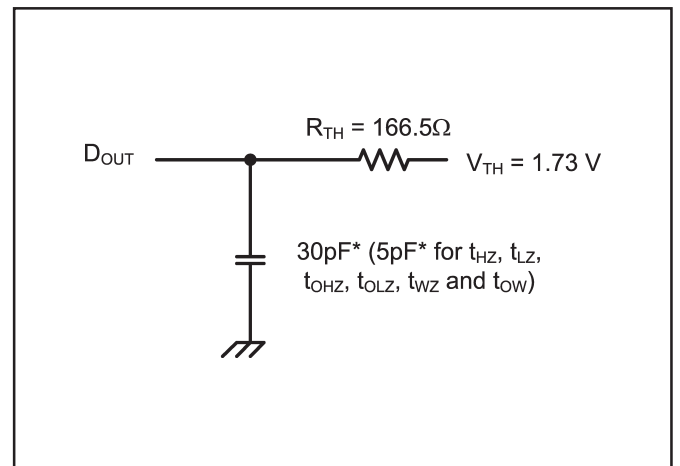


Figure 2. Thevenin Equivalent

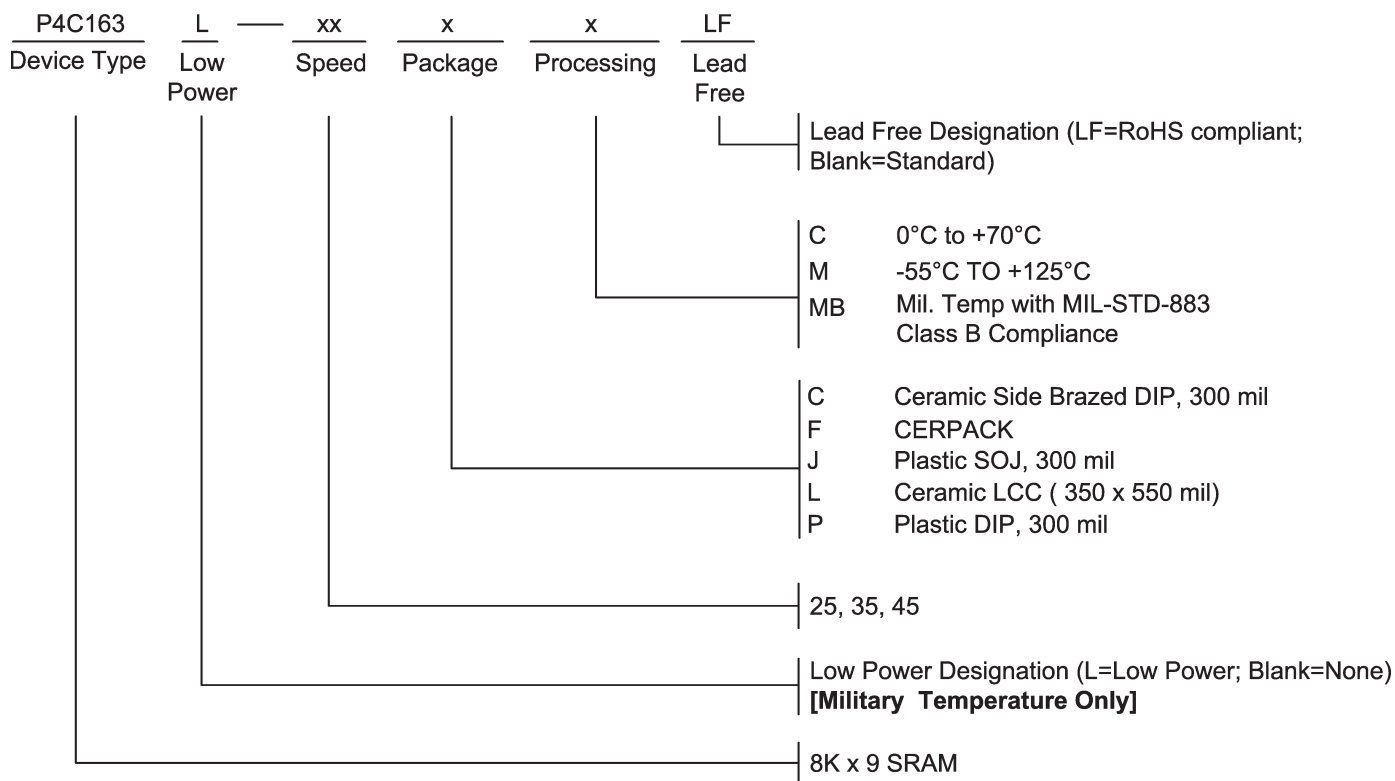
\* including scope and test fixture.

**Note:**

Because of the ultra-high speed of the P4C163/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the  $V_{CC}$  and ground planes directly up to the contactor fingers. A 0.01  $\mu$ F high frequency

capacitor is also required between  $V_{CC}$  and ground. To avoid signal reflections, proper termination must be used; for example, a 50 $\Omega$  test environment should be terminated into a 50 $\Omega$  load with 1.73V (Thevenin Voltage) at the comparator input, and a 116 $\Omega$  resistor must be used in series with  $D_{OUT}$  to match 166 $\Omega$  (Thevenin Resistance).

## ORDERING INFORMATION



## SELECTION GUIDE

The P4C163/L is available in the following temperature, speed and package options. The P4C163L is only available over the military temperature range.

| Temperature Range    | Package         | Speed  |        |        |
|----------------------|-----------------|--------|--------|--------|
|                      |                 | 25     | 35     | 45     |
| Commercial           | Plastic DIP     | -25PC  | -35PC  | N/A    |
|                      | Plastic SOJ     | -25JC  | -35JC  | N/A    |
| Military Temperature | Side Brazed DIP | -25CM  | -35CM  | -45CM  |
|                      | LCC             | -25LM  | -35LM  | -45LM  |
|                      | CERPACK         | -25FM  | -35FM  | -45FM  |
| Military Processed*  | Side Brazed DIP | -25CMB | -35CMB | -45CMB |
|                      | LCC             | -25LMB | -35LMB | -45LMB |
|                      | CERPACK         | -25FMB | -35FMB | -45FMB |

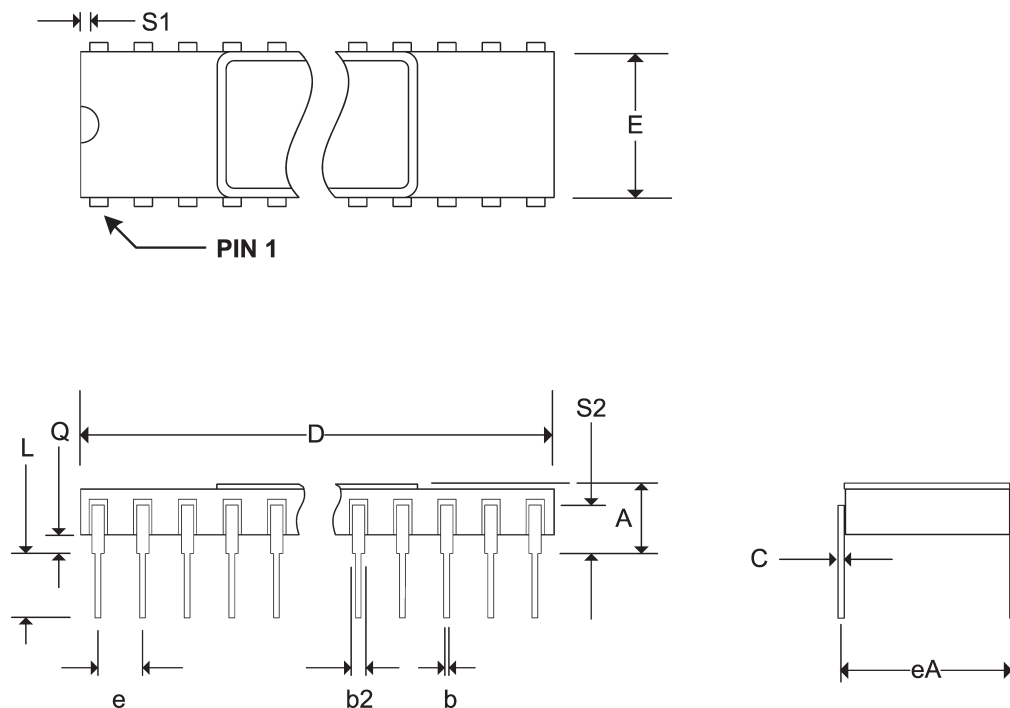
\* Military temperature range with MIL-STD-883, Class B processing.

N/A = Not available



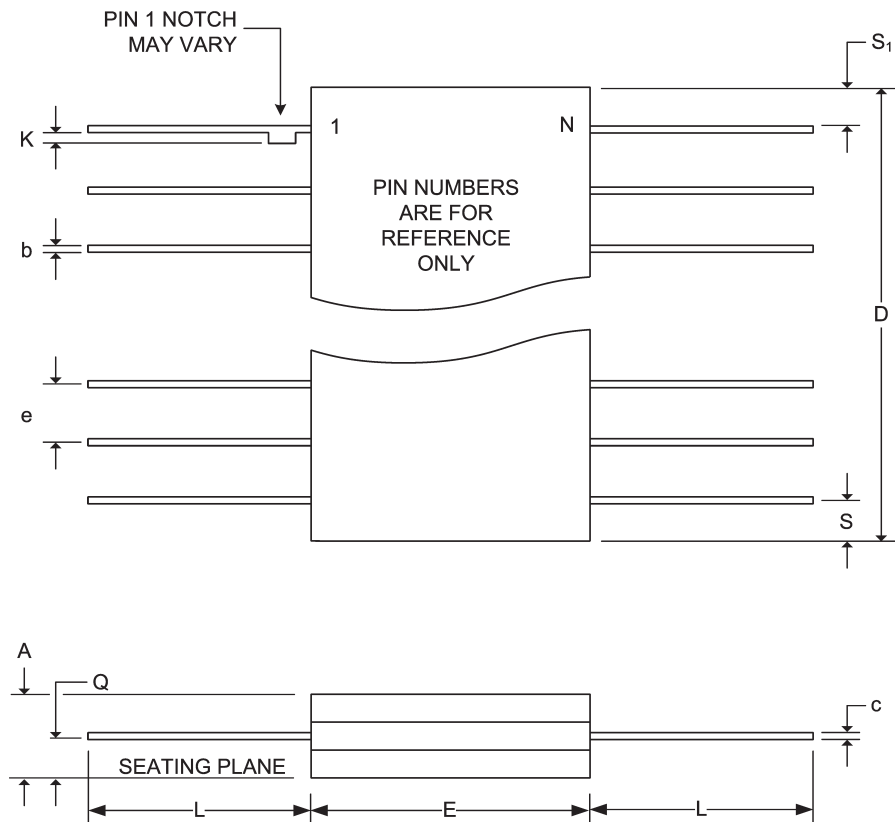
|        |              |            |
|--------|--------------|------------|
| Pkg #  | <b>C5</b>    |            |
| # Pins | 28 (300 mil) |            |
| Symbol | <b>Min</b>   | <b>Max</b> |
| A      | -            | 0.225      |
| b      | 0.014        | 0.026      |
| b2     | 0.045        | 0.065      |
| C      | 0.008        | 0.018      |
| D      | -            | 1.485      |
| E      | 0.240        | 0.310      |
| eA     | 0.300 BSC    |            |
| e      | 0.100 BSC    |            |
| L      | 0.125        | 0.200      |
| Q      | 0.015        | 0.070      |
| S1     | 0.005        | -          |
| S2     | 0.005        | -          |

**SIDE BRAZED DUAL IN-LINE PACKAGE**



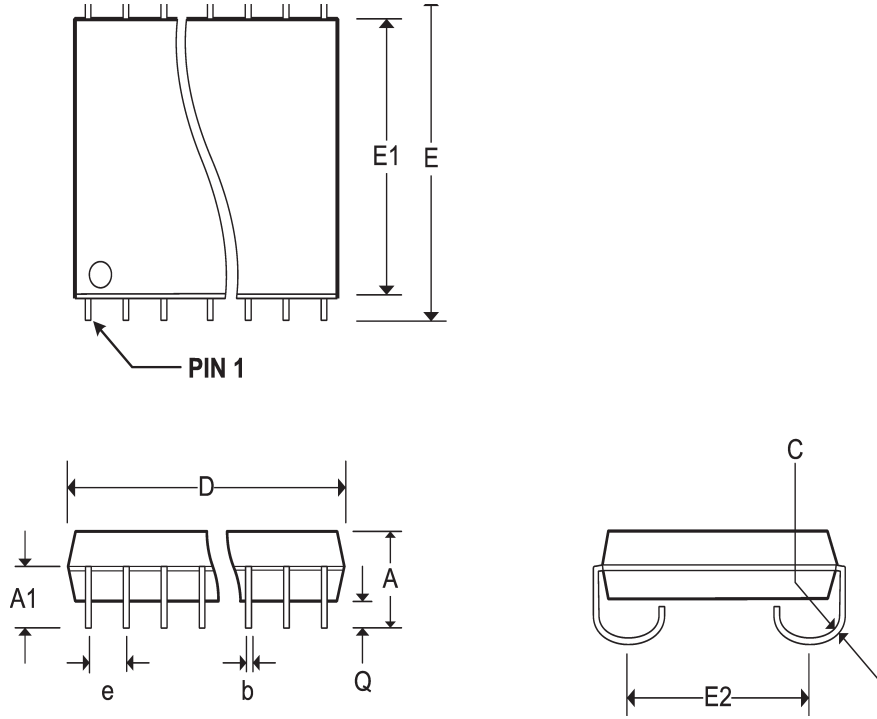
|        |            |            |
|--------|------------|------------|
| Pkg #  | <b>F4</b>  |            |
| # Pins | 28         |            |
| Symbol | <b>Min</b> | <b>Max</b> |
| A      | 0.060      | 0.090      |
| b      | 0.015      | 0.022      |
| c      | 0.004      | 0.009      |
| D      | -          | 0.730      |
| E      | 0.330      | 0.380      |
| e      | 0.050 BSC  |            |
| k      | 0.005      | 0.018      |
| L      | 0.250      | 0.370      |
| Q      | 0.026      | 0.045      |
| S      | -          | 0.085      |
| S1     | 0.005      | -          |

**CERPACK CERAMIC FLAT PACKAGE**



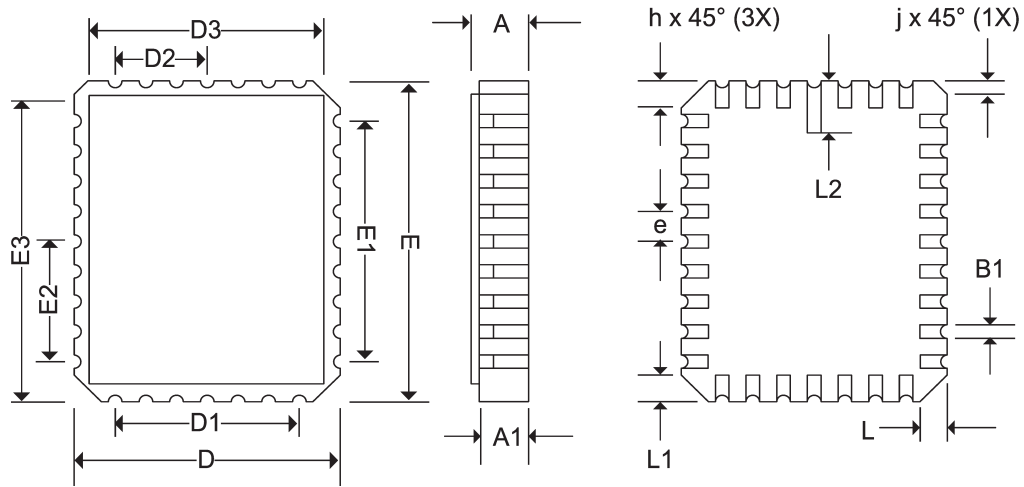
| Pkg #  | J5           |       |
|--------|--------------|-------|
| # Pins | 28 (300 mil) |       |
| Symbol | Min          | Max   |
| A      | 0.120        | 0.148 |
| A1     | 0.078        | -     |
| b      | 0.014        | 0.020 |
| C      | 0.007        | 0.011 |
| D      | 0.700        | 0.730 |
| e      | 0.050 BSC    |       |
| E      | 0.335 BSC    |       |
| E1     | 0.292        | 0.300 |
| E2     | 0.267 BSC    |       |
| Q      | 0.025        | -     |

**SOJ SMALL OUTLINE IC PACKAGE**



| Pkg #  | L5        |       |
|--------|-----------|-------|
| # Pins | 28        |       |
| Symbol | Min       | Max   |
| A      | 0.060     | 0.075 |
| A1     | 0.050     | 0.065 |
| B1     | 0.022     | 0.028 |
| D      | 0.342     | 0.358 |
| D1     | 0.200 BSC |       |
| D2     | 0.100 BSC |       |
| D3     | -         | 0.358 |
| E      | 0.540     | 0.560 |
| E1     | 0.400 BSC |       |
| E2     | 0.200 BSC |       |
| E3     | -         | 0.558 |
| e      | 0.050 BSC |       |
| h      | 0.040 REF |       |
| j      | 0.020 REF |       |
| L      | 0.045     | 0.055 |
| L1     | 0.045     | 0.055 |
| L2     | 0.075     | 0.095 |
| ND     | 5         |       |
| NE     | 9         |       |

**RECTANGULAR LEADLESS CHIP CARRIER**



| Pkg #    | P5           |       |
|----------|--------------|-------|
| # Pins   | 28 (300 mil) |       |
| Symbol   | Min          | Max   |
| A        | -            | 0.210 |
| A1       | -            | -     |
| b        | 0.014        | 0.023 |
| b2       | 0.045        | 0.070 |
| C        | 0.008        | 0.014 |
| D        | 1.345        | 1.400 |
| E1       | 0.270        | 0.300 |
| E        | 0.300        | 0.380 |
| e        | 0.100 BSC    |       |
| eB       | -            | 0.430 |
| L        | 0.115        | 0.150 |
| $\alpha$ | 0°           | 15°   |

PLASTIC DUAL IN-LINE PACKAGE

