

Preliminary Data

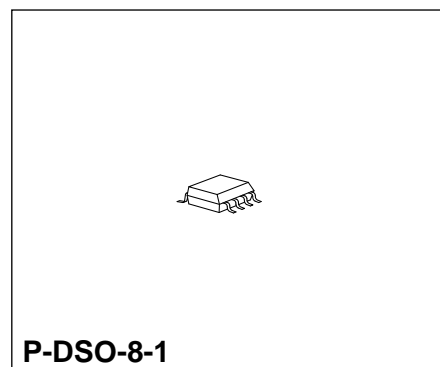
Bipolar IC

Features

- Few external components
- Low noise
- Low spurious signal content
- High conversion transconductance
- Very highly isolated RF, IF and LO ports
- Good suppression of input signals at output
- Wide range of supply voltage

Applications

- Cellular radio mixer
- Cordless telephone mixer
- UHF transceivers
- RF data links
- HF/VHF/UHF frequency conversion



Type	Version	Ordering Code	Package
PMB 2330	V1.1	Q67000-A6045	P-DSO-8-1 (SMD)
PMB 2330T	V1.2	Q67000-A6103	P-DSO-8-1 (SMD)

The PMB 2330 is a low power, monolithic, double balanced mixer similar to S 042 P and TBB 042 G for frequencies up to 2 GHz.

Circuit Description

The pins RF (7) and $\overline{\text{RF}}$ (8) are low resistance inputs of the base coupled difference stage.

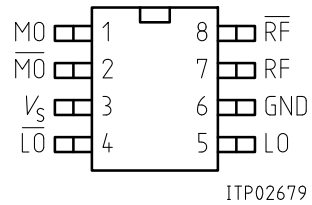
The resistor of at least 200 Ω may be connected between pins 7 and 6 (ground) and between 8 and 6 to increase the currents (max. 4 mA per pin) and thus the conversion transductance.

The pins $\overline{\text{LO}}$ (4) and LO (5) are the local oscillator inputs of the mixer.

The connections to the mixer inputs may be symmetrical or asymmetrical coupled, capacitive or inductive coupled.

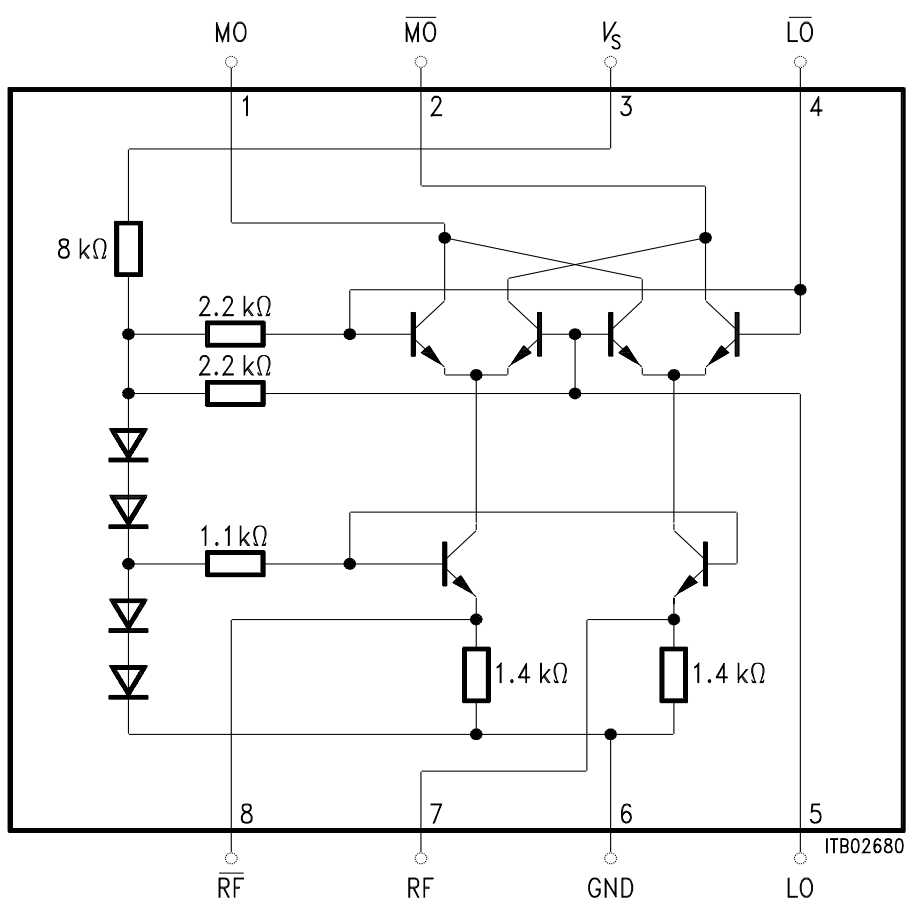
The mixer outputs MO (1) and $\overline{\text{MO}}$ (2) are high impedance open-collector outputs for frequencies up to 2 GHz.

Pin Configuration (top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	MO	Mixer output
2	\overline{MO}	Mixer output
3	V_S	Supply voltage
4	\overline{LO}	Oscillator input
5	LO	Oscillator input
6	GND	Ground
7	RF	Mixer input
8	\overline{RF}	Mixer input



Block Diagram

Electrical Characteristics

Absolute Maximum Ratings

$T_A = -40$ to 85 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	typ.		
Supply voltage	V_S	0	8	V	
Mixer output	$V_{1,2}$	1	8	V	open collector
Oscillator input	$V_{4,5}$	0	2.5	V	
Mixer input	$V_{7,8}$	0.8	3.5	V	
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	-40	125	°C	
Thermal resistance	$R_{th SA}$		185	K/W	

All pins have no additional internal ESD protection circuitry

Operational Range

Within the operational range the IC operates as described in the circuit description.

Supply voltage	V_S	3	7	V	
Input frequency range	f_i	10	2000	MHz	
Ambient temperature in operation	T_A	-40	85	°C	

Characteristics

$V_S = 5\text{ V} \pm 10\%$; $T_A = 25\text{ }^\circ\text{C}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	$I_{MO} + I_{\overline{MO}} + I_{VS}$		1.6		mA	
Output current	$I_{MO} = I_{\overline{MO}}$		0.54		mA	
Output current difference	$ I_{MO} - I_{\overline{MO}} $			60	μA	
Break down voltage	$V_{MO, \overline{MO}}$		13		V	$I_{MO, \overline{MO}} = 8\text{ mA}$

Signal Input RF/ $\overline{\text{RF}}$

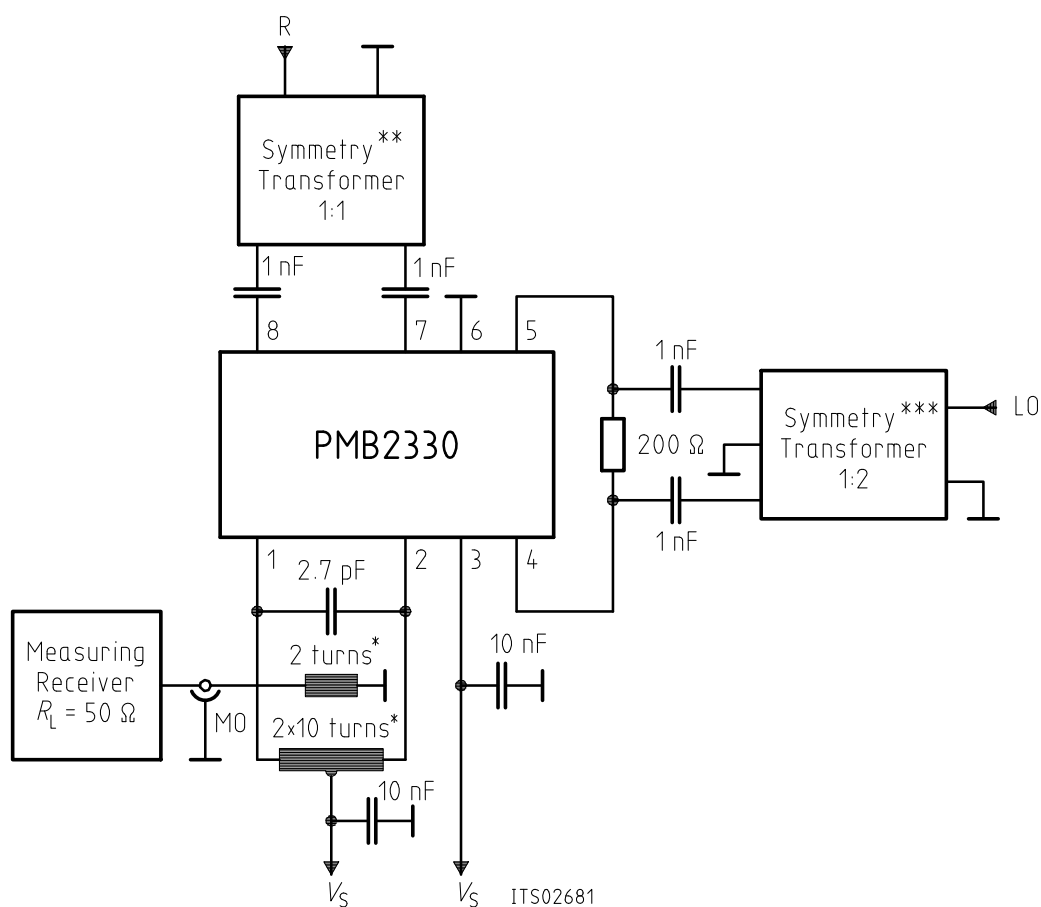
Input resistance	R_{RF}		100		Ω	
Input inductance	L_{RF}		10		nH	in series to R_{RF}
Input level	P_{RF}			0	dBm	
Input Intercept point	P_{IPI}		-5		dBm	referred to input
Input frequency	f_{RF}	0		2.0	GHz	
Noise figure						according to test circuit
$f_{RF} = 100\text{ MHz}, f_{LO} = 145\text{ MHz}$	N		6		dB	
$f_{RF} = 1\text{ GHz}, f_{LO} = 1.045\text{ GHz}$	N		8		dB	

Local Oscillator Input LO/ $\overline{\text{LO}}$

Input resistance	$R_{LO\text{ diff}}$ $R_{LO\text{ diff}}$		3.8 0.6		k Ω k Ω	$f_{LO} = 100\text{ MHz}$ $f_{LO} = 1\text{ GHz}$
Input capacitance	$C_{LO\text{ diff}}$		1.5		pF	parallel to $R_{LO\text{ diff}}$
Input level	P_{LO} P_{LO}	-10 -5		10 10	dBm dBm	$f_{LO} = 100\text{ MHz}$ $f_{LO} = 1\text{ GHz}$
Input frequency	f_{LO}			2.0	GHz	

Mixer Output MO/ $\overline{\text{MO}}$

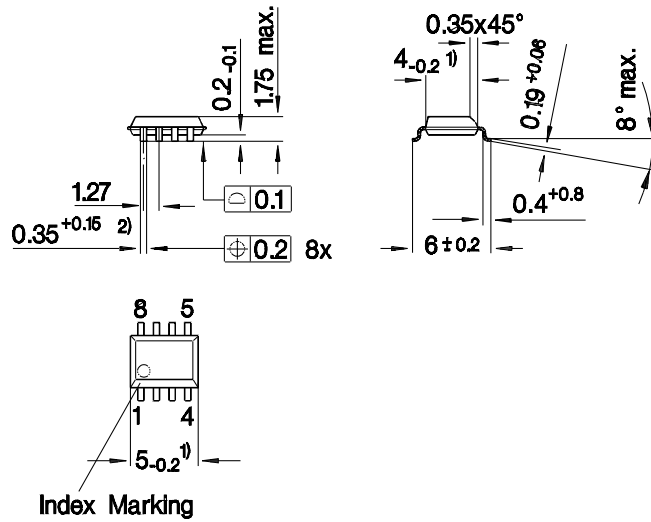
Output resistance	$R_{MO\text{ diff}}$ $R_{MO\text{ diff}}$		7.0 0.6		k Ω k Ω	$f_{MO} = 100\text{ MHz}$ $f_{MO} = 1\text{ GHz}$
Output capacitance	$C_{MO\text{ diff}}$		1.5		pF	parallel to $R_{MO\text{ diff}}$
Power gain						
$f_{RF} = 100\text{ MHz}, f_{LO} = 145\text{ MHz}$	V_P		10		dB	
$f_{RF} = 1\text{ GHz}, f_{LO} = 1.045\text{ GHz}$	V_P		10		dB	
Intermediate frequency	f_{IF}			2.0	GHz	



- * Kit Vogt 5171100002
Cul 0.08
- ** Balance to unbalance balun 1:1
00553100 Fa. NEOSID
- *** Balance to unbalance balun 1:2
00553110 Fa. NEOSID

Test Circuit

Plastic Package, P-DSO-8-1 (SMD)
 (Plastic Dual Small Outline)



- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion

GPS05121

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"

SMD = Surface Mounted Device

Dimensions in mm