

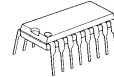
# DIGITAL TO ANALOG CONVERTER FOR STEREO AUDIO

## ■ GENERAL DESCRIPTION

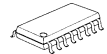
The **NJU8402** is a 16-bit delta-sigma Digital-to-Analog Converter for stereo audio. It consists of Serial Audio Data Interface, Digital Interpolation Filter,  $\Delta\Sigma$  Modulator, SC LPF, Buffer Amp, System Controller for status control. It operates on single +5V power supply. Furthermore, it accepts 16-bit input audio data length or 18-bit, and supports I<sup>2</sup>S serial data format and LSB justified.

Therefore, the **NJU8402** is suitable for CD, MD, DAT and other digital audio applications.

## ■ PACKAGE OUTLINE



NJU8402D

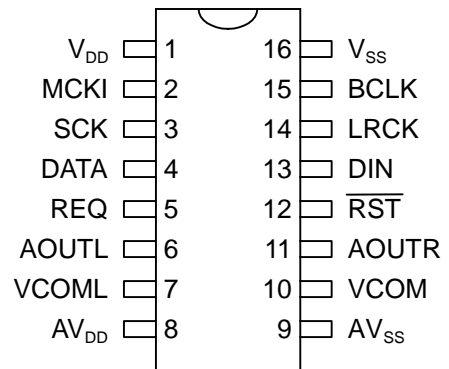


NJU8402M

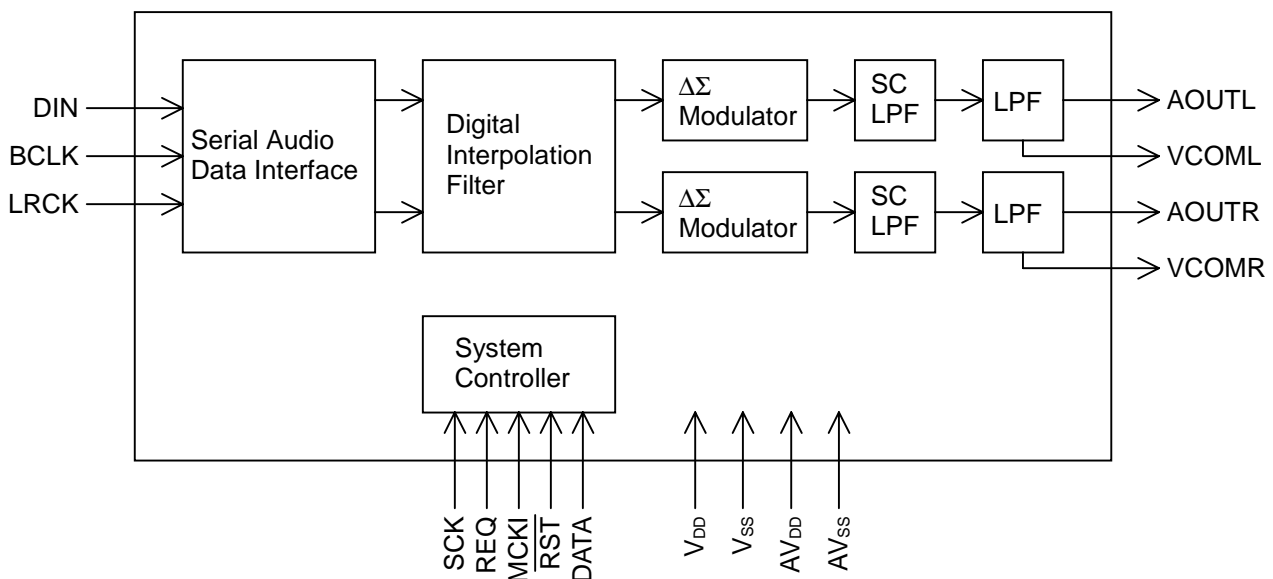
## ■ FEATURES

- $\Delta\Sigma$  type 1bit stereo DAC
- Sample Rate ( fs ) : 50kHz ( Maximum )
- Signal-to-Noise Ratio : 94dB
- Input Audio Data Length : 16bits or 18bits
- Single ended Analog Output
- Internal SC type Low Pass Filter
- Operating Voltage +5V  $\pm$ 5%
- Package Outline DIP16 / DMP16

## ■ PIN CONFIGURATION



## ■ BLOCK DIAGRAM



## ■ TERMINAL DESCRIPTION

| PIN No. | SYMBOL                  | INPUT /OUTPUT | FUNCTION   |
|---------|-------------------------|---------------|--|
| 1       | V <sub>DD</sub>         | —             | Digital Power Supply, +5V  |
| 16      | V <sub>SS</sub>         | —             | Digital GND, 0V  |
| 8       | AV <sub>DD</sub>        | —             | Analog Power Supply, +5V   |
| 9       | AV <sub>SS</sub>        | —             | Analog GND, 0V   |
| 2       | MCKI                    | I             | Master Clock Input Terminal<br>The input signal frequency is 256 times or 384 times of fs.   |
| 13      | DIN                     | I             | Serial Audio Data Input Terminal   |
| 14      | LRCK                    | I             | L/R Channel Clock Input Terminal<br>This clock must synchronize with MCKI.   |
| 15      | BCLK                    | I             | Audio Serial Data Clock Input Terminal<br>This clock must synchronize with MCKI.   |
| 3       | SCK                     | I             | Control Register Serial Data Sift Clock Input Terminal<br>Control register leads the control data synchronizing the rising edge of SCK signal. When the control register is not used, the state of SCK terminal has to keep level "H".   |
| 4       | DATA                    | I             | Control Register Serial Data Input Terminal<br>Input data sets various functions.<br>When the control register is not used, the state of DATA terminal has to keep level "H".  |
| 5       | REQ                     | I             | Control Register Serial Data Request Input Terminal<br>The control data are latched in the control register at the rising edge of REQ signal.<br>When the control register is not used, the state of REQ terminal has to keep level "H". |
| 12      | $\overline{\text{RST}}$ | I             | Reset<br>"L" level signal into reset terminal initializes the system.  |
| 7       | VCOML                   | —             | Left channel Analog Signal Common Terminal for Connecting Smooth Capacitor<br>A chemical capacitor should be connected between this terminal and AV <sub>SS</sub> for stabilizing.   |
| 10      | VCOMR                   | —             | Right Channel Analog Signal Common Terminal for Connecting Smooth Capacitor<br>A chemical capacitor should be connected between this terminal and AV <sub>SS</sub> for stabilizing.  |
| 6       | AOUTL                   | O             | L-Channel Analog Signal Output Terminal  |
| 11      | AOUTR                   | O             | R-Channel Analog Signal Output Terminal  |

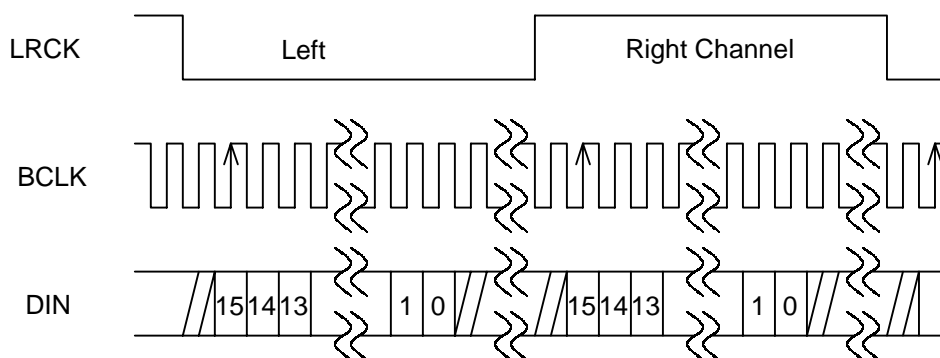
## ■ FUNCTION DESCRIPTION

### (1-1) Analog Audio Signal Output

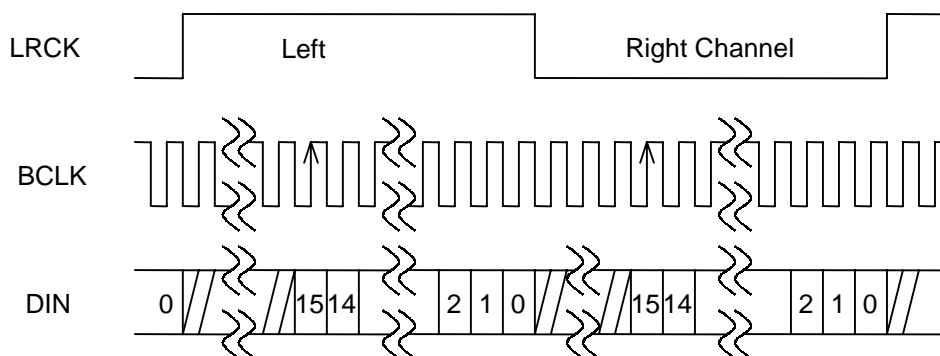
Analog signal output is biased in the chip and the maximum amplitude is  $0.56 \times AV_{DD}$ . The internal switched capacitor Low Pass Filter is so effective that the external Low Pass Filters are required only 2-pole LPF or 3-pole.

### (1-2) Serial Data Interface

DIN (Data Input), BCLK (Bit Clock) and LRCK (L/R Clock) are the serial data interface terminals. BCLK is the bit clock of audio data and IO data are leaded at raising edge of the BCLK. The signal into LRCK terminal represents the signal for distinguishing between Lch and Rch, and the signal for starting data. The frequency of LRCK is sampling rate of system ( $f_s$ ). The MCIK must be synchronized with LRCK and is 256 times or 384 of  $f_s$ . The serial data format is complement of 2, MSB-first and compatible with I<sup>2</sup>S serial data protocol or LSB justified. This serial data format is set by the control register.



I<sup>2</sup>S serial data format



LSB justified serial data format

### (1-3) System Clock

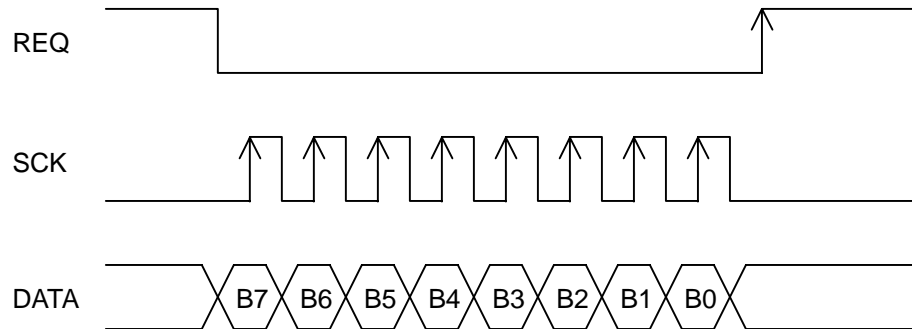
System Clock into the MCIK terminal must be 256 times or 384 times of  $f_s$  and synchronizing with LRCK. This frequency is set by the control register.

### (1-4) Reset

The external reset is the asynchronous reset. Reset is released at the falling edge at LRCK. Reset by command is synchronous which operates as same as the external reset function.

(1-5) Control Register

The Control Register controls **NJU8402** operation using the serial interface. The SCK terminal is the data shift clock, the REQ terminal is data request signal, the DATA terminal is the serial data input. The control data is loaded into the shift register at rising edge of SCK, then it is latched at the rising edge of REQ. The least 8-bit data, which order is MSB first, is valid for control.



CONTROL PORT TIMING CHART

• Serial Data Format

| B7 | B6 | B5 | B4 | B3 | B2   | B1   | B0   |
|----|----|----|----|----|------|------|------|
| 0  | 0  | 0  | 0  | *  | DIF1 | DIF0 | CLKR |
| 0  | 0  | 0  | 1  | *  | *    | *    | RST  |

(\*: Don't Care)

\*1 Don't input commands except this table.

|              |      | 0                | 1             | Default |
|--------------|------|------------------|---------------|---------|
| System Clock | CLKR | 256fs            | 384fs         | 0       |
| Data Length  | DIF0 | 16               | 18            | 0       |
| Format       | DIF1 | I <sup>2</sup> S | LSB Justified | 0       |
| Reset        | RST  | Normal           | Reset         | *2      |

\*2 The level becomes 0 after initial setting.

## ■ ABSOLUTE MAXIMUM RATING

( $V_{SS}=AV_{SS}=0V$ )

| PARAMETER             |                    | SYMBOL           | CONDITIONS                 | UNIT |
|-----------------------|--------------------|------------------|----------------------------|------|
| Power Supply          | DIGITAL            | $V_{DD}$         | -0.3 to +7.0               | V    |
|                       | ANALOG             | $AV_{DD}$        | -0.3 to +7.0               | V    |
|                       | $V_{DD} - AV_{DD}$ | $\Delta V_{AVD}$ | $ V_{DD} - AV_{DD}  < 0.2$ | V    |
| Input Voltage         |                    | $V_{IN}$         | -0.3 to $V_{DD} + 0.3$     | V    |
| Operating Temperature |                    | $T_a$            | -30 to +80                 | °C   |
| Storage Temperature   |                    | $T_{stg}$        | -40 to +125                | °C   |
| Power Consumption     |                    | PD               | 500(DIP16)<br>200(DMP16)   | mW   |

## ■ RECOMMENDATION OPERATION CONDITION

( $V_{SS}=AV_{SS}=0V$ )

| PARAMETER    |         | SYMBOL    | CONDITIONS |      |      | UNIT |
|--------------|---------|-----------|------------|------|------|------|
|              |         |           | MIN.       | TYP. | MAX. |      |
| Power Supply | DIGITAL | $V_{DD}$  | 4.75       | 5.0  | 5.25 | V    |
|              | ANALOG  | $AV_{DD}$ | 4.75       | 5.0  | 5.25 | V    |

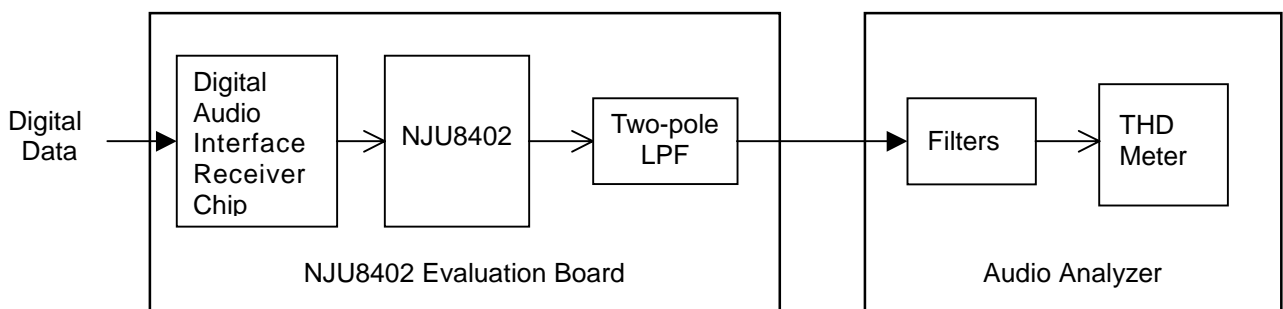
## ■ ELECTRICAL CHARACTERISTICS

### • ANALOG AC CHARACTERISTICS

(The case without the report  $T_a=25^{\circ}\text{C}$ ,  $V_{DD}=AV_{DD}=5.0\text{V}$ ,  $f_s=44.1\text{kHz}$ , Input Signal Frequency=1kHz, Input Signal Level=Full Scale, MCKI=256fs, Bandwidth=22Hz to 20kHz)

| PARAMETER                          | SYMBOL | CONDITIONS     | MIN.                  | TYP.                  | MAX.                  | UNIT                    | NOTE |
|------------------------------------|--------|----------------|-----------------------|-----------------------|-----------------------|-------------------------|------|
| Resolution                         |        |                | —                     | 16                    | —                     | bit                     |      |
| S/N                                | S/N    | EIAJ, A-weight | 90                    | 94                    | —                     | dB                      |      |
| Dynamic Range                      | DR     | EIAJ, A-weight | —                     | 94                    | —                     | dB                      |      |
| THD+N                              | THD+N  | Output 0dB     | —                     | -88                   | -82                   | dB                      |      |
| Channel Separation                 |        | EIAJ(1kHz)     | —                     | 90                    | —                     | dB                      |      |
| Differential Gain Between Channels |        |                | —                     | 0.1                   | 0.3                   | dB                      |      |
| Gain Drift                         |        |                | —                     | 100                   |                       | ppm/ $^{\circ}\text{C}$ |      |
| Maximum Output Voltage             |        |                | $0.55 \times AV_{DD}$ | $0.57 \times AV_{DD}$ | $0.59 \times AV_{DD}$ | $V_{PP}$                |      |
| Bias                               |        |                | —                     | $0.50 \times AV_{DD}$ | —                     | V                       |      |
| Output Load Resistance             |        |                | 10                    | —                     | —                     | $k\Omega$               |      |
| Output Load Capacitance            |        |                | —                     | —                     | 300                   | pF                      |      |

BLOCK DIAGRAM FOR TESTING ANALOG AC CHARACTERISTICS



Two-pole LPF :  $f_c=25\text{kHz}$  ( refer ■ APPLICATION CIRCUITS )  
 Filters : 22Hz HPF + 20kHz Ten-pole LPF  
 ( A-Weighting Filter is on at measuring S/N and Dynamic Range )

• **DIGITAL INTERPOLATION FILTER CHARACTERISTICS**

(The case without the report.  $T_a=25^{\circ}\text{C}$ ,  $V_{DD}=AV_{DD}=5.0\text{V}$ ,  $f_s=44.1\text{kHz}$ )

| PARAMETER               | SYMBOL | CONDITIONS | MIN.  | TYP. | MAX. | UNIT | NOTE |
|-------------------------|--------|------------|-------|------|------|------|------|
| Band Pass               | PB     |            | 0.02  | —    | 20.0 | kHz  |      |
| Rejection Band          | SB     |            | 24.10 | —    | —    | kHz  |      |
| Rejection Band Quantity | SA     |            | 50    | —    | —    | dB   |      |

Note :Band Pass and Rejection Band are proportioned to  $f_s$ .  $PB=0.4535 \times f_s$ ,  $SB=0.5465 \times f_s$

• **DIGITAL ANALOG LOW PASS FILTER CHARACTERISTIC**

(The case without the report.  $T_a=25^{\circ}\text{C}$ ,  $V_{DD}=AV_{DD}=5.0\text{V}$ ,  $f_s=44.1\text{kHz}$ )

| PARAMETER          | SYMBOL | CONDITIONS | MIN. | TYP.      | MAX. | UNIT | NOTE |
|--------------------|--------|------------|------|-----------|------|------|------|
| Frequency Response | FR     | 22Hz~20kHz | —    | $\pm 0.2$ | —    | dB   |      |

• **POWER CHARACTERISTICS**

(The case without the report  $T_a=25^{\circ}\text{C}$ ,  $V_{DD}=AV_{DD}=5.0\text{V}$ ,  $f_s=44.1\text{kHz}$ )

| PARAMETER      | SYMBOL               | CONDITIONS | MIN.      | TYP. | MAX. | UNIT | NOTE |
|----------------|----------------------|------------|-----------|------|------|------|------|
| Supply Voltage | $V_{DD}$ , $AV_{DD}$ |            | 4.75      | 5.0  | 5.25 | V    |      |
| Supply Current | $V_{DD}$             | $I_{DD}$   | No signal | —    | 12   | 14   | mA   |
|                | $AV_{DD}$            | $AI_{DD}$  | No signal | —    | 10   | 18   | mA   |

• **DIGITAL DC CHARACTERISTICS**

(The case without the report  $T_a=25^{\circ}\text{C}$ ,  $V_{DD}=AV_{DD}=5.0\text{V}$ )

| PARAMETER             | SYMBOL   | CONDITIONS | MIN.         | TYP. | MAX.         | UNIT          | NOTE |
|-----------------------|----------|------------|--------------|------|--------------|---------------|------|
| Digital Input Voltage | $V_{IH}$ |            | $0.7 V_{DD}$ | —    | $V_{DD}$     | V             |      |
|                       | $V_{IL}$ |            |              | —    | $0.3 V_{DD}$ | V             |      |
| Input Leakage Current | $I_{LK}$ |            | —            | —    | $\pm 1$      | $\mu\text{A}$ |      |

## • DIGITAL AC CHARACTERISTICS

(The case without the report  $T_a=25^{\circ}\text{C}$ ,  $V_{DD}=AV_{DD}=5.0\text{V}$ )

### Master Clock & Reset

| PARAMETER             |                        | SYMBOL            | CONDITIONS | MIN.  | TYP. | MAX. | UNIT | NOTE |
|-----------------------|------------------------|-------------------|------------|-------|------|------|------|------|
| MCKI                  | Frequency              | $f_{\text{MCKI}}$ | 256fs      | 1.024 | —    | 12.8 | MHz  |      |
|                       |                        |                   | 386fs      | 9.216 | —    | 19.2 | MHz  |      |
|                       | Pulse Width High-Level | $t_{\text{MCKH}}$ |            | 20    | —    | —    | ns   |      |
|                       | Pulse Width Low-Level  | $t_{\text{MCKL}}$ |            | 20    | —    | —    | ns   |      |
| Reset Low Level Width |                        | $t_{\text{RST}}$  |            | 1     | —    | —    | ns   |      |

### Digital Audio Signal Interface

| PARAMETER               |  | SYMBOL            | CONDITIONS | MIN.      | TYP. | MAX. | UNIT | NOTE |
|-------------------------|--|-------------------|------------|-----------|------|------|------|------|
| Audio DAC Sampling Rate |  | $f_s$             |            | 24        | —    | 50   | kHz  |      |
| Audio Data Setup Time   |  | $t_{\text{DS}}$   |            | 50        | —    | —    | ns   |      |
| Audio Data Hold Time    |  | $t_{\text{DH}}$   |            | 50        | —    | —    | ns   |      |
| BCLK Period             |  | $t_{\text{BCLK}}$ |            | 1/(128fs) | —    | —    | ns   |      |
| BCLK Pulse Time "H"     |  | $t_{\text{BCKH}}$ |            | 20        | —    | —    | ns   |      |
| BCLK Pulse Time "L"     |  | $t_{\text{BCKL}}$ |            | 20        | —    | —    | ns   |      |
| BCLK Rise to LRCK Edge  |  | $t_{\text{BLR}}$  |            | 40        | —    | —    | ns   |      |
| LRCK Edge to BCLK Rise  |  | $t_{\text{LRB}}$  |            | 40        | —    | —    | ns   |      |

### Control Register Interface

| PARAMETER               |  | SYMBOL           | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|-------------------------|--|------------------|------------|------|------|------|------|------|
| SCK Period              |  | $t_{\text{SCK}}$ |            | 2    | —    | —    | ns   |      |
| SCK Pulse Time "H"      |  | $t_{\text{SCH}}$ |            | 0.8  | —    | —    | ns   |      |
| SCK Pulse Time "L"      |  | $t_{\text{SCL}}$ |            | 0.8  | —    | —    | ns   |      |
| Control Data Setup Time |  | $t_{\text{DAS}}$ |            | 0.8  | —    | —    | ns   |      |
| Control Data Hold Time  |  | $t_{\text{DAH}}$ |            | 0.8  | —    | —    | ns   |      |
| REQ Pulse Time "H"      |  | $t_{\text{REH}}$ |            | 1.6  | —    | —    | ns   |      |
| SCK Data Setup Time     |  | $t_{\text{RQS}}$ |            | 0.8  | —    | —    | ns   |      |
| REQ Hold Time           |  | $t_{\text{RQH}}$ |            | 0.8  | —    | —    | ns   |      |

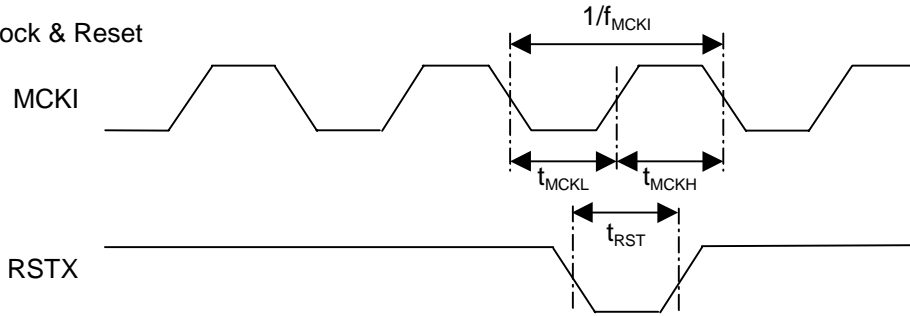
### Input Signal Rise and Fall Time

| PARAMETER              |  | SYMBOL          | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|------------------------|--|-----------------|------------|------|------|------|------|------|
| Input Signal Rise Time |  | $t_{\text{UP}}$ |            | —    | —    | 100  | ns   |      |
| Input Signal Fall Time |  | $t_{\text{DN}}$ |            | —    | —    | 100  | ns   |      |

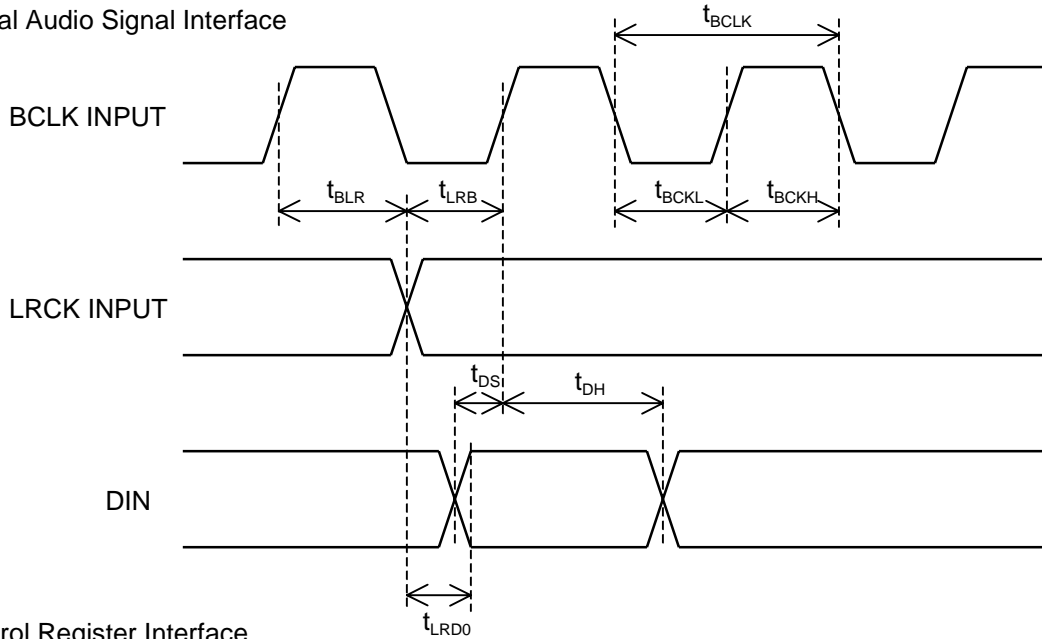


## • TIMING CHART

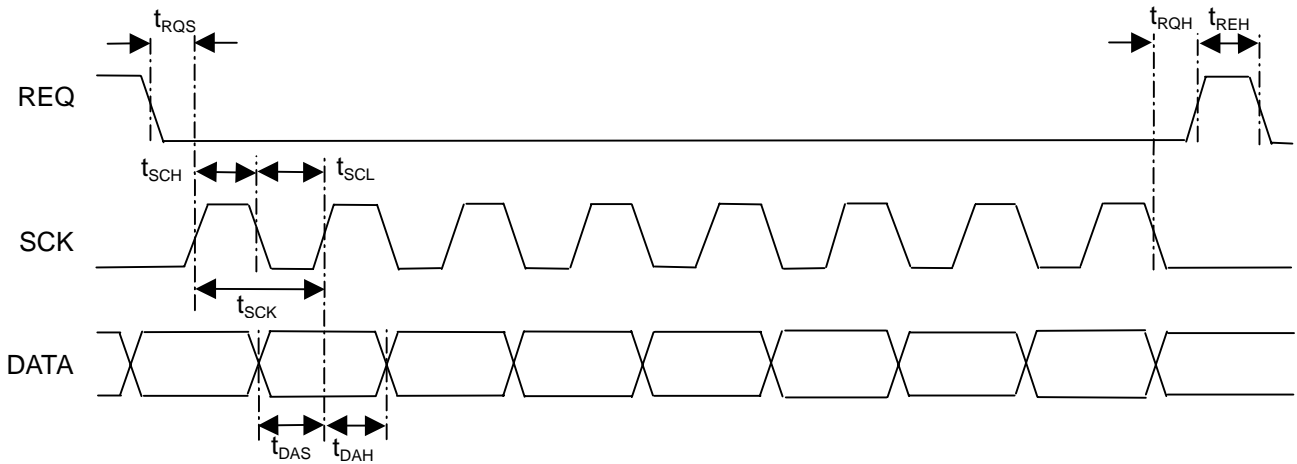
Master Clock & Reset



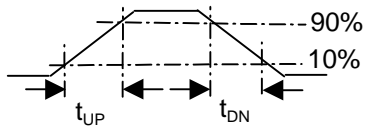
Digital Audio Signal Interface



Control Register Interface

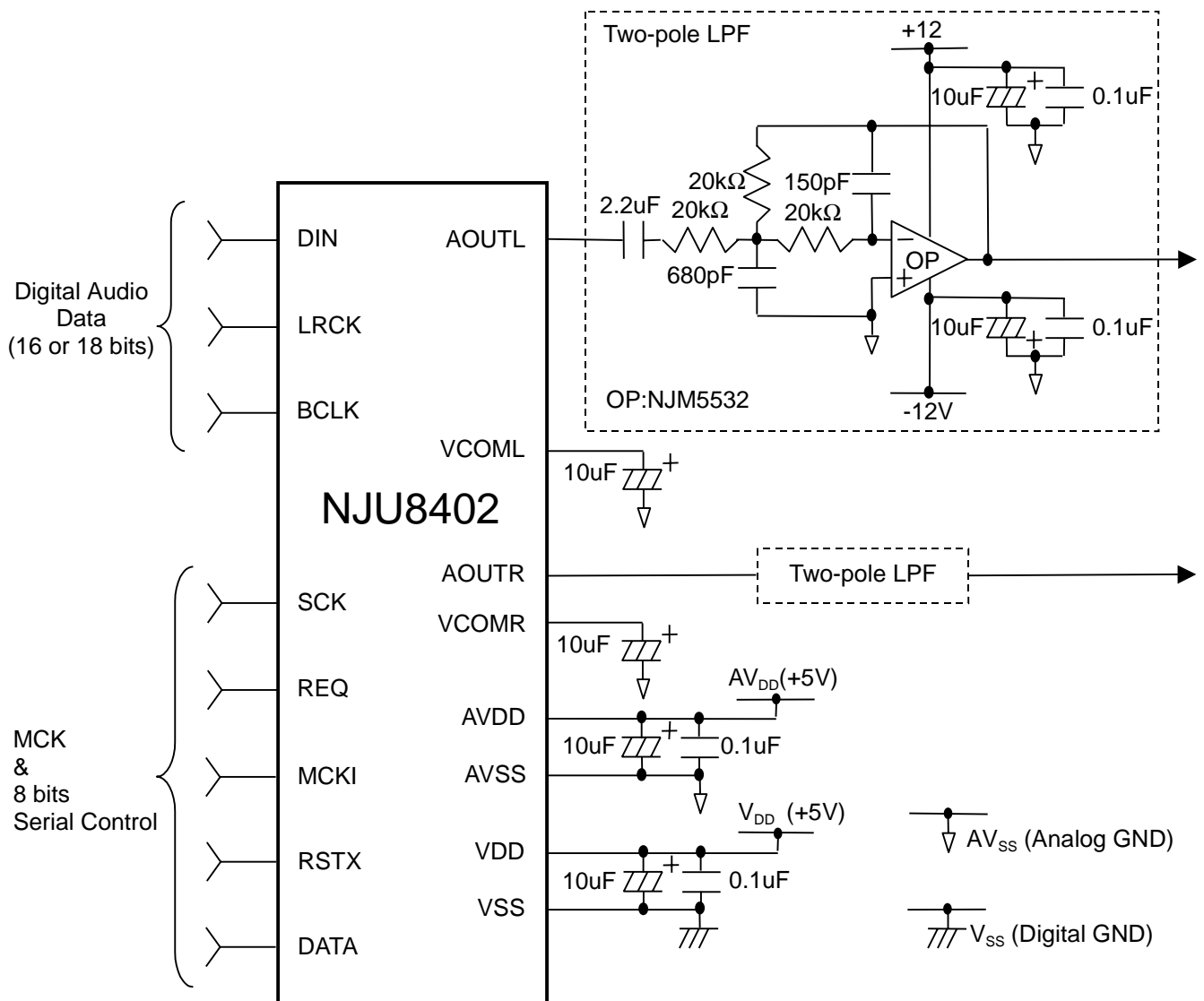


Input Signal Rise and Fall Time



# NJU8402

## APPLICATION CIRCUITS



**[CAUTION]**  
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