12-CHARACTER 4-LINE
DOT MATRIX LCD CONTROLLER

■ GENERAL DESCRIPTION

The NJU6620 is a Dot Matrix LCD controller driver for 12-character 4-line with icon display in single chip.
It contains voltage converter and regulator, bleeder resistance, CR oscillator, microprocessor interface circuits, instruction decoder controller, character generator ROM/RAM, high voltage operation common and segment drivers.
The voltage converter generates high voltage(about 8V) from the supply voltage(3V) and it is regulated by the regulator.
The bias level of LCD driving voltage is generated of high value of bleeder resistance and the buffer amplifire convert its impedance. The 16th gray scale contrast control function is incorporated for its adjustment. Therefore, simple power supply circuit and easy contrast adjustment are available.
The complete CR oscillator is incorporated, therefore no external components for oscillation circuit are required.
The microprocessor interface circuits which operate by 1MHz, can be selected serial, 4 or 8 bit interface.
The character generator ROM consists of 10,080 bits stores 252 kinds of character Font. Each 160 bits CG RAM and Icon display RAM can stores 4 kinds of special character displayed on the dot matrix display area or 152 kind of Icon on the Icon display area.
The 37-common (32 for character, 4 for icon and 1 for static) and 63-segment (60 for character, 2 for icon and 1 for static) drivers operated up to 9.9V drives 12-character 4-line with 128 Icon and static segment LCD display.
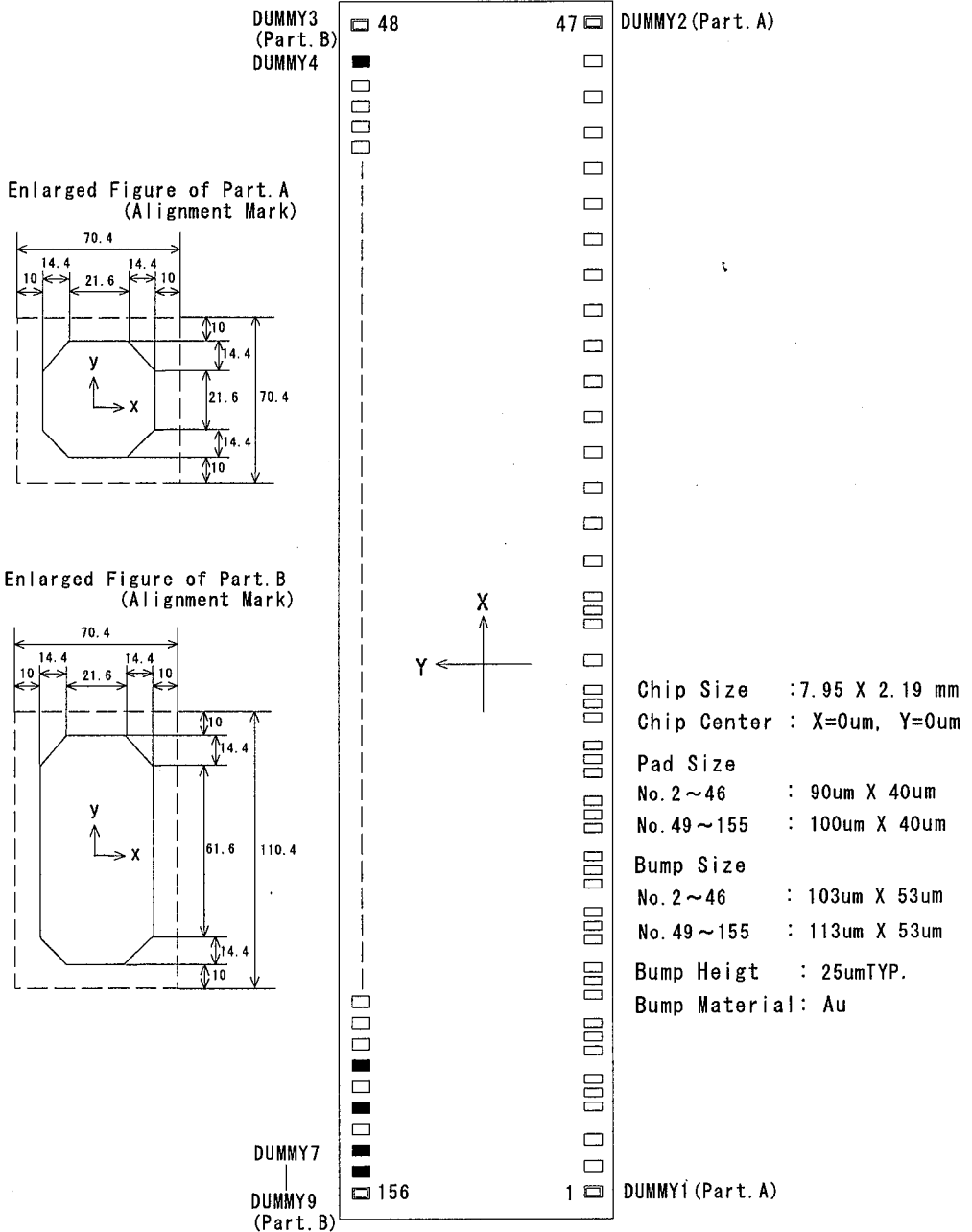
■ PACKAGE OUTLINE

NJU6620CH

■ FEATURES
● 12-character 4-line Dot Matrix LCD Controller Driver
● Maximum 128 Icon Display
● Serial, 4 or 8 Bit parallel Direct Interface with Microprocessor
● Display Data RAM   – 48 x 8 bits : Maximum 12-character 4-line Display
● Character Generator ROM – 10,080 bits : 252 Characters for 5 x 7 Dots
● Character Generator RAM – 32 x 5 bits : 4 Patterns(5 x 7 Dots)
● Icon Display RAM   – 32 x 5 bits : Maximum 128 Icon
● High Voltage LCD Driver : 37-common / 63-segment
● Duty and Bias Ratio   : 1/36 duty and 1/7 bias
● Useful Instruction Set : Clear Display, Return Home, Display ON/OFF Cont, Cursor ON/OFF
                           Cont, Display Blink, Cursor Shift, Character Shift
● Common and Segment driver Location order Select Function(Mode A/Mode B)
● Power On Initialization / Hardware Reset
● Voltage Converter and Bleeder Resistance on-chip
● Voltage regulator on-chip
● Software contrast control
● Oscillation Circuit on-chip
● Low Power Consumption
● Operating Voltage   ----   2.4 to 3.3 V (Except LCD Driving Voltage)
● Package Outline   ----   Bumped Chip
● C-MOS Technology

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Ver. 1

New Japan Radio Co., Ltd.

■ PAD LOCATION

DUMMY3 (Part.B)
DUMMY4

48   47 DUMMY2(Part.A)

Enlarged Figure of Part.A
(Alignment Mark)

70.4
14.4   14.4
10   21.6   10
10
14.4
y
21.6   70.4
X
14.4
10

Enlarged Figure of Part.B
(Alignment Mark)

70.4
14.4   14.4
10   21.6   10
10
14.4
y
61.6   110.4
X
14.4
10

X
Y ←

Chip Size   : 7.95 X 2.19 mm
Chip Center : X=0um, Y=0um

Pad Size
No. 2～46   : 90um X 40um
No. 49～155 : 100um X 40um

Bump Size
No. 2～46   : 103um X 53um
No. 49～155 : 113um X 53um

Bump Heigt   : 25umTYP.
Bump Material : Au

DUMMY7

DUMMY9   156   1   DUMMY1(Part.A)
(Part.B)

■ PAD COORDINATES CHIP   SIZE 7.95 mm x 2.19 mm (CHIP CENTER X=0 μm, Y=0 μm)

PAD No.	PAD NAME Mode A	PAD NAME Mode B	X=(μm)	Y=(μm)	PAD No.	PAD NAME Mode A	PAD NAME Mode B	X=(μm)	Y=(μm)
1	$DUMMY_1$	$DUMMY_1$	-3831	-935	51	COM_9	COM_9	3570	940
2	OSC_1	OSC_1	-3570	-935	52	COM_{10}	COM_{10}	3500	940
3	OSC_2	OSC_2	-3405	-935	53	COM_{11}	COM_{11}	3430	940
4	V_5	V_5	-3252	-935	54	COM_{12}	COM_{12}	3360	940
5	V_5	V_5	-3180	-935	55	COM_{13}	COM_{13}	3290	940
6	V_5	V_5	-3107	-935	56	COM_{14}	COM_{14}	3220	940
7	V_{SS}	V_{SS}	-2865	-935	57	COM_{15}	COM_{15}	3150	940
8	V_{SS}	V_{SS}	-2793	-935	58	COM_{16}	COM_{16}	3080	940
9	V_{SS}	V_{SS}	-2720	-935	59	COM_{25}	COM_{25}	3010	940
10	V_{5OUT}	V_{5OUT}	-2568	-935	60	COM_{26}	COM_{26}	2940	940
11	V_{5OUT}	V_{5OUT}	-2495	-935	61	COM_{27}	COM_{27}	2870	940
12	V_{5OUT}	V_{5OUT}	-2423	-935	62	COM_{28}	COM_{28}	2800	940
13	C_2^-	C_2^-	-2178	-935	63	COM_{29}	COM_{29}	2730	940
14	C_2^-	C_2^-	-2105	-935	64	COM_{30}	COM_{30}	2660	940
15	C_2^-	C_2^-	-2033	-935	65	COM_{31}	COM_{31}	2590	940
16	C_2^+	C_2^+	-1791	-935	66	COM_{32}	COM_{32}	2520	940
17	C_2^+	C_2^+	-1718	-935	67	$SEGM_1$	$SEGM_2$	2450	940
18	C_2^+	C_2^+	-1646	-935	68	SEG_1	SEG_{60}	2380	940
19	C_1^-	C_1^-	-1404	-935	69	SEG_2	SEG_{59}	2310	940
20	C_1^-	C_1^-	-1332	-935	70	SEG_3	SEG_{58}	2240	940
21	C_1^-	C_1^-	-1259	-935	71	SEG_4	SEG_{57}	2170	940
22	C_1^+	C_1^+	-1017	-935	72	SEG_5	SEG_{56}	2100	940
23	C_1^+	C_1^+	-945	-935	73	SEG_6	SEG_{55}	2030	940
24	C_1^+	C_1^+	-872	-935	74	SEG_7	SEG_{54}	1960	940
25	V_{DD}	V_{DD}	-719	-935	75	SEG_8	SEG_{53}	1890	940
26	V_{DD}	V_{DD}	-646	-935	76	SEG_9	SEG_{52}	1820	940
27	V_{DD}	V_{DD}	-574	-935	77	SEG_{10}	SEG_{51}	1750	940
28	VR	VR	-423	-935	78	SEG_{11}	SEG_{50}	1680	940
29	V_{REG}	V_{REG}	-10	-935	79	SEG_{12}	SEG_{49}	1610	940
30	V_{REG}	V_{REG}	62	-935	80	SEG_{13}	SEG_{48}	1540	940
31	V_{REG}	V_{REG}	135	-935	81	SEG_{14}	SEG_{47}	1470	940
32	TEST	TEST	324	-935	82	SEG_{15}	SEG_{46}	1400	940
33	SEL	SEL	666	-935	83	SEG_{16}	SEG_{45}	1330	940
34	RESET	RESET	841	-935	84	SEG_{17}	SEG_{44}	1260	940
35	P/S	P/S	1131	-935	85	SEG_{18}	SEG_{43}	1190	940
36	RS	RS	1299	-935	86	SEG_{19}	SEG_{42}	1120	940
37	R/W	R/W	1590	-935	87	SEG_{20}	SEG_{41}	1050	940
38	E/SCL	E/SCL	1758	-935	88	SEG_{21}	SEG_{40}	980	940
39	DB_0	DB_0	2031	-935	89	SEG_{22}	SEG_{39}	910	940
40	DB_1	DB_1	2255	-935	90	SEG_{23}	SEG_{38}	840	940
41	DB_2	DB_2	2497	-935	91	SEG_{24}	SEG_{37}	770	940
42	DB_3	DB_3	2722	-935	92	SEG_{25}	SEG_{36}	700	940
43	DB_4	DB_4	2964	-935	93	SEG_{26}	SEG_{35}	630	940
44	DB_5	DB_5	3189	-935	94	SEG_{27}	SEG_{34}	560	940
45	DB_6	DB_6	3430	-935	95	SEG_{28}	SEG_{33}	490	940
46	DB_7	DB_7	3655	-935	96	SEG_{29}	SEG_{32}	420	940
47	$DUMMY_2$	$DUMMY_2$	3831	-935	97	SEG_{30}	SEG_{31}	350	940
48	$DUMMY_3$	$DUMMY_3$	3785	940	98	SEG_{31}	SEG_{30}	280	940
49	$DUMMY_4$	$DUMMY_4$	3710	940	99	SEG_{32}	SEG_{29}	210	940
50	$SEGS_1$	$SEGS_1$	3640	940	100	SEG_{33}	SEG_{28}	140	940

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PAD No.	PAD NAME Mode A	PAD NAME Mode B	X=(μm)	Y=(μm)
101	SEG_{34}	SEG_{27}	70	940
102	SEG_{35}	SEG_{26}	0	940
103	SEG_{36}	SEG_{25}	-70	940
104	SEG_{37}	SEG_{24}	-140	940
105	SEG_{38}	SEG_{23}	-210	940
106	SEG_{39}	SEG_{22}	-280	940
107	SEG_{40}	SEG_{21}	-350	940
108	SEG_{41}	SEG_{20}	-420	940
109	SEG_{42}	SEG_{19}	-490	940
110	SEG_{43}	SEG_{18}	-560	940
111	SEG_{44}	SEG_{17}	-630	940
112	SEG_{45}	SEG_{16}	-700	940
113	SEG_{46}	SEG_{15}	-770	940
114	SEG_{47}	SEG_{14}	-840	940
115	SEG_{48}	SEG_{13}	-910	940
116	SEG_{49}	SEG_{12}	-980	940
117	SEG_{50}	SEG_{11}	-1050	940
118	SEG_{51}	SEG_{10}	-1120	940
119	SEG_{52}	SEG_9	-1190	940
120	SEG_{53}	SEG_8	-1260	940
121	SEG_{54}	SEG_7	-1330	940
122	SEG_{55}	SEG_6	-1400	940
123	SEG_{56}	SEG_5	-1470	940
124	SEG_{57}	SEG_4	-1540	940
125	SEG_{58}	SEG_3	-1610	940
126	SEG_{59}	SEG_2	-1680	940
127	SEG_{60}	SEG_1	-1750	940
128	$SEGM_2$	$SEGM_1$	-1820	940
129	COM_{24}	COM_{24}	-1890	940
130	COM_{23}	COM_{23}	-1960	940
131	COM_{22}	COM_{22}	-2030	940
132	COM_{21}	COM_{21}	-2100	940
133	COM_{20}	COM_{20}	-2170	940
134	COM_{19}	COM_{19}	-2240	940
135	COM_{18}	COM_{18}	-2310	940
136	COM_{17}	COM_{17}	-2380	940
137	COM_8	COM_8	-2450	940
138	COM_7	COM_7	-2520	940
139	COM_6	COM_6	-2590	940
140	COM_5	COM_5	-2660	940
141	COM_4	COM_4	-2730	940
142	COM_3	COM_3	-2800	940
143	COM_2	COM_2	-2870	940
144	COM_1	COM_1	-2940	940
145	$COMM_4$	$COMM_4$	-3010	940
146	$COMM_3$	$COMM_3$	-3080	940
147	$COMM_2$	$COMM_2$	-3150	940
148	$COMM_1$	$COMM_1$	-3220	940
149	$COMS_1$	$COMS_1$	-3290	940
150	$DUMMY_5$	$DUMMY_5$	-3360	940

PAD No.	PAD NAME Mode A	PAD NAME Mode B	X=(μm)	Y=(μm)
151	CV1V4	CV1V4	-3430	940
152	$DUMMY_6$	$DUMMY_6$	-3500	940
153	CV2V3	CV2V3	-3570	940
154	$DUMMY_7$	$DUMMY_7$	-3640	940
155	$DUMMY_8$	$DUMMY_8$	-3710	940
156	$DUMMY_9$	$DUMMY_9$	-3785	940

Note) Mode A : SEL="L", Mode B : SEL="H"

■ BLOCK DIAGRAM

Block diagram of the NJU6620 showing signal inputs CLK1, CLK2, RESET, RS, R/W, E/SCL, P/S, DB7/CS, DB6/SIO, DB4~DB5, DB0~DB3, SEL connecting through Main OSC, RESET, I/O Buffer, Instruction Reg. (IR), Add. Count., Data Reg. (DR), Busy Flag, Instruction Decoder (ID), Timing Gen., Display Control circuit (COM/SEG Driver control, Cursor Blink control), Display Data RAM (DD RAM) 48x8 bits, Icon Display RAM (MK RAM) 32x5bits, Character Generator RAM (CG RAM) 32x5bits, Character Generator ROM (CG ROM) 10080bits, Sub. OSC, Static Driver, 36bit Shift Reg., Common Driver, 62bit Latch, Segment Driver with outputs COMS1, SEGS1, COM1~COM32, COMM1~COMM4, CV1V4, SEG1~SEG60, SEGM1~SEGM2, CV2V3.

LCD Driving Voltage section showing V1, V2, V3, V4, V5, VDD, VSS, RB1, RB1, RB2, RB1, RB1, and E.V.R. Value (16 Step), Voltage Conv., VREG, VR, V5OUT, C1+, C1-, C2+, C2-.

NJU6620

■ TERMINAL DESCRIPTION

PAD No	SYMBOL	I/O	FUNCTION
25~27 7~9	V_{DD}, V_{SS}	—	Power Source VDD; +3V, VSS; 0V
4~6	V_5	—	LCD driving voltage
2	OSC_1	I	System clock input terminal This terminal should be open, for internal clock operation.
3	OSC_2	O	System clock output terminal This terminal can use for clock frequency monitoring. 。
35	P/S	I	Parallel or serial interface selection terminal "0":Serial interface "1":Parallel interface
36	RS	I	Register selection signal input terminal "0":Instruction register (writing) Busy flag, address counter (reading) "1":Data register (writing / reading)
37	R/W	I	Read / Write selection signal input terminal "0":Write "1": Read
38	E	I	Read / Write activation signal input in parallel mode
	SCL	I	Sift clock input in serial mode
46	DB_7	I/O	3-state data bus for MSB to transfer the Data between MPU and NJU6620 in parallel mode . DB 7 is also used for the Busy Flag reading.
	CS	I	Chip select signal input in serial mode
45	DB_6	I/O	3-state data bus for bit 6 to transfer the Data between MPU and NJU6620 in parallel mode
	SIO	I/O	Serial Data I/O in serial mode
43, 44	DB_5	I/O	3-state data bus for bit 4 and 5 to transfer the Data between MPU and NJU6620 in parallel mode .
39~42	DB_4	I/O	In serial mode, these terminals are not used and should be open.
39~42	DB_0~DB_3	I/O	3-state data bus for lower 4 bit to transfer the Data between MPU and NJU6620 in parallel mode In serial and 4-bit parallel mode, these terminals are not used and should be open.
153, 151	CV_1V_4, CV_2V_3	—	Capacitor terminals for noise reduction of COM/SEG output voltage. The capacitor connected between CV1V4, CV2V3 and VDD is required to operate with the LCD panel actually.

PAD No	SYMBOL	I/O	FUNCTION
51~66 129~144	COM$_1$~COM$_{32}$	O	LCD common driving signal output terminals
145~148	COMM$_1$~COMM$_4$	O	Icon common driving signal output terminals
149	COMS$_1$	O	Static driving common signal output terminal When power down mode, VDD or VSS level are output.
68~127	SEG$_1$~SEG$_{60}$	O	LCD segment driving signal output terminals
67, 128	SEGM$_1$, SEGM$_2$	O	Icon segment driving signal output terminals
50	SEGS$_1$	O	Static Driving Segment signal output terminal When power down mode, VDD or VSS level are output.
13~24	C2$^-$, C2$^+$ C1$^-$, C1$^+$	I/O	Step up voltage capacitor connecting terminals In case of tripler operation, connect the capacitor between C1+ and C1−, C2+ and C2−. In case of doubler operation, connect the capacitor between C2+ and C2−, connect C2+ to C1+, and C1− should be open.
10~12	V$_{5OUT}$	O	Step up voltage output terminal
29~31	V$_{REG}$	O	Voltage regulator output terminal Connect the resistor between this terminal and VR Terminal.
28	VR	I	Reference voltage for voltage regulator input terminal Connect the resistor between this terminal and VDD terminal.
34	RESET	I	Reset Terminal. When the "L" level input over than 1.2ms to this terminal, the system will be reset (at fOSC=212KHz).
33	SEL	I	Common and Segment driver location order select terminal "0":Mode A location (See the PAD COORDINATES) "1":Mode B location (See the PAD COORDINATES)
32	TEST	I	Maker Testing Terminal (Pull down) This terminal should be connected to VSS or open.
49, 150 152, 154 155, 156	DUMMY$_4$ ~DUMMY$_8$	—	Dummy terminal These terminals are electrically open.
1, 47 48, 156	DUMMY$_1$ DUMMY$_2$ DUMMY$_3$ DUMMY$_9$	—	Dummy terminal These terminals are electrically open and an alignment pattern is placed beside each terminals.

■FUNCTIONAL DESCRIPTION

(1)Description for each block

(1-1)Register

The NJU6620 incorporates two 8-bit registers, an Instruction Register(IR) and a Data Register (DR). The Register(IR) stores instruction codes such as "Clear Display" and "Cursor Shift" or address data for Display Data RAM(DD RAM), Character Generator RAM(CG RAM) and Icon Display RAM (MK RAM).
The MPU can write the instruction code and address data to the Register(IR), but it cannot read out from the Register(IR).
The Register(DR) is a temporary stored register, the data stored in the Register(DR) is written into the DD RAM, CG RAM or MK RAM and read out from the DD RAM, CG RAM or MK RAM.
The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM, CG RAM or MK RAM by internal operation.
When the address data for the DD RAM, CG RAM or MK RAM is written into the Register(IR), the addressed data in the DD RAM, CG RAM or MK RAM is transferred to the Register(DR).
By the MPU read out the data in the Register(DR), the data transmitting process is performed completely.
After reading the data in the Register(DR) by the MPU, the next address data in the DD RAM, CG RAM or MK RAM is transferred automatically to the Register(DR) to provide for the next MPU reading.
These two registers are selected by the selection signal RS as shown below.
Table 1. shows register operation controlled by RS and R/W signals.

Table 1.   Register Operation

RS	R/W	Selected Register	Operation
O	O	IR	Write
O	1	IR	Read busy flag(DB7) and address counter(DB0~DB6)
1	O	DR	Write (Register(DR) to DD RAM, CG RAM or MK RAM)
1	1	DR	Read (DD RAM, CG RAM or MK RAM to Register(DR))

(1-2)Busy Flag (BF)
When the internal circuits are in the operation mode, the busy flag(BF) is "1", and any instruction reading is inhibited.
The busy flag(BF) is output at DB7 when RS="0" and R/W="1" as shown in Table 1.
The next instruction should be written after the busy flag(BF) goes to "0".

(1-3)Address Counter (AC)
The address counter(AC) addresses the DD RAM, CG RAM or MK RAM.
When the address setting instruction is written into the Register(IR), the address informtion is transferred from Register(IR) to the Counter(AC). The selection of either the DD RAM, CG RAM or MK RAM is also determined by this instruction.
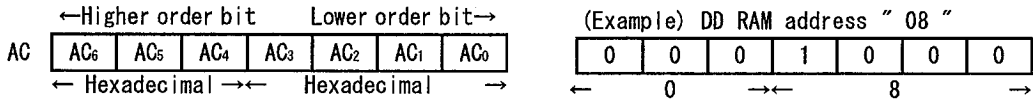After writing (or reading) the display data to (or from) the DD RAM, CG RAM or MK RAM, the Counter(AC) increments (or decrements) automatically.
The address data in the Counter(AC) is output from DB6~DB0 when RS="0" and R/W="1" as shown in Table 1.

(1-4) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consists of 48 x 8 bits stores up to 48-character display data represented in 8-bit code.
The DD RAM address data set in the address counter(AC) is represented in Hexadecimal.

←Higher order bit   Lower order bit→

(Example) DD RAM address " 08 "

AC	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
	← Hexadecimal →←			Hexadecimal			→

0	0	0	1	0	0	0
←	0	→←		8		→

· 4-line Display

The relation between DD RAM address and display position on the LCD is shown below.

Display Position	1	2	3	4	5	6	7	8	9	10	11	12
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B
2nd Line	10	11	12	13	14	15	16	17	18	19	1A	1B
3rd Line	20	21	22	23	24	25	26	27	28	29	2A	2B
4th Line	30	31	32	33	34	35	36	37	38	39	3A	3B

←DD RAM Address (Hexadecimal)

Note : The 1st, 2nd, 3rd and 4th line address are defined as (00)H to (0B)H, (10)H to (1B)H, (20)H to (2B)H, and (30)H to (3B)H. The end of each line address and the beginning of following line address are not consecutive.

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00)←	01	02	03	04	05	06	07	08	09	0A	0B	00
(10)←	11	12	13	14	15	16	17	18	19	1A	1B	10
(20)←	21	22	23	24	25	26	27	28	29	2A	2B	20
(30)←	31	32	33	34	35	36	37	38	39	3A	3B	30

(Right Shift Display)

0B	00	01	02	03	04	05	06	07	08	09	0A	→(0B)
1B	10	11	12	13	14	15	16	17	18	19	1A	→(1B)
2B	20	21	22	23	24	25	26	27	28	29	2A	→(2B)
3B	30	31	32	33	34	35	36	37	38	39	3A	→(3B)

Note : The left and right shift performes only in same line, the display data do not change to other line.

(1-5) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character code.
The storage capacity is up to 252 kinds of 5 x 7 dots character pattern(available address is (04)H through (FF)H).
The correspondence between character code and standard character pattern of NJU6620 is shown in Table 2-1.
User-defined character patterns (Custom Font) are also available by mask option.

Table 2-1. CG ROM Character Pattern (ROM version -02)

(1-6) Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) can store any kind of character pattern in 5 x 7 dots written by the user program to display user's original character pattern. The CG RAM can store 4 kind of character in 5 x 7 dots mode.
To display user's original character pattern stored in the CG RAM, the address data (00)H–(03)H should be written to the DD RAM as shown in Table 2-1.
Table 3. show the correspondence among the character pattern, CG RAM address and Data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern(5 x 7 dots)

Character Code (DD RAM data)	CG RAM Address		Character Pattern (CG RAM data)	
7 6 5 4 3 2 1 0 ← Upperbit Lower bit →	7 6 5 4 3 2 1 0 ← Upperbit Lower bit →		4 3 2 1 0 Upper bit Lower bit	
0 0 0 0 0 0 0 0	0 1 0 0 0	000 001 010 011 100 101 110 111	1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 0 0 0 0 0	Character Pattern Example(1) ←Cursor Position
0 0 0 0 0 0 0 1	0 1 0 0 1	000 001 010 011 100 101 110 111	1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0	Character Pattern Example(2) ←Cursor Position
		000 001		
. . . .	. . . .	. . . .	. . . .	
0 0 0 0 0 0 1 1	0 1 0 1 1			
		100 101 110 111		

Notes : 1. Character code bit 0,1 correspond to the CG RAM address bit 3,4(2bits:4 patterns).
2. CG RAM address 0 to 2 designate character pattern line position. The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 8th line should be "0". If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above.
4. CG RAM character patterns are selected when character code bits 2 to 7 are all "0" and these are addressed by character code bits 0 and 1.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.

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(1-7) Icon Display RAM (MK RAM)

The NJU6620 can display maximum 128 Icons.
The Icon Display can be controlled by writing the Data in MK RAM corresponds to the Icon.
The relation between MK RAM address and Icon Display position is shown below:
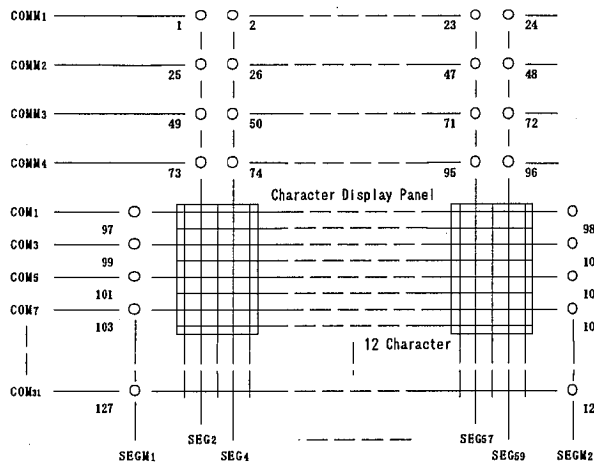
Table 4. Correspondence among Icon Position, MK RAM Address and Data

MK RAM Address		Bits for Icon Display Position								
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0110 0000	60ₕ	*	*	*	1	2	3	4	97	COMM1 Line and Both besides of 1st Line (COM1, 3, 5, 7)
0110 0001	61ₕ	*	*	*	5	6	7	8	98	
:	:				:					
0110 0101	65ₕ	*	*	*	21	22	23	24	102	
0110 0110	66ₕ	*	*	*	*	*	*	*	103	
0110 0111	67ₕ	*	*	*	*	*	*	*	104	
0110 1000	68ₕ	*	*	*	25	26	27	28	105	COMM2 Line and Both besides of 2nd Line (COM9, 11, 13, 15)
0110 1001	69ₕ	*	*	*	29	30	31	32	106	
:	:				:					
0110 1101	6Dₕ	*	*	*	45	46	47	48	110	
0110 1110	6Eₕ	*	*	*	*	*	*	*	111	
0110 1111	6Fₕ	*	*	*	*	*	*	*	112	
0111 0000	70ₕ	*	*	*	49	50	51	52	113	COMM3 Line and Both besides of 3rd Line (COM17, 19, 21, 23)
0111 0001	71ₕ	*	*	*	53	54	55	56	114	
:	:				:					
0111 0101	75ₕ	*	*	*	69	70	71	72	118	
0111 0110	76ₕ	*	*	*	*	*	*	*	119	
0111 0111	77ₕ	*	*	*	*	*	*	*	120	
0111 1000	78ₕ	*	*	*	73	74	75	76	121	COMM4 Line and Both besides of 4th Line (COM25, 27, 29, 31)
0111 1001	79ₕ	*	*	*	77	78	79	80	122	
:	:				:					
0111 1101	7Dₕ	*	*	*	93	94	95	96	126	
0111 1110	7Eₕ	*	*	*	*	*	*	*	127	
0111 1111	7Fₕ	*	*	*	*	*	*	*	128	

Notes: 1. When the Icon display function using, the system should be initialized by the software initialization because the MK RAM is not initialized by the power turning on and hardware reset.

2. The cross-points between SEGM1, SEGM2 and some of common COMM1 through COMM4, even common likes as COM2, COM4...COM32, are always off because of the corresponding RAM does not exist as shown above.

3. In the table 4, the bits D5 to D7 mentioned by * are invalid, therefore both of "0" or "1" can be written but these are no meaning.

(1-8) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM and MK RAM and other internal circuits.
RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.
Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

(1-9) LCD Driver

LCD Driver consist of 37-common driver and 63-segment driver.
The character pattern data are latched to the addressed Segment-register respectively. This latched data controls display driver to output LCD driving waveform.

(1-10) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and the cursor position character blinks.
The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).
When the address counter is (08)H, a cursor position is shown as follows:

	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
AC	0	0	0	1	0	0	0

4-Line display

	1	2	3	4	5	6	7	8	9	10	11	12	←Display position
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B	←DD RAM address
2nd Line	10	11	12	13	14	15	16	17	18	19	1A	1B	(Hexadecimal)
3rd Line	20	21	22	23	24	25	26	27	28	29	2A	2B	
4th Line	30	31	32	33	34	35	36	37	38	39	3A	3B	

Cursor position

Note : The cursor or blinks also appear when the address counter (AC) selects the CG RAM or the MK RAM. But the displayed cursor and blink are meaningless.
If the AC storing the CG or MK RAM address data, the cursor and blink are displayed in the meaningless position.

(2)Power on Initialization by internal circuits

(2-1)Initialization By Internal Reset Circuits

The NJU6620 is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 7 ms (fosc=212kHz) after VDD rises to 2.4V.

Initialization flow is shown below:

Function Set	DL=1 :8-bit long interface data PD=1 :Power down off
Contrast control	Setting (00)H to the contrast control register
Display On/Off control	D = 0 :Display Off C = 0 :Cursor Off B = 0 :Cursor Blink Off
Entry Mode Set	I/D=1 :Increment by 1 S = 0 :No Shift
Clear Display	AC=00H
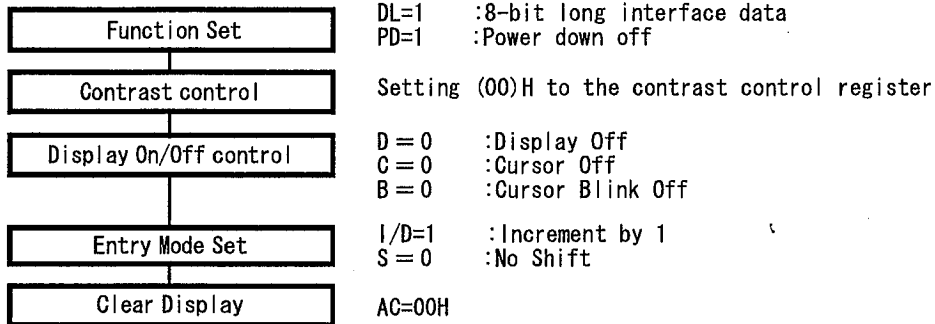
Note : If the condition of power supply rise time described in the Electrical Characteritics is not satisfied, the internal Power On Initialization Circuits will not operated and initialization will not performed.
In this case the initialization by MPU software is required.

(2-2)Initialization By Hardware

The NJU6620 incorporates RESET terminal to initialize the all system. When the "L" level input over 1.2ms to the RESET terminal, reset sequence is executed. In this time, busy signal output during 7 ms (fosc=212kHz) after RESET terminal goes to "H".

・Timing Chart
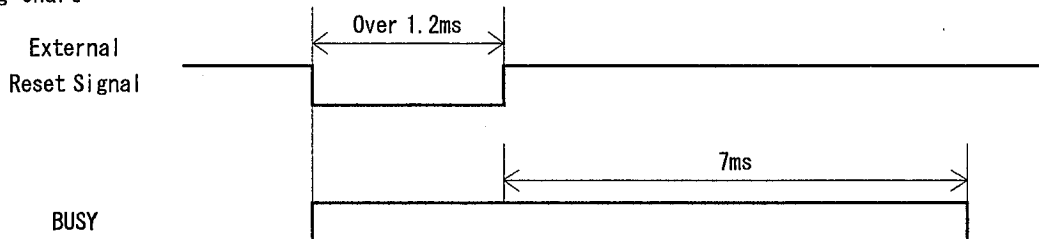
(3)Instructions

The NJU6620 incorporates two registers, an Instruction Register (IR) and a Data Register(DR). These two registers store control information temporarily to allow interface between NJU6620 and MPU or peripheral ICs operating different cycles. The operation of NJU6620 is determined by this control signal from MPU. The control information includes register selection signals (RS), read/write signals (R/W) and data bus signals (DB0 to DB7).
Table 5. shows each instruction and its operating time.

Note : The execution time mentioned in Table 5. based on fcp or fosc=212kHz.
If the oscillation frequency is changed, the execution time is also changed.

Table 4.   Table of Instructions

INSTRUCTIONS	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	Execute Time f_{osc} = 212KHz
Maker Testing	0	0	0	0	0	0	0	0	0	0	All "0" code is using for maker testing.	—
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets RAM address (00)H in AC.	6.87ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets RAM address (00)H in AC and returns display being shifted original position. RAM contents remain unchanged.	141μs
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display are performed in data read/write. I/D=1:Increment, I/D=0:Decremen S=1:Accompanies display shift	0μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B).	0μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor & shifts display without changing RAM contents S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to the right R/L=0 : Shift to the left	cursor: 141μs display: 0μs
Function Set	0	0	0	0	1	DL	*	*	*	PD	Sets interface data length(DL) and power down mode (PD).	PD=0: 0μs PD=1: 200μs
Contrast control	0	0	0	1	*	*	←—	Cc	—→		Sets data to Contrast Control Register.	0μs
Set RAM Address	0	0	1	←——			AR		—→		Sets RAM address. After this instruction, the data is transferred to/from RAM.	141μs
Read Busy Flag & AC contents	0	1	BF	←——			AC		—→		Reads busy flag and AC content BF=1 : Internally operating BF=0 : Can accept instruction	0μs
Write Data to RAM	1	0	←—		Write Data (DD RAM)			—→			Writes data into RAM.	141μs
	1	0	*	*	*	←—	(CG RAM)		—→			
	1	0	*	*	*	←—	(MK RAM)		—→			
Read Data from RAM	1	1	←—		Write Data (DD RAM)			—→			Reads data from RAM.	141μs
	1	1	*	*	*	←—	(CG RAM)		—→			
	1	1	*	*	*	←—	(MK RAM)		—→			
Explanation of Abbreviation	DD RAM : Display data RAM, CG RAM : Character generator RAM, MK RAM : Icon display RAM, AR : RAM address (both of DD, CG and MK RAM) AC : Address counter used for both of DD, CG and MK RAM											

*:Don't care

(3-1)Description of each instructions

(a)Maker Testing

Code	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	0	0	0	0	0	0	0	0	0	0

All "0" code in 4-bit length is using for device testing mode (only for maker).
Therefore, please avoid all "0" input or no meaning Enable signal input at data "0".
(Especially please pay attention the output condition of Enable signal when the power turns on.)

(b)Clear Display

Code	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code "1" is written into DB0.
When this instruction is executed, the space code (20)H is written into every DD RAM address,
the DD RAM address (00)H is set into the address counter and entry mode is set increment.
If the cursor or blink are displayed, they are returned to the left end of the 1st line in
the LCD.
The S of entry mode does not change.

Note: The character pattern for character code (20)H must be blank code in the user-defined
      character pattern(Custom font).

(c)Return Home

Code	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	0	0	0	0	0	0	0	0	1	*

* =Don't Care

Return home instruction is executed when the code "1" is written into DB1. When this instruc-
tion is executed, the DD RAM address (00)H is set into the address counter. Display is re-
turned its original position if shifted, the cursor or blink are returned to the left end of
the 1st line in the LCD if the cursor or blink are on the display.
The DD RAM contents do not change.

(d) Entry Mode Set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB2 and the codes of (I/D) and (S) are written into DB1(I/D) and DB0(S), as shown below.
(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	Function
1	Address increment: The address of the DD RAM or CG RAM increment (+1) when the read/write, and the cursor or blink move to the right.
0	Address decrement: The address of the DD RAM or CG RAM decrement (−1) when the read/write, and the cursor or blink move to the left.

S	Function
1	Entire display shift. The shift direction is determined by I/D.: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shift.

(e) Display ON/OFF Control

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

Display On/Off control instruction which controls the whole display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB3 and the codes of (D), (C) and (B) are written into DB2(D), DB1(C) and DB0(B), as shown below.

D	Function
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

C	Function
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change

B	Function
1	The cursor position character is blinking. Blinking rate is 439ms at fosc=212kHz. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.
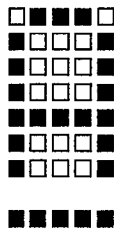
Character Font 5 x 7 dots

(1) Cursor display example
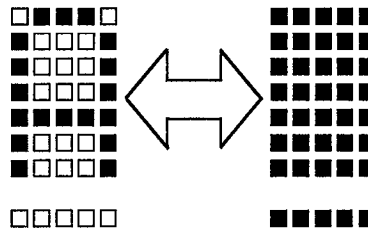
Alternating display

(2) Blink display example

(f) Cursor/Display Shift

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Code	0	0	0	0	0	1	S/C	R/L	*	*	* =Don't Care

The Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display. The cursor moves to the 2nd line when it passes the 12th digit of the 1st line. Notice that the every 1st to 3rd line displays shift at the same time. When the displayed data are shifted repeatedly, each line moves only horizontally.
The 2nd and 3rd line display does not shift into the 1st and 2nd line.
The contents of address counter (AC) does not change by operation of the display shift only.
This instruction is executed when the code "1" is written into DB4 and the codes of (S/C) and (R/L) are written into DB3 (S/C) and DB2 (R/L), as shown below.

S/C	R/L	Function
0	0	Shifts the cursor position to the left ((AC) is decremented by 1)
0	1	Shifts the cursor position to the right ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

(g) Function Set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Code	0	0	0	0	1	DL	*	*	*	PD	* =Don't Care

Function set instruction which sets the interface data length and powerdown mode, is executed, when the code "1" is written into DB5 and the code of (DL) and (PD) is written into DB4 (DL) and DB0 (PD), as shown below. In the serial interface operation, the DL is not cared.
When the powerdown mode is set, the display is off automatically (D=0). Afterward, when the powerdown mode is reset, the display is off continuously. The display is appeared by the display on (D="1") instruction.

Note : This function set instruction must be performed at the head of the program prior to all other existing instructions (except Busy flag/Address read). This function set instruction can not be executed afterwards unless the interface data length change.

DL	Function
1	Set the interface data length of 8-bit (using from DB7 to DB0) in the parallel operation only
0	Set the interface data length of 4-bit (using from DB7 to DB4) in the parallel operation only the data must be sent or received twice in this mode.

PD	Function
1	Power down mode off (Normal operation)
0	Power down mode on (The display goes to off automatically.)

Note : When the Power down mode, it must be not execution except for this instruction.

(h) Contrast Control

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Code	0	0	0	1	*	*	C_3	C_2	C_1	C_0	* =Don't Care

Contrast Control instruction which adjusts the contrast of the LCD, is executed when the code "1" is written into DB6 and the codes of C3 to C0 are written into DB3 to DB0 as shown below.
The contrast of LCD can be adjusted one of 16 voltage stage by setting this 4-bit register.
See (5-1) to realize "how to adjust the Contrast of LCD".
Set the binary code "0000" when contrast adjustment is unused.

C_3	C_2	C_1	C_0	V_{LCD}
0	0	0	0	low
		:		
		:		
1	1	1	1	high

$V_{LCD} = V_{DD} - V_5$

(i) Set RAM Address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	A	A	A	A	A	A	A

←Higher order bit   Lower order bit→

The RAM address set instruction is executed when the code "1" is written into DB7 and the address is written into DB6 to DB0 as shown above.
The address data (DB6 to DB0) is written into the address counter (AC) by this instruction.
After this instruction execution, the data writing/reading is performed into/from the addressed RAM.
The RAM includes DD RAM, CG RAM and MK RAM, and these RAMs are shared by address as shown below.

```
                              RAM  Address
DD RAM 1st Line        : from (00)H to (0B)H
DD RAM 2nd Line        : from (10)H to (1B)H
DD RAM 3rd Line        : from (20)H to (2B)H
DD RAM 4th Line        : from (30)H to (3B)H
CG RAM 4 characters    : from (40)H to (5F)H
MK RAM 128 icons       : from (60)H to (7F)H
```

(j) Read Busy Flag & AC contents

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	A	A	A	A	A	A	A

←Higher order bit   Lower order bit→

This instruction reads out the internal status of the NJU6620. When this instruction is executed, the busy flag (BF) stored in DB7 and the address counter (AC) contents stored in DB6 to DB0 are read out.
The (BF)="1" indicates that internal operation is in progress. The next instruction is inhibited when (BF)="1". Check the (BF) status before the next write operation.

(k) Write Data to RAM

Write Data to RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).

By the execution of this instruction, the binary 8-bit data (A7 to A0) are written into the DD RAM, and the binary 5-bit data (A4 to A0) are written into the CG or MK RAM. The selection of RAM is determined by the previous instruction. After this instruction execution, the address increment(+1) or decrement(-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

·Write Data to DD RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	D	D	D	D	D	D	D	D

←Higher order bit   Lower order bit→

·Write Data to CG or MK RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	*	*	*	D	D	D	D	D

←Higher order bit   Lower order bit→   * =Don't Care

(l) Read Data from MK RAM

Read Data from RAM instruction is executed when the code "1" is written into (RS) and (R/W). By the execution of this instruction, the binary 8-bit data (D7 to D0) are read out from the DD RAM, the binary 5-bit data (D4 to D0) are read out from the CG or MK RAM. The selection of RAM is determined by previous instruction. Before executing this instruction, RAM address set must be executed, otherwise the read out data are invalidated.

When this instruction is serially executed, the next address data is normally read from the second read.

The RAM address set instruction is not required if the cursor shift instruction is executed just beforehand (only DD RAM reading). The cursor shift instruction has same function as the DD RAM address set, so that after reading the DD RAM, the address increment or decrement is executed automatically according to the entry mode.

But display shift does not occur regardless of the entry mode.

Note : The address counter(AC) is automatically incremented or decremented by 1 after write instruction to either of the DD RAM, CG RAM or DD RAM. Even if the read instruction is executed after this write instruction, the addressed data can not be read out correctly.

For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

·Read Data from DD RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	D	D	D	D	D	D	D	D

←Higher order bit   Lower order bit→

·Read Data from CG or MK RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	*	*	*	D	D	D	D	D

←Higher order bit   Lower order bit→   * =Don't Care

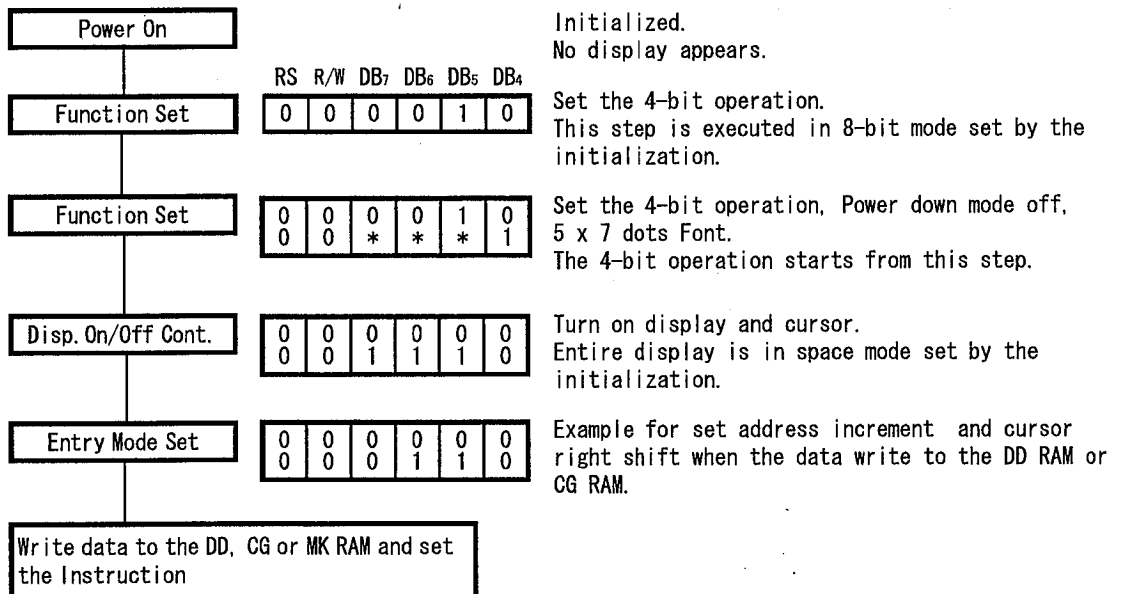(3-2) Initialization using the internal reset circuits

(a) 8-bit operation (Using internal reset circuits).

The Function set, Display On/Off Control and Entry Set Instruction must be executed before the data input, as shown below.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Power On											Initialized. No display appears.
Function Set	0	0	0	0	1	1	*	*	*	1	Set the 8-bit operation and Power down mode off.
Disp. On/Off Cont.	0	0	0	0	0	0	1	1	1	0	Turns on display and cursor. Entire display is in space mode set by the initialization.
Entry Mode Set	0	0	0	0	0	0	0	1	1	0	Example for set address increment and cursor right shift when the data write to the DD, CG or MK RAM.
Write data to the DD, CG or MK RAM and set the Instruction											

(b) 4-bit operation (Using internal reset circuits).

In the 4-bit operation, the function set must be performed by the user programming.
When the power is turned on, 8-bit operation is selected automatically, therefore the first input is performed under 8-bit operation. In this operation, full instruction can not input because of terminals DB0 to DB3 are no connection. Therefore, same instruction must be rewritten on the RS, R/W and DB7 to DB4, as shown below. Since one operation is completed by the two accesses in the 4-bit operation mode, rewrite is required to set the instruction code in full.

	RS	R/W	DB7	DB6	DB5	DB4	
Power On							Initialized. No display appears.
Function Set	0	0	0	0	1	0	Set the 4-bit operation. This step is executed in 8-bit mode set by the initialization.
Function Set	0	0	0	0	1	0	Set the 4-bit operation, Power down mode off, 5 x 7 dots Font.
	0	0	*	*	*	1	The 4-bit operation starts from this step.
Disp. On/Off Cont.	0	0	0	0	0	0	Turn on display and cursor. Entire display is in space mode set by the initialization.
	0	0	1	1	1	0	
Entry Mode Set	0	0	0	0	0	0	Example for set address increment and cursor right shift when the data write to the DD RAM or CG RAM.
	0	0	0	1	1	0	
Write data to the DD, CG or MK RAM and set the Instruction							

Note : When the Icon display function using, the system should be initialized by software initialization.

(3-3) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6620 must be initialized by the instruction.

(a) Initialization by Instruction in 8-bit interface length.

Step	Initialized. No display appears.
Power On	Initialized. No display appears.
Wait more than 7ms after VDD rises to 2.4V	

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Function Set	0	0	0	0	1	1	*	*	*	*	Function Set (8-bit interface length)
Wait more then 3.0ms											
Function Set	0	0	0	0	1	1	*	*	*	*	Function Set (8-bit interface length)
Wait more then 200μs											
Function Set	0	0	0	0	1	1	*	*	*	*	Function Set (8-bit interface length)

Busy Flag (BF) can not be checked before this step, but it can be checked after this step. After this step, busy flag (BF) check or longer waiting time than each instruction execution time is required.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Function Set	0	0	0	0	1	1	*	*	*	1	Set the 8-bit operation and Powerdown mode off.
Display Off	0	0	0	0	0	0	1	0	0	0	
Display Clear	0	0	0	0	0	0	0	0	0	1	
Entry Mode Set	0	0	0	0	0	0	0	1	1	0	Example for set address increment and cursor right shift when the data write to the DD, CG or MK RAM.

Write data to the DD, CG or MK RAM and set the Instruction

Note : When the Icon display function using, the system should be initialized by software initialization.

(b) Initialization by Instruction in 4-bit interface length

```
┌──────────────────────┐
│       Power On        │          Initialized.
└──────────────────────┘          No display appears.
           │
┌──────────────────────┐
│ Wait more than 7ms after │
│ VDD rises to 2.4V     │
└──────────────────────┘
           │              RS  R/W DB7 DB6 DB5 DB4
┌──────────────────────┐  ┌──┬──┬──┬──┬──┬──┐
│    Function Set       │  │ 0│ 0│ 0│ 0│ 1│ 1│  Function Set
└──────────────────────┘  └──┴──┴──┴──┴──┴──┘  (8-bit interface length )
           │
┌──────────────────────┐
│  Wait more then 3.0ms │
└──────────────────────┘
           │
┌──────────────────────┐  ┌──┬──┬──┬──┬──┬──┐
│    Function Set       │  │ 0│ 0│ 0│ 0│ 1│ 1│  Function Set
└──────────────────────┘  └──┴──┴──┴──┴──┴──┘  (8-bit interface length )
           │
┌──────────────────────┐
│ Wait more then 200μs  │
└──────────────────────┘
           │
┌──────────────────────┐  ┌──┬──┬──┬──┬──┬──┐
│    Function Set       │  │ 0│ 0│ 0│ 0│ 1│ 1│  Function Set
└──────────────────────┘  └──┴──┴──┴──┴──┴──┘  (8-bit interface length )
```

Function Set (8-bit interface length)
Busy Flag (BF) can not be checked before this step, but it can be checked after this step. After this step, busy flag (BF) check or longer waiting time than each instruction execution time is required.

```
┌──────────────────────┐  ┌──┬──┬──┬──┬──┬──┐
│    Function Set       │  │ 0│ 0│ 0│ 0│ 1│ 0│  Function Set
└──────────────────────┘  └──┴──┴──┴──┴──┴──┘  Set 4-bit interface length by 8-bit inter-
           │                                    face length.
┌──────────────────────┐  ┌──┬──┬──┬──┬──┬──┐
│    Function Set       │  │ 0│ 0│ 0│ 0│ 1│ 0│  Set the 4-bit operation and Powerdown mode
└──────────────────────┘  │ 0│ 0│ *│ *│ *│ 1│  off.
           │              └──┴──┴──┴──┴──┴──┘
┌──────────────────────┐  ┌──┬──┬──┬──┬──┬──┐
│    Display Off        │  │ 0│ 0│ 0│ 0│ 0│ 0│
└──────────────────────┘  │ 0│ 0│ 1│ 0│ 0│ 0│
           │              └──┴──┴──┴──┴──┴──┘
┌──────────────────────┐  ┌──┬──┬──┬──┬──┬──┐
│    Display Clear      │  │ 0│ 0│ 0│ 0│ 0│ 0│
└──────────────────────┘  │ 0│ 0│ 0│ 0│ 0│ 1│
           │              └──┴──┴──┴──┴──┴──┘
┌──────────────────────┐  ┌──┬──┬──┬──┬──┬──┐
│    Entry Mode Set     │  │ 0│ 0│ 0│ 0│ 1│ 0│  Example for set address increment and cursor
└──────────────────────┘  │ 0│ 0│ 0│ 1│ 1│ 0│  right shift when the data write to the DD, CG
           │              └──┴──┴──┴──┴──┴──┘  or DD RAM.
           │
┌──────────────────────┐
│ Write data to the DD, CG or MK RAM and set │
│ the Instruction       │
└──────────────────────┘
```

Note : When the Icon display function using, the system should be initialized by software initialization.

(4)Powerdown Function

NJU6620 incorporates the powerdown mode to decrease the operating current.
The powerdown mode can be set/reset by the function set instruction.
In the powerdown mode, all the character display (12-character 4-line) and icon display turn off and only the static display area operates automatically.
The status of internal circuits at the powerdown mode is shown below :

- Main oscillator stops operation and sub oscillator for the static display starts operations.
- Voltage converter, voltage regulator and buffer amplifire for the bleeder resistance stop the operation.
- The contents of DD RAM, CG RAM and MK RAM are kept.

(5)LCD display

(5-1)Power Supply for LCD Driving

NJU6620 incorporates Voltage converter (tripler or doubler) to generate the LCD driving high voltage, Voltage regulator to adjust the LCD driving voltage, Bleeder resistance and buffer amplifire.

(a)Voltage converter

· Voltage tripler

By connecting the capacitor between C1+ and C1−, C2+ and C2−, VSS and V5OUT respectively, two times negative voltage of VDD−VSS output from V5OUT.

· Voltage doubler

By connecting the capacitor between C2+ and C2−, VSS and V5OUT respectively, and connecting the C1+ terminal to C2+ terminal, and C1− terminal being open, negative voltage of VDD−VSS output from V5OUT.

$V_{DD}=+3V$
$V_{SS}=\pm0V$
$V_{5OUT}=-3V$

Voltage doubler

$V_{DD}=+3V$
$V_{SS}=\pm0V$
$V_{5OUT}=2V_{SS}=-6V$

Voltage tripler
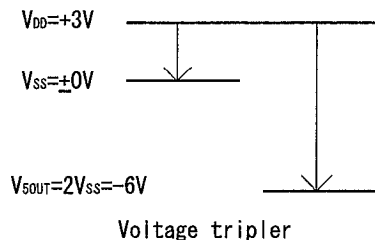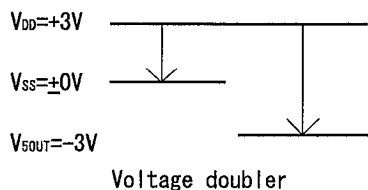
(b)Voltage Regulator

Voltage Regulator incorporates a non-inverting OP-AMP which supplied VDD and V5OUT, and a reference voltage source.
By stetting the VR level by connecting Ra and Rb, the regulator which amplifies VREF output the LCD driving voltage to the VREG terminal.
Therefore, the LCD operating voltage can be output between VDD and VREG by setting VREF and the external resistances Ra and Rb.

$$VREG=(1+Rb/Ra)\cdot VREF \quad where, \quad VDD=0V \quad and \quad |VREG|<|V5OUT|$$
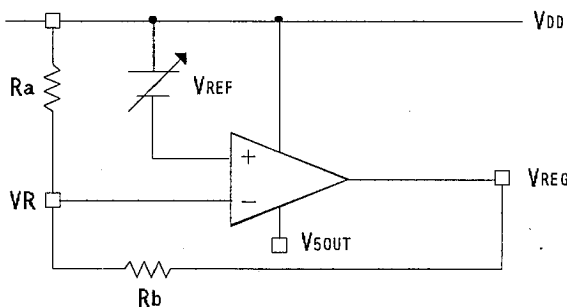
The contrast control function performs VREF value adjustment from 1st step to 16th step by a step setting when the 4-bit data write into the contrast control register by the instruction.

Note : Set the contrast control register to (00)H when the contrast control funcion is unused.
Use variable resistances to the external resistances Ra, Rb and a thermister if need due to the voltage reference VREF is changed by the lot and operating temperature.
Take care the Noise input on the VR terminal because of it designed in high impedance.
Short wiring or sealed wiring are required to avoid the noise input, if necessary.

[The Voltage Reference VREF characteristics]

Supply Voltage : VDD= 0V, VSS= -3V   Temperature : 25℃
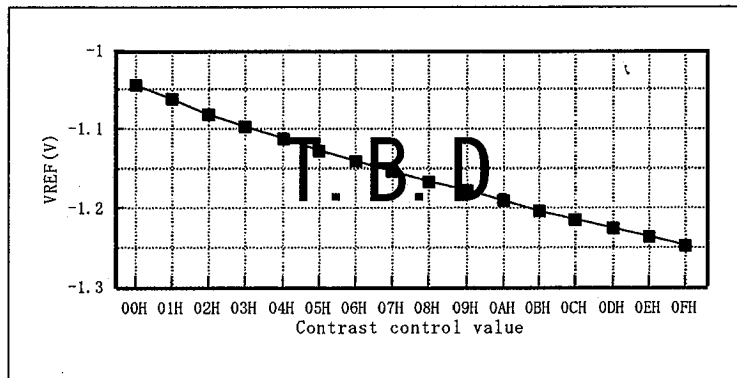
[The LCD Operating Voltage VREG characteristics]

Supply Voltage   : VDD= 0V, VSS= -3V   Voltage Tripler Output : V5OUT=-9V
External Resistances : Ra = 180KΩ, Rb = 820KΩ   Temperature   : 25℃

Used Equation   : VREG(xx)H = (1 + 820kΩ / 180kΩ) · VREF(xx)H
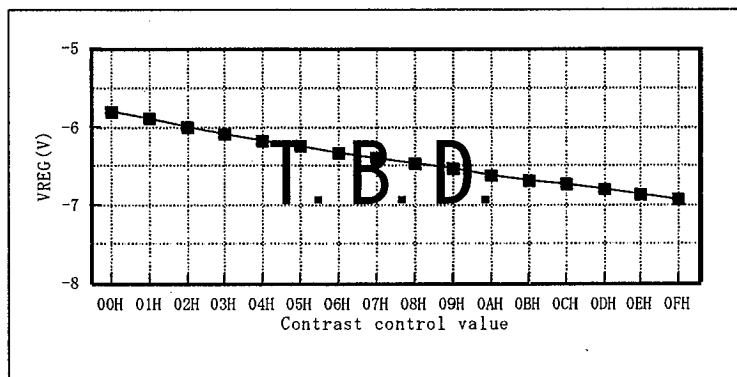
(c) Bleeder Resistance

Each LCD driving voltage (V1, V2, V3, V4) is generated by the high impedance bleeder resistance buffered by voltage follower OP-AMP to get a enough display characteristics with low operating current.

The bleeder resistance is set 1/7 bias suitable for 1/36 duty ratio and 5MΩ resistance in total. The capacitor connected between V5 and VDD is needed for stabilizing V5. The determination of the each capacitance of C1, C2 and C3 generating for LCD operating voltage, is required to operate with the LCD panel actually. The capacitance for the typical application is shown below :

LCD Driving Voltage vs Duty Ratio

Power supply	Duty Ratio	1/36
	Bias	1/7
	V_{LCD}	$V_{DD} - V_5$

VLCD is the maximum amplitude for LCD driving voltage.

RB1=714KΩ typ
RB2=2.14MΩ typ
RB=5.0MΩ typ

Bleeder Resistance and
Buffer Amplifire

Typical Capacitance :
C1, C2, C3, C4 = from 1.0 to 10uF
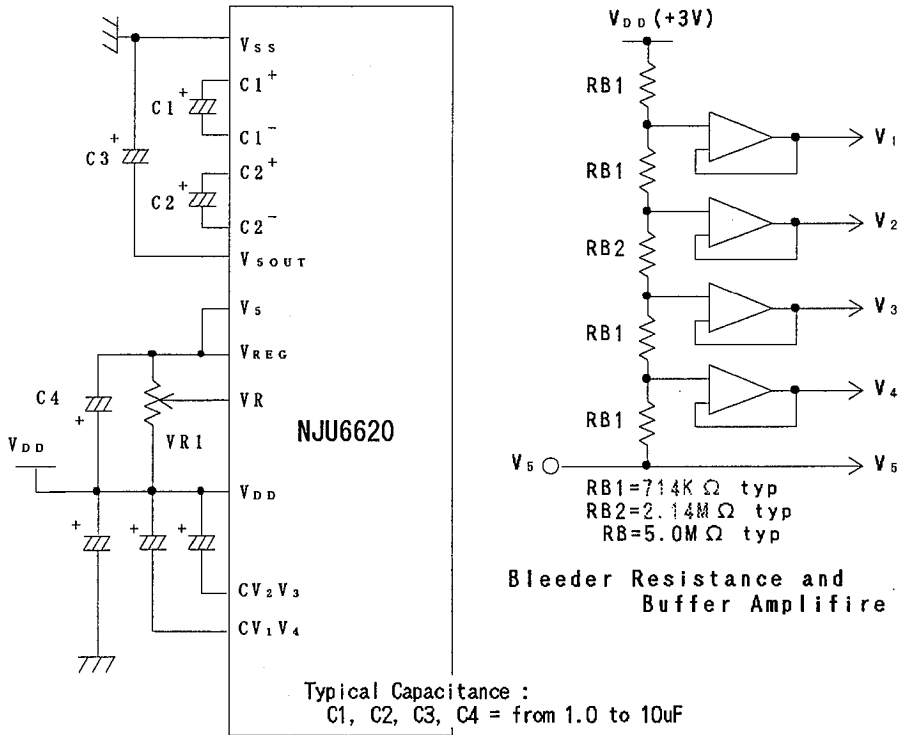
Typical application for LCD operating voltage generation

Note 1 : Take care the Noise input on the VR terminal as designed in high impedance. Short wiring or sealed wiring are required to avoid the noise input, if necessary.
Note 2 : The capacitor connected CV1V4 and CV2V3 terminals are required to operate with the LCD panel actually.

NJU6620

(5-2)Relation between oscillation frequency and LCD frame frequency

As the NJU6620 incorporate oscillation capacitor and resistor for CR oscillation, 192kHz oscillation is available without any external components.
The LCD frame frequency example mentioned below is based on ***kHz oscillation. (1clock = ****us)

1/36 duty ratio
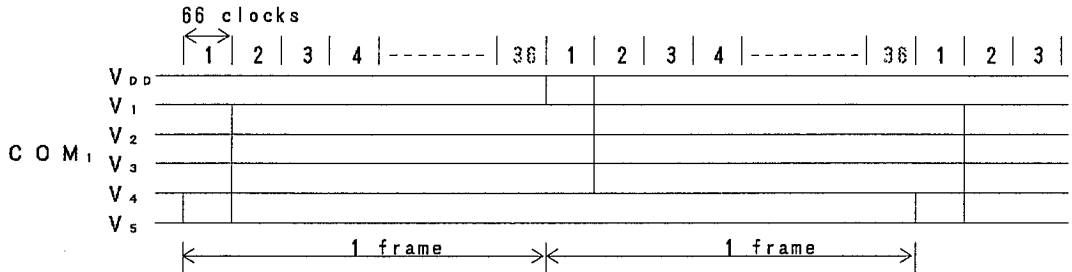
1 frame = 4.76(us) * 66 * 36 = 11.3(ms)
Frame frequency = 1 / 11.3(ms) = 88.5(Hz)

(6) Interface with MPU

Interface circuits of NJU6620 can be connected to serial or 4/8-bit parallel.
NJU6620 can be interfaced with both of 4/8-bit MPU and the two-time 4-bit or one-time 8-bit data transfer is available.

(6-1) 4-bit MPU interface

When the interface length is 4-bit, the data transfer is performed by 4 lines connected to DB4 to DB7 (DB0 to DB3 are not used). The data transfer with the MPU is completed by the two time 4-bit data transfer.

The data transfer is executed in the sequence of upper 4-bit (the data DB4 to DB7 at 8-bit length) and lower 4-bit (the data DB0 to DB3 at 8-bit length).

The busy flag check can be executed after two-time 4-bit data transfer (1 instruction execution by two-time transfer). In this case, the data of busy flag and address counter contents are also output twice.

(6-2) 8-bit MPU interface

RS			
R/W			
E			
Internal Status	operation		
DB7	Data Busy Busy No Busy Data		

| Writing Instruction Into Instruction Register(IR) | Busy Flag Check | Busy Flag Check | Busy Flag Check | Writing Instruction Into Instruction Register(IR) |
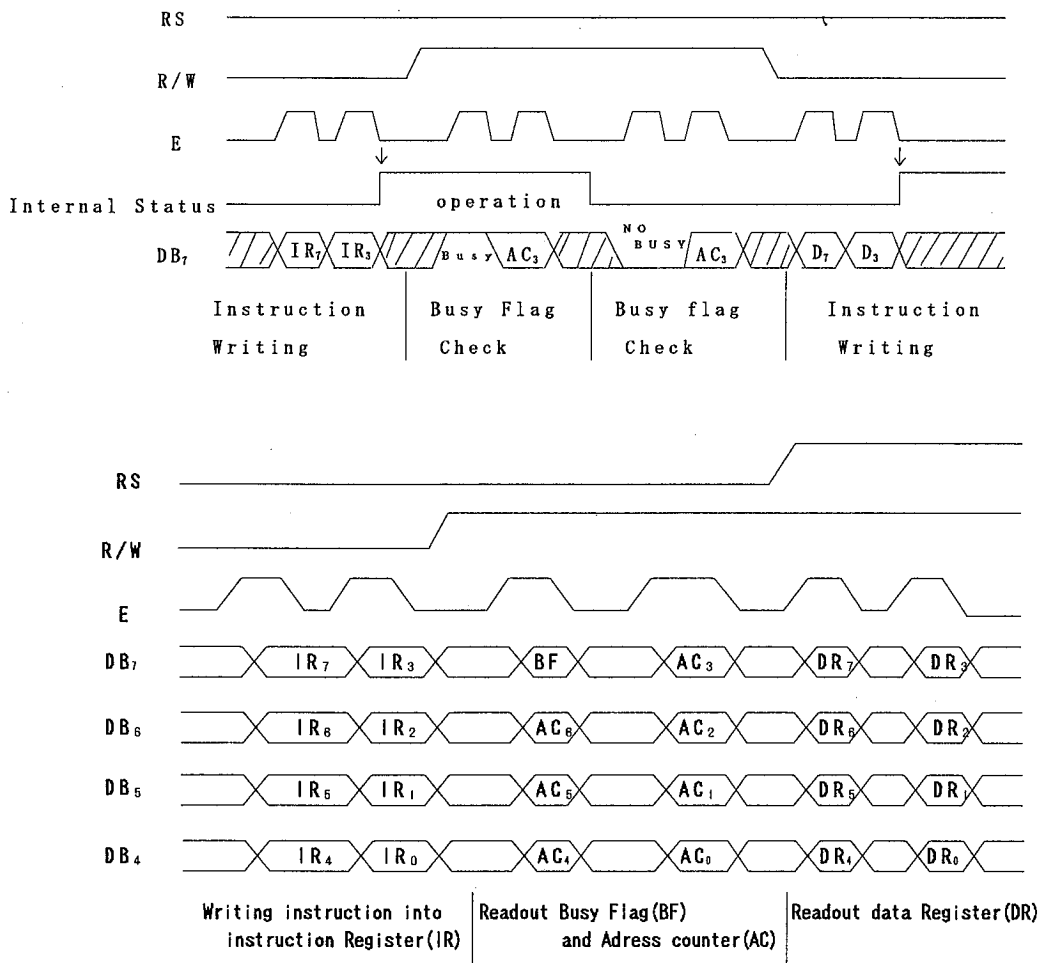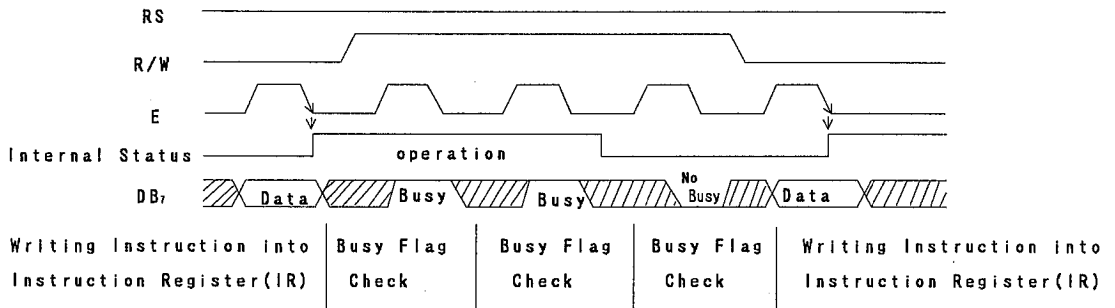
(6-3) Serial interface

Serial interface circuit is activated when the P/S terminal is set to "L" level then the chip select terminal (CS) goes to "L" level. The data input/output is MSB first like as the order of DB7, DB6 ···· DB0.

The input data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The shift register converted to parallel data at the CS rise edge input.

In case of entering over than 8-bit data, valid data is last 8-bit data.

The output data is exited from the shift register synchronized at the fall edge of the serial clock SCL.

The time chart for the serial interface is shown below.

Note : The level ("L" or "H") of RS and R/W terminals should be set before CS terminal goes to "L" level.
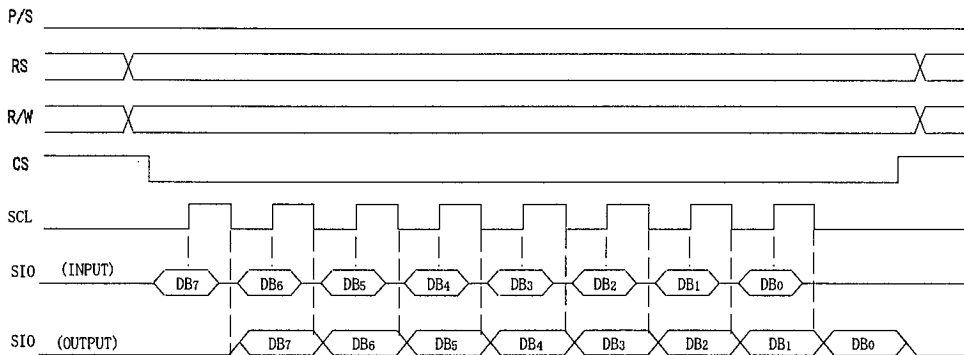
■ ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Supply Voltage (1)	V_{DD}	$-0.3 \sim +7.0$	V	
Supply Voltage (2)	V_{LCD}	$VDD-11.0 \sim VDD+0.3$	V	
Input Voltage	V_{IN}	$-0.3 \sim V_{DD}+0.3$	V	
Operating Temperature	Topr	$-30 \sim +80$	℃	
Storage Temperature	Tstg	$-55 \sim +125$	℃	

Note 1 : If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recomended for normal operation. Use beyond the electric characteristics conditions will cause mal function and poor reliability.
Note 2 : Decoupling capacitor should be connected between VDD and VSS due to the stabilized operation for the Voltage converter.
Note 3 : All voltage values are specified as VSS = 0V
Note 4 : The relation : VDD > VSS , VDD > VSS ≧ V5OUT, VSS=0V must be maintained.

■ ELECTRICAL CHARACTERISTICS (V_{DD}=2.4 ~ 3.3V、Ta=−20 ~ +75℃)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Operationg Voltage		V_{DD}		2.4	3.0	3.3	V	
Input Voltage		V_{IH}		$0.8V_{DD}$	—	V_{DD}	V	4
		V_{IL}		V_{SS}	—	$0.2V_{DD}$	V	5
Output Voltage		V_{OH}	$-I_{OH}$=0.205mA、V_{DD}=3V	2.0	—	—	V	6
		V_{OL}	I_{OL}=1.6mA、V_{DD}=3V	—	—	0.5	V	
Driver On-resist. (COM)		R_{COM}	$\pm I_d$=1μA (All COM term.)	—	—	20	kΩ	9
Driver On-resist. (SEG)		R_{SEG}	$\pm I_d$=1μA (All SEG term.)	—	—	30	kΩ	
Input Leakage Current		I_{LI}	V_{IN}=0~V_{DD}	−1	—	1	μA	7
Pull-up MOS Current		$-I_P$	V_{DD}=3V, (All DB terminals)	10	25	50	μA	
Operating Current		I_{DD1}	V_{DD}=3V f_{osc}=Internal Osc. V_5=−5V during display	T.B.D.			μA	8
		I_{DD2}	V_{DD}=3V f_{osc}=Internal Osc. during access, T_{CYCE}=5μs	T.B.D.			μA	
		I_{DD3}	V_{DD}=3V, f_{osc}=Internal Osc. during Powerdown mode	T.B.D.			μA	
Voltage Converter (Tripler)	Output Voltage	V_{5OUT}	V_{DD}=3V, Ta=25℃, I_{OUT}=100μA	—	−4.8	—	V	
	Voltage Efficiency	V_{ef}	R_L=∞	—	95.0	—	%	
Voltage Converter (Doubler)	Output Voltage	V_{5OUT}	V_{DD}=3V, Ta=25℃, I_{OUT}=100μA		−1.8	—	V	
	Voltage Efficiency	V_{ef}	R_L=∞		95.0	—	%	
Voltage Regulator	Reference Voltage	V_{REF}	Contrast Control (00)H. Ta=25℃	VDD−0.75	VDD−1.05	VDD−1.35	V	
	Output Voltage	V_{REG}	R_L=∞, V_{5OUT}=−6V, R_{RV}=1MΩ. Contrast Control (00)H		VDD−5.8			
Bleeder resistance		R_B	V_{DD}−V_5=3V	—	5	—	MΩ	
Oscillation Frequency		f_{osc}	V_{DD}=3V, Ta=25℃	135	212	289	kHz	
LCD Driving Voltage		V_{LCD}	V_{LCD}=V_{DD}−V_5	V_{DD}−5.0	—	V_{DD}−10.0	V	10
V5 Terminal Current		I_5	VDD=3V, V5=6V			200	μA	

Note 5 : Input/Output structure except LCD driver are shown below:
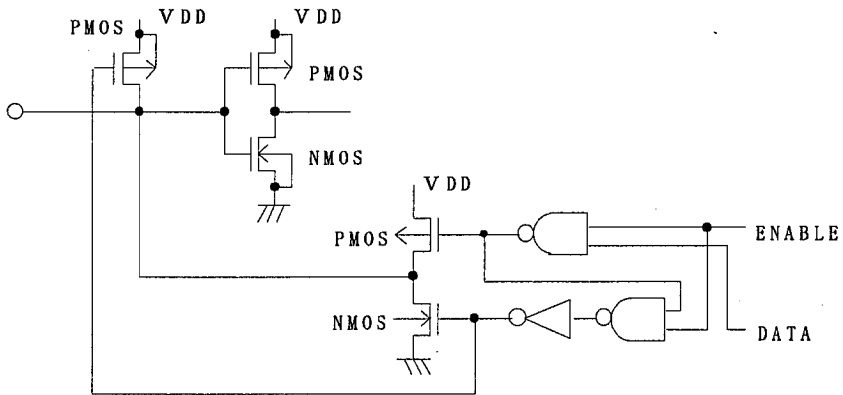
· Input Terminal Strucure
E/SCL, RS, R/W, P/S, SEL Terminals $\overline{RESET}$ Terminal
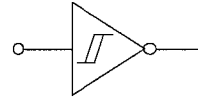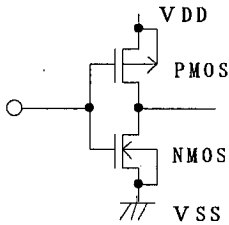
· Input/Output Terminal Structure
DB0 to DB7 Terminals

Note 6 : Apply to the Output and Input/Output Terminals.
Note 7 : Except pull-up resistance current and output driver current.
Note 8 : Except Input/output current but including the current flow on bleeder resistance.
If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L".

· Operating Current Measurement Circuit
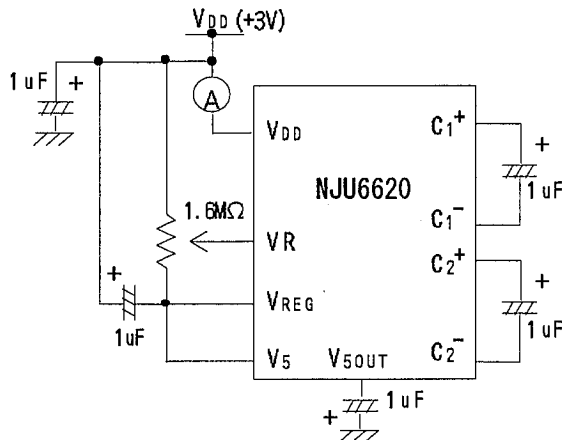
Note 9 : RCOM and RSEG are the resistance values between power supply terminals (VDD, V5OUT) and each common terminal (COM1 to COM32, COMMK1 to COMMK4) and suplly voltage (VDD, V5OUT) and each segment terminal (SEG1 to SEG60, SEGM1 and SEGM2) respectively, and measured when the current Id is flown on every common and segment terminals at a same time.

Note 10: Apply to the output voltage from each COM and SEG are less than ± 0.15V against the LCD driving constant voltage (VDD, V5OUT) at no load condition.

Voltage Tripler Measurement Circuit
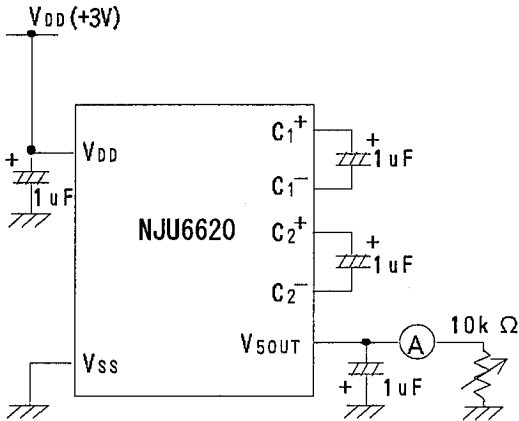
Voltage Doubler Measurement Circuit
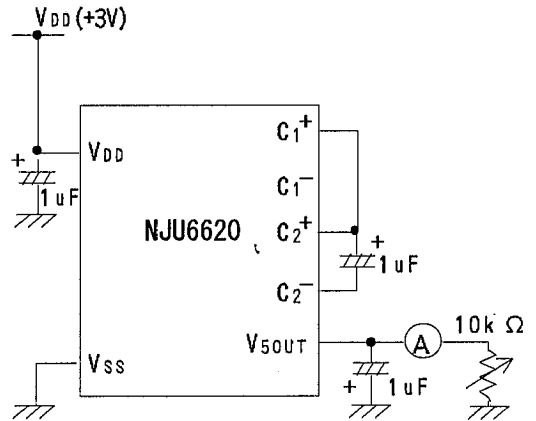
Voltage Tripler/Doubler
peration Clock Frequency = 10kHz

Bleeder Resistance
and Buffer Amplifire

NJU6620's Internal

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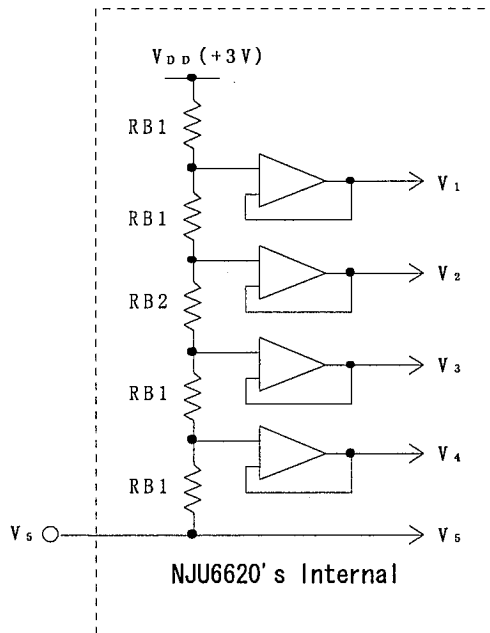
・Bus timing characteristics (VDD = 2.4 ~ 3.3V, VSS = 0V, Ta = −20 ~ +75℃)

Write operation (Write from MPU to NJU6620)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Enable cycle time		t_{CYCE}	1	—		μ s
Enable pulse width	"1" level	PW_{EH}	400	—		
Enable rise time, fall time		t_{Er}, t_{Ef}	—	20		
Set up time	RS, R/W, E	t_{AS}	200	—	fig. 1	
Address hold time		t_{AH}	200	—		ns
Data set up time		t_{DSW}	200	—		
Data hold Time		t_H	200	—		

Timing Characteristics (Write operation)
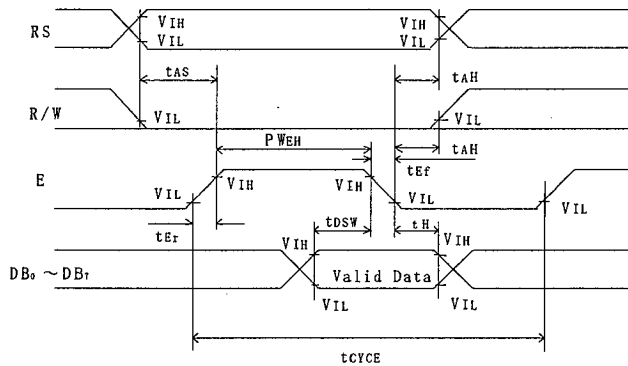
fig. 1

Read operation (Read from NJU6620 to MPU)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Enable cycle time		t_{CYCE}	1	—		μ s
Enable pulse width	"1" level	PW_{EH}	750	—		
Enable rise time, fall time		t_{Er}, t_{Ef}	—	20		
Set up time	RS, R/W, E	t_{AS}	200	—	fig. 2	
Address hold time		t_{AH}	200	—		ns
Data delay time		t_{DDR}	—	750		
Data hold time		t_{DHR}	200	—		

Load Condition of DB0 to DB7 : CL=100pF

Timing Characteristics (Read operation)
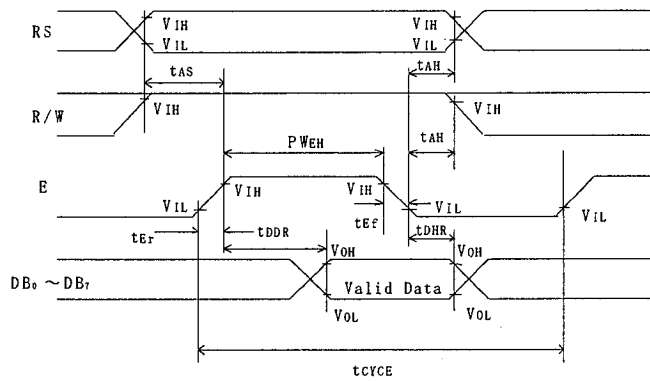
fig. 2

·Serial Interface Sequence

(V$_{DD}$=2.4 ~ 3.3V, V$_{SS}$=0V, Ta=−20 ~ +75℃)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Serial clock cycle time		t$_{CYCE}$	1	—		μs
Serial clock width	"1" level	t$_{SCH}$	300	—		
	"0" level	t$_{SCL}$	700	—		
Serial clock rise and fall Time		t$_{SCR}$, t$_{SCF}$	—	20		
Chip select pulse width		PW$_{CS}$	500	—		
Chip select set up time		t$_{CSU}$	200	—		
Chip select hold time		t$_{CH}$	200	—	fig.3	ns
Chip Select rise and fall Time		t$_{CSR}$, t$_{CSF}$	—	20		
Set up time	RS, R/W – CS	t$_{AS}$	200	—		
Address hold time	CS – RS, R/W	t$_{AH}$	200	—		
Serial input data set up time		t$_{SISU}$	200	—		
Serial input data hold time		t$_{SIH}$	200	—		
Serial output data delay time		t$_{SOD}$	—	700		
Serial output data hold time		t$_{SOH}$	200	—		

Serial Interface
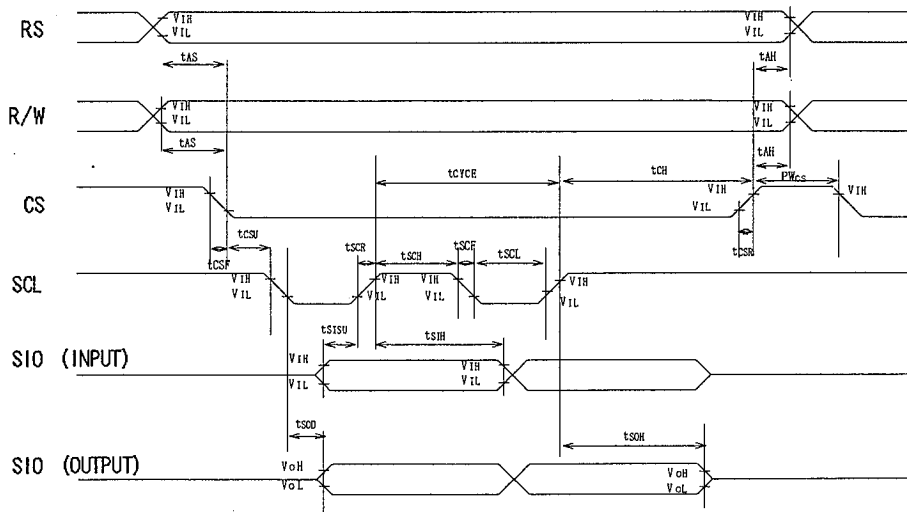
fig.3

・The Input Condition when using the Hardware Reset Circuit

Input timing
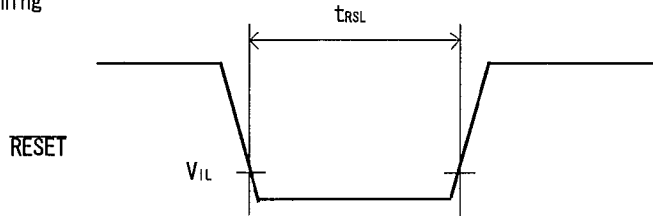
RESET

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Reset input "0" level width	t_{RSL}	f_{osc}=212kHz	1.2	—	—	ms

・Power Supply Condition when using the internal initialization circuit(Ta = −20 ～ +75℃)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Power supply rise time	t_{rDD}	—	0.1	—	5	ms
Power supply OFF time	t_{OFF}	—	1	—	—	ms

Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction. (Refer to initialization by the instruction)
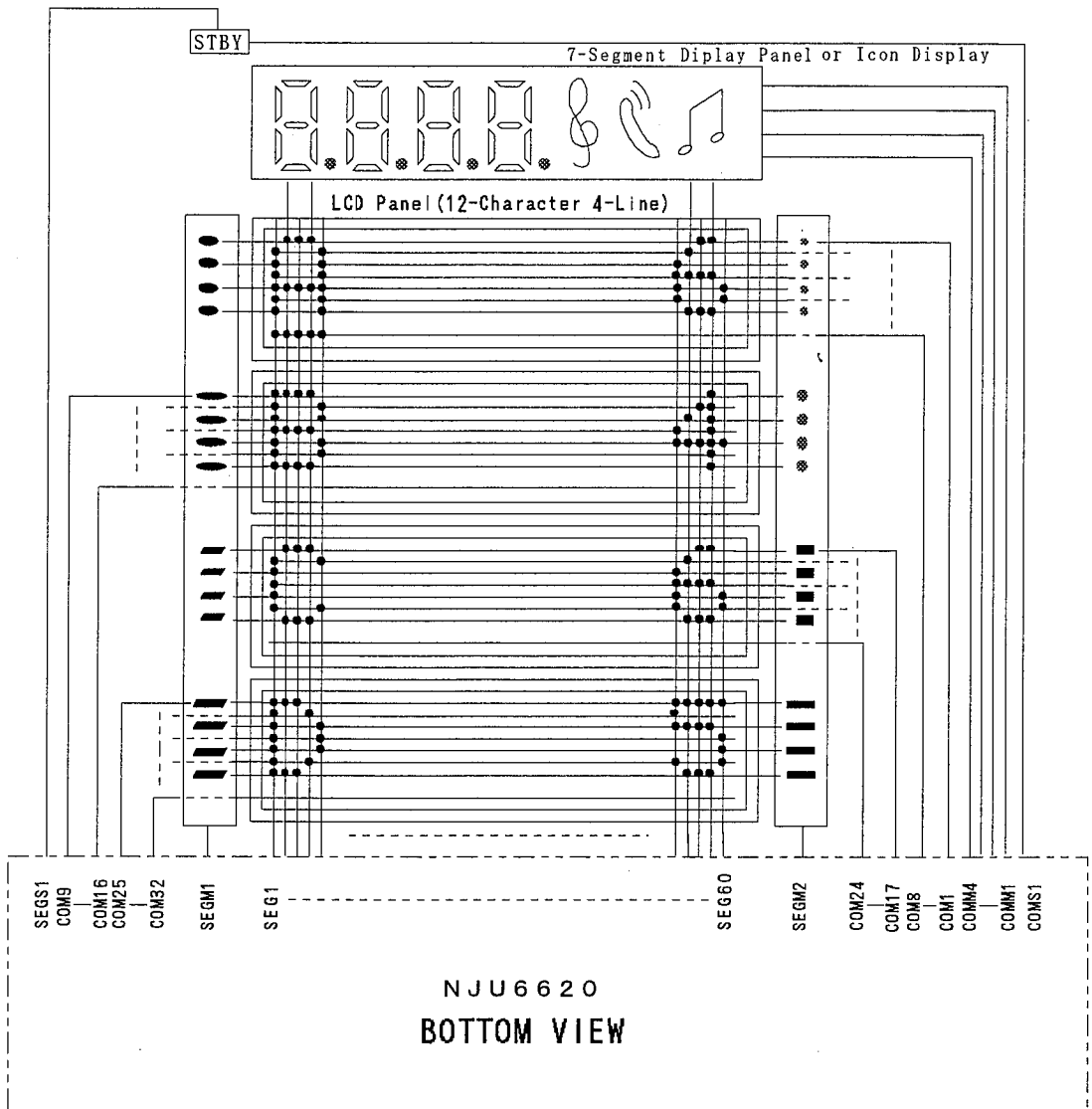

$0.1ms \leqq t_{rDD} \leqq 5ms$ $t_{OFF} \geqq 1ms$
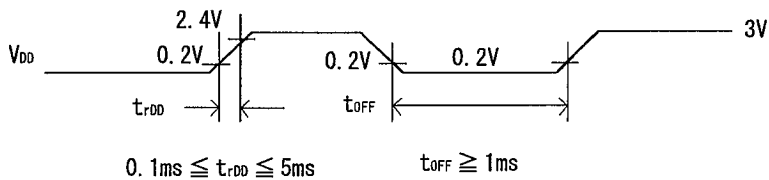
tOFF specifies the power off time in a short period off or cyclical on/off.

■ LCD DRIVING WAVE FORM

1/36 Duty Driving
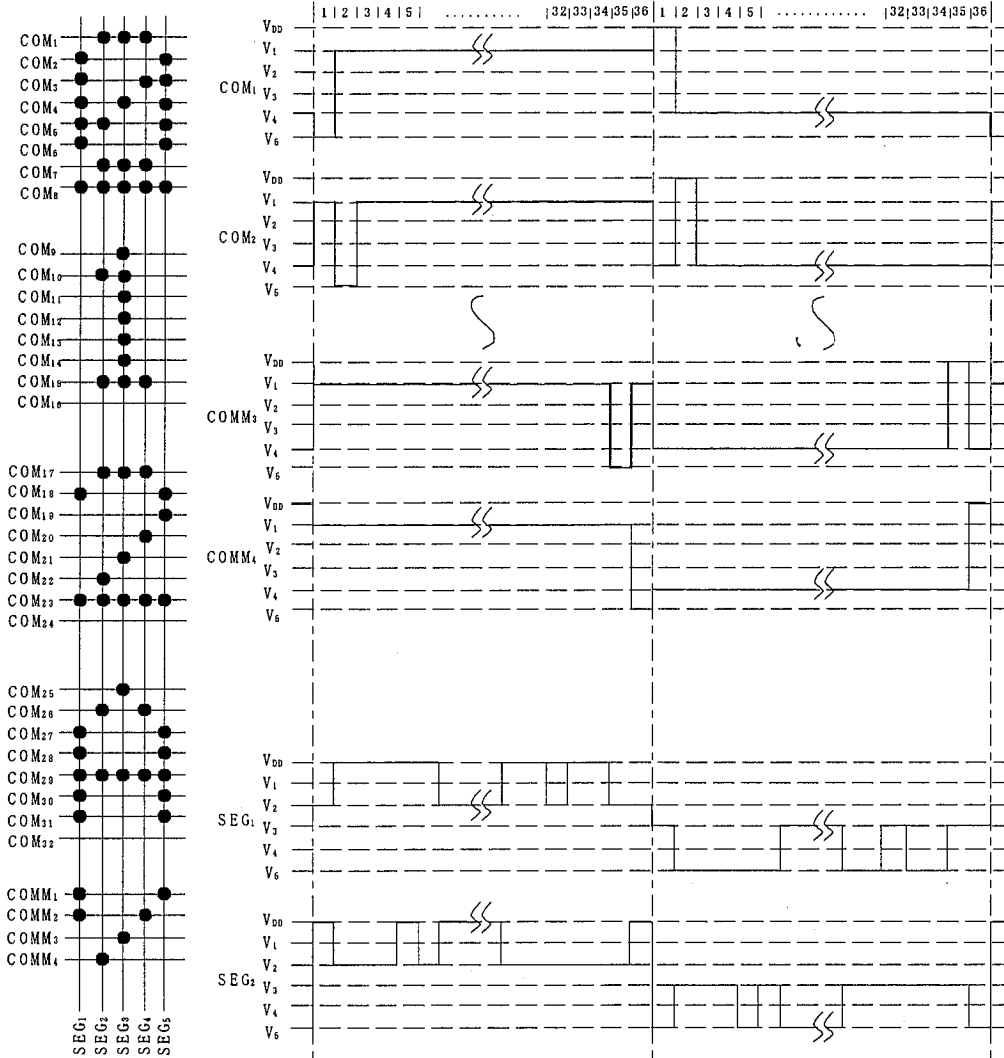
■ APPLICATION CIRCUITS (1)

STBY

7-Segment Diplay Panel or Icon Display

LCD Panel (12-Character 4-Line)

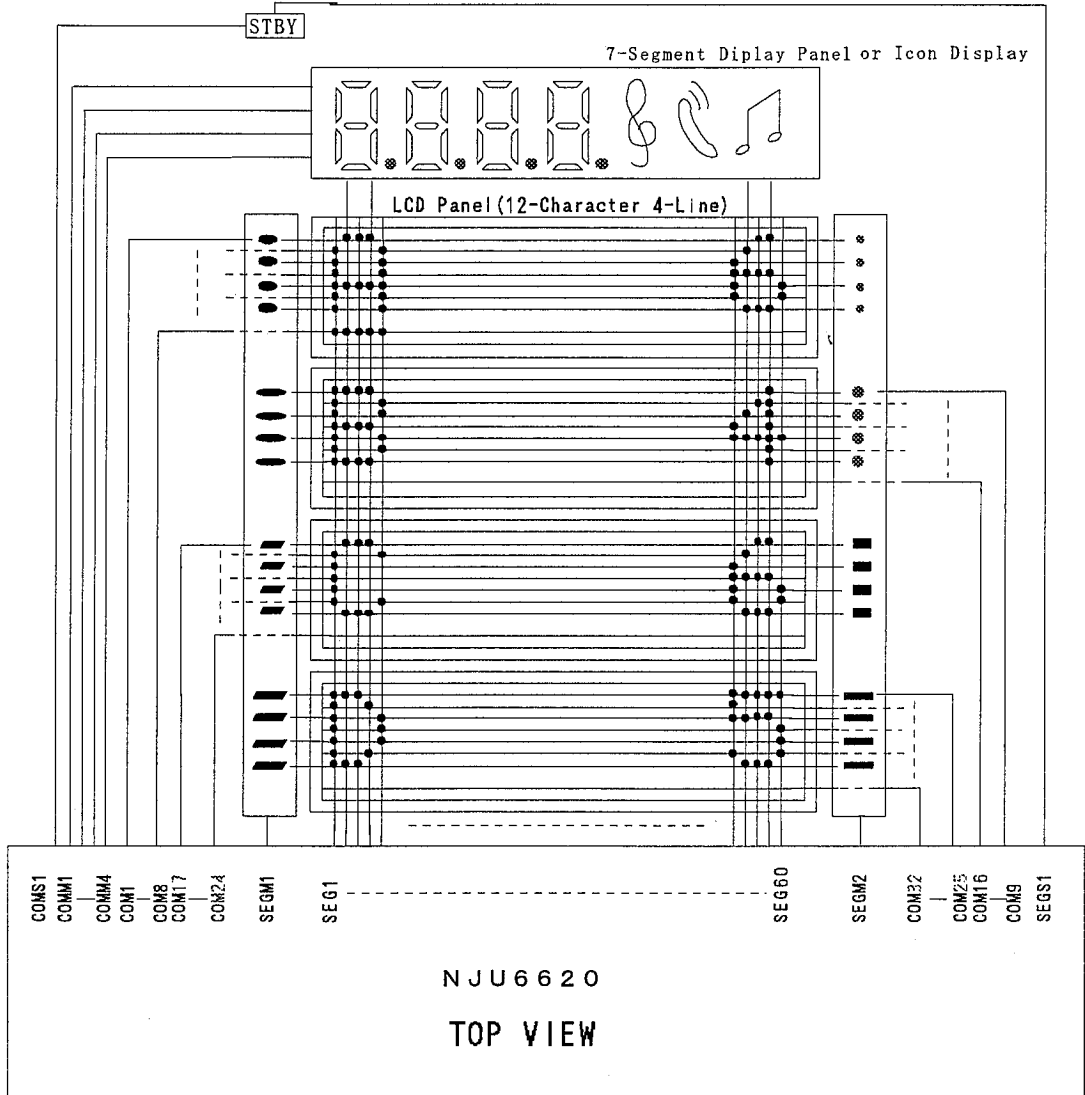SEGS1 COM9 COM16 COM25 COM32 SEGM1 SEG1 ---- SEG60 SEGM2 COM24 COM17 COM8 COM1 COMM4 COMM1 COMS1

NJU6620

BOTTOM VIEW

12-character 4-line Display Example
(The terminal description is "Mode A".)

■ APPLICATION CIRCUITS (2)

12-character 4-line Display Example
(The terminal description is "Mode B".)

New Japan Radio Co.,Ltd.

MEMO