PRELIMINARY

1/4 DUTY LCD DRIVER

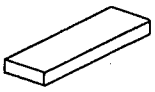
■ GENERAL DESCRIPTION

The NJU6439 is a 1/4 duty LCD driver for segment type LCD panel.

The LCD driver consists of 4-common and 40-segment drives up to 160 segments.

The rectangle outline is useful the COG applications.

■ PACKAGE OUTLINE



■ FEATURES

NJU6439C

- 40 Segment Drivers
- Duty and Bias Ratio : 1/4Duty, 1/3Bias (up to 160 segments)
- Serial Data Transmission (Shift Clock 2MHz max.)
- Oscillation Circuit On-chip
- Display Off Function (INH Terminal)
- Operating Voltage — 2.4~3.6V
- LCD Driving Voltage — 6.0V Max.
- Package Outline — Chip / Bumped Chip
- C-MOS Technology

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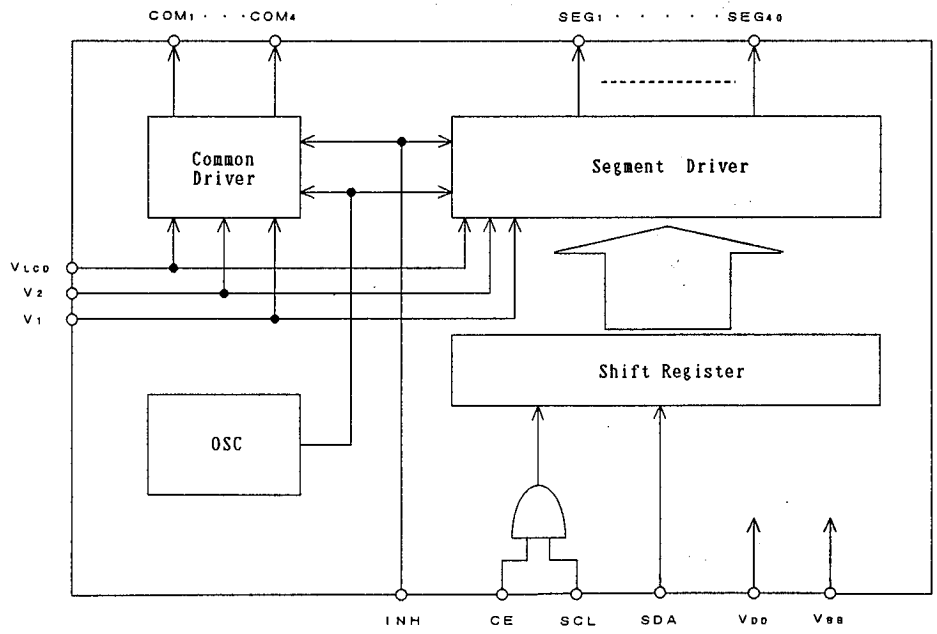
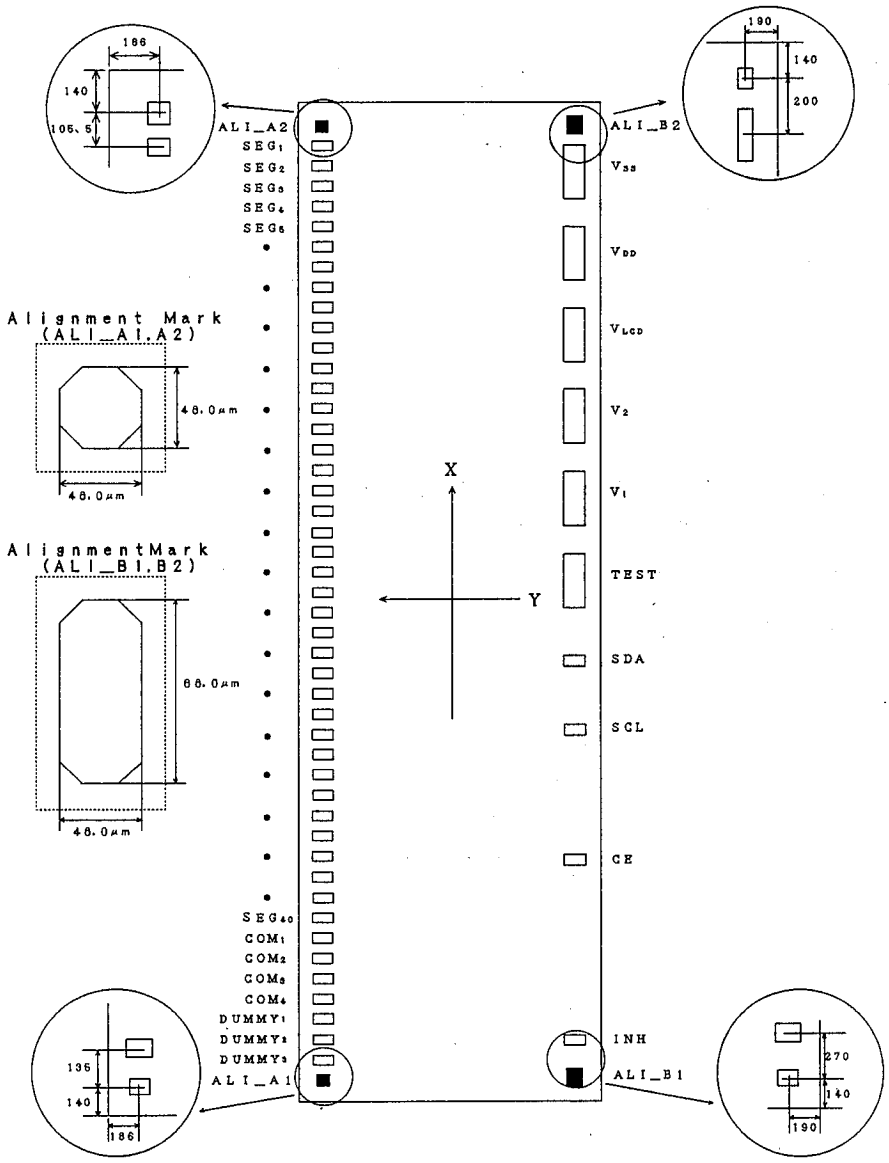
■ BLOCK DIAGRAM



■ PAD LOCATION



Chip size : 5.12mm x 1.56mm
Chip center : X=0μm, Y=0μm
Chip thickness : 400±30μm
Pad size : 50μm x 100μm
V_1, V_2, V_{LCD}, V_{DD}, V_{SS} Terminal is 250μm x 100μm
Bump height : 25μmTYP.
Bump material : Au

■:4th Mark is the Alignment Mark.

The Alignment Mark is useful the COG Asembly.

■ COORDINATES

Chip Size 5.12x1.56mm(Chip Center X=0μm, Y=0μm)

No	PAD NAME	X=(μm)	Y=(μm)	No	PAD NAME	X=(μm)	Y=(μm)
1	INH	-2150.0	- 590.0	32	SEG_{22}	214.5	594.0
2	CE	-1240.0	- 590.0	33	SEG_{23}	114.5	594.0
3	SCL	- 494.0	- 590.0	34	SEG_{24}	14.5	594.0
4	SDA	- 178.0	- 590.0	35	SEG_{25}	- 85.5	594.0
5	TEST	206.0	- 590.0	36	SEG_{26}	- 185.5	594.0
6	V_1	660.0	- 590.0	37	SEG_{27}	- 285.5	594.0
7	V_2	1040.0	- 590.0	38	SEG_{28}	- 385.5	594.0
8	V_{LCD}	1430.0	- 590.0	39	SEG_{29}	- 485.5	594.0
9	V_{DD}	1820.0	- 590.0	40	SEG_{30}	- 585.5	594.0
10	V_{SS}	2220.0	- 590.0	41	SEG_{31}	- 685.5	594.0
11	SEG_1	2314.5	594.0	42	SEG_{32}	- 785.5	594.0
12	SEG_2	2214.5	594.0	43	SEG_{33}	- 885.5	594.0
13	SEG_3	2114.5	594.0	44	SEG_{34}	- 985.5	594.0
14	SEG_4	2014.5	594.0	45	SEG_{35}	-1085.5	594.0
15	SEG_5	1914.5	594.0	46	SEG_{36}	-1185.5	594.0
16	SEG_6	1814.5	594.0	47	SEG_{37}	-1285.5	594.0
17	SEG_7	1714.5	594.0	48	SEG_{38}	-1385.5	594.0
18	SEG_8	1614.5	594.0	49	SEG_{39}	-1485.5	594.0
19	SEG_9	1514.5	594.0	50	SEG_{40}	-1585.5	594.0
20	SEG_{10}	1414.5	594.0	51	COM_1	-1685.5	594.0
21	SEG_{11}	1314.5	594.0	52	COM_2	-1785.5	594.0
22	SEG_{12}	1214.5	594.0	53	COM_3	-1885.5	594.0
23	SEG_{13}	1114.5	594.0	54	COM_4	-1985.5	594.0
24	SEG_{14}	1014.5	594.0	55	DUMMY1 ※	-2085.5	594.0
25	SEG_{15}	914.5	594.0	56	DUMMY2 ※	-2185.5	594.0
26	SEG_{16}	814.5	594.0	57	DUMMY3 ※	-2285.5	594.0
27	SEG_{17}	714.5	594.0	ALI_A1		-2420.0	594.0
28	SEG_{18}	614.5	594.0	ALI_A2		2420.0	594.0
29	SEG_{19}	514.5	594.0	ALI_B1		-2420.0	- 590.0
30	SEG_{20}	414.5	594.0	ALI_B2		2420.0	- 590.0
31	SEG_{21}	314.5	594.0	—		—	—

※DUMMY PAD

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■ TERMINAL DESCRIPTION

NO.	SYMBOL	F U N C T I O N
1	INH	Display-Off Control Terminal : When display goes to off, the display data in the shift-register is retained. "H" : Display-Off "L" : Display-On
2	CE	Chip Enable Signal Input Terminal : "H" : LCD display data "L" : Disable
3	SCL	Serial Data Transmission Clock Input Terminal : LCD display data are input synchronized SCL clock signal rise edge.
4	SDA	Serial Data Input Terminal Data input timing : SCL clock rise edge
6	V_1	LCD Driver Voltage Adjust Terminal
7	V_2	LCD Driver Voltage Adjust Terminal
8	V_{LCD}	Power Supply for LCD Driving
9	V_{DD}	Power Supply (+3V)
10	V_{SS}	Power Supply (0V)
11～50	SEG_1 ～ SEG_{40}	LCD Segment Output Terminals
51～54	COM_1 ～ COM_4	LCD Common Output Terminals

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■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuit :

This circuits supply the basical clock signal to other circuits like as common driver and segment driver.

(1-2) Shift-Register

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.

(1-3) Common Divider Circuit

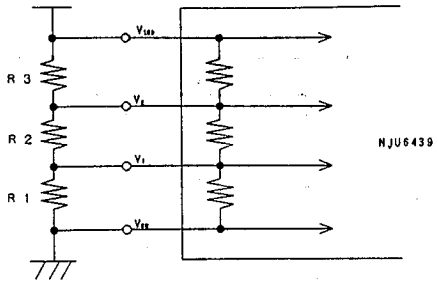
This circuit divides the oscillating signal to generate the common timing.

(1-4) Segment Divider Circuit

This circuit divides the oscillating signal to generate the segment timing.

(1-5) The LCD Driver Voltage Adjust circuit

The incorprate Bleeder Resistance sets 1/3 bias, and LCD Driver ability can be increased by connecting external resistance.



(2) Display Data input timing, correspond to segment and common terminal

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.
When the power is turned on, whole data in the shift-resister are "L".

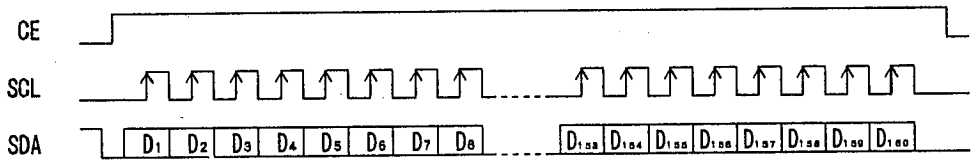
※ Whole 160bits data transfer to the shift register.When the input data in less than 160bits, parts which bit data is inputed corresponded to display,and segment which correspond to the rest part in "off".
In care of over then 160bits,front 160bits from fall edge of "CE"signal is valid.

- Input data correspond to Segment Status

The "H" input data correspond to segment "ON" and "L" correspond to "OFF".

Data (D1···D160)	Segment Status
"H"	ON
"L"	OFF

- Display Data Correspond to Segment Status



・Input data correspond to Segment Status
The "H" input data correspond to segment "ON" and "L" correspond to "OFF".

Data (D1・・・D160)	Segment Status
"H"	ON
"L"	OFF

・Display Data Correspond to Segment and Common Terminals

Segment	Data	COM_1	COM_2	COM_3	COM_4
SEG_1	D_1 D_2 D_3 D_4	○	○	○	○
SEG_2	D_5 D_6 D_7 D_8	○	○	○	○
⋮	⋮	⋮	⋮	⋮	⋮
SEG_{39}	D_{153} D_{154} D_{155} D_{156}	○	○	○	○
SEG_{40}	D_{157} D_{158} D_{159} D_{160}	○	○	○	○

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Operating Voltage (1)	V_{DD}	-0.3 ~ +7.0	V
Operating Voltage (2)	V_{LCD}	-0.3 ~ +7.0	V
Operating Voltage (3)	V_1, V_2	-0.3 ~ +7.0	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD}	V
Operating Temperature	T_{opr}	-20 ~ +75	°C
Storage Temperature	T_{stg}	-55 ~ +125	°C

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.
Note 2) All voltage values are specified as V_{SS} = 0 V
Note 3) The relation: $V_{LCD} \geqq V_2 \geqq V_1 \geqq V_{SS}$ must be maintained.
Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation.

■ ELECTRICAL CHARACTERISTICS

· DC Characteristics

(Ta=25°C, V_{DD}=3.0V, V_{SS}=0V, V_{LCD}=6.0V)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
Operating Voltage (1)	Recommend	V_{DD}	V_{DD} Terminal	2.4	3.0	3.6	V	
	Available	V_{DD}	V_{DD} Terminal	2.4	3.0	5.5	V	
Operating Voltage (2)		V_{LCD}	V_{LCD} Terminal	2.0		6.0	V	
Operating Voltage (3)		V_2	V_2 Terminal	V_1	$2/3V_{LCD}$	V_{LCD}	V	
Operating Voltage (4)		V_1	V_1 Terminal	0.7	$1/3V_{LCD}$	V_2	V	
"H" Input Voltage		V_{IH}	CE, SCL, SDA, INH Terminals	$0.7V_{DD}$		V_{DD}	V	
"L" Input Voltage		V_{IL}	CE, SCL, SDA, INH Terminals	V_{SS}		$0.3V_{DD}$	V	
"H" Input Current		I_{IH}	CE, SCL, SDA, INH Terminals $V_{IN}=V_{DD}$			5	μA	
"L" Input Current		I_{IL}	CE, SCL, SDA, INH Terminals $V_{IN}=V_{SS}$			5	μA	
"H" Output Voltage(1)		$V_{OH(1)}$	SEG_1~SEG_{40} Term., I_O= -1μA	V_{LCD}-0.6			V	5
"L" Output Voltage(1)		$V_{OL(1)}$	SEG_1~SEG_{40} Term., I_O= 1μA			V_{DD}+0.6	V	5
Middle Level Voltage 1/3 (1)		$V_{MS1/3}$	SEG_1~SEG_{40} Term., I_O=±1μA	$1/3V_{LCD}$ -0.6	$1/3V_{LCD}$	$1/3V_{LCD}$ +0.6	V	5
Middle Level Voltage 2/3 (1)		$V_{MS2/3}$	SEG_1~SEG_{40} Term., I_O=±1μA	$2/3V_{LCD}$ -0.6	$2/3V_{LCD}$	$2/3V_{LCD}$ +0.6	V	5
"H" Output Voltage(2)		$V_{OH(2)}$	COM_1~COM_4 Term., I_O= -30μA	V_{LCD}-0.6			V	6
"L" Output Voltage(2)		$V_{OL(2)}$	COM_1~COM_4 Term., I_O= 30μA			V_{SS}+0.6	V	6
Middle Level Voltage 1/3 (2)		$V_{MC1/3}$	COM_1~COM_4 Term., I_O= ±1μA	$1/3V_{LCD}$ -0.6	$1/3V_{LCD}$	$1/3V_{LCD}$ +0.6	V	6
Middle Level Voltage 2/3 (2)		$V_{MC2/3}$	COM_1~COM_4 Term., I_O= ±1μA	$2/3V_{LCD}$ -0.6	$2/3V_{LCD}$	$2/3V_{LCD}$ +0.6	V	6
"L" Output Voltage(3)		$V_{OL(3)}$	SDA I_O= 30mA			V_{SS}+0.4	V	6
Operating Current (1)		I_{DD}	V_{DD} Terminal V_{DD}=3.0V V_{LCD} OPEN		15	25	μA	7
Operating Current (2)		I_{LCD}	V_{LCD} Terminal V_{DD}=3.0V V_{LCD}=6.0V		18	28	μA	8
Hysteresis Voltage		V_H	SCL Terminal, V_{DD}=3.0V	0.3			V	
Terminal Capacitor		C_H	SCL, SDA Terminal Except measurement terminal are open.			10	pF	

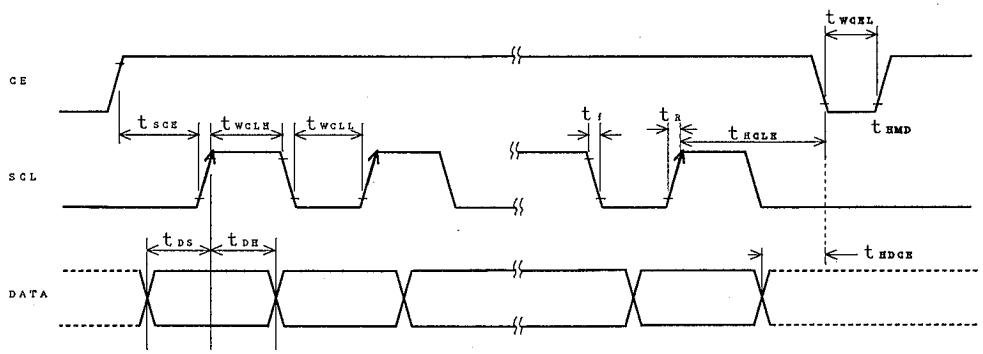
Note 5) Segment terminals except measurement terminal are open.
Note 6) Common terminals except measurement terminal are open.
Note 7) CE, SCL, SDA terminals are conected V_{SS}./INH teiminal is conected V_{DD}./TEST terminal is open.
Note 8) CE, SCL, SDA, INH terminals are measurement terminal are conected V_{SS}./TEST terminal is open.

・AC Characteristics

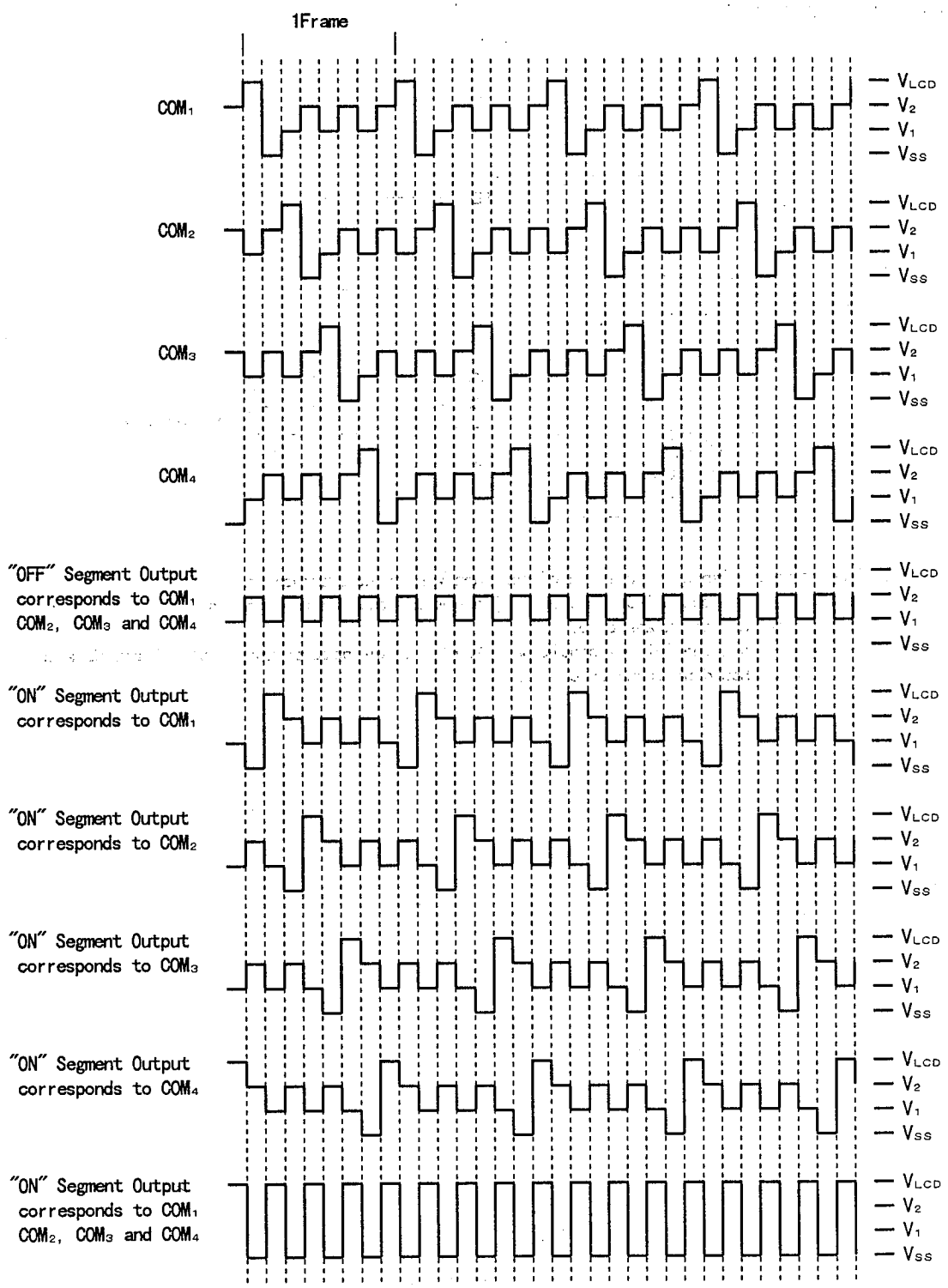
(Ta=25°C, V_{DD}=3.0V, V_{SS}=0V, V_{LCD}=6.0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	t_{WCLL}	SCL	0.25	—	—	μs
"H" Clock Pulse Width	t_{WCLH}	SCL	0.25	—	—	μs
SCL Rise Time	t_R	SCL	—	—	50	ns
SCL Fall Time	t_H	SCL	—	—	50	ns
SDA Data Set-up Time	t_{DS}	SDA, SCL	0.25	—	—	μs
SDA Data Hold Time	t_{DH}	SCL	0.25	—	—	μs
CE Set-up Time	t_{SCE}	CE, SDA	1.25	—	—	μs
CE Hold Time(1)	t_{HDCE}	SE, SDA	1.00	—	—	μs
CE Hold Time(2)	t_{HCLE}	SCL, CE	1.25	—	—	μs
"L" CE Pulse Width	t_{WCEL}	CE	4.00	—	—	μs
Frame Frequency	f_o	COM_1～COM_4, SEG_1～SEG_{40}	45	70	—	

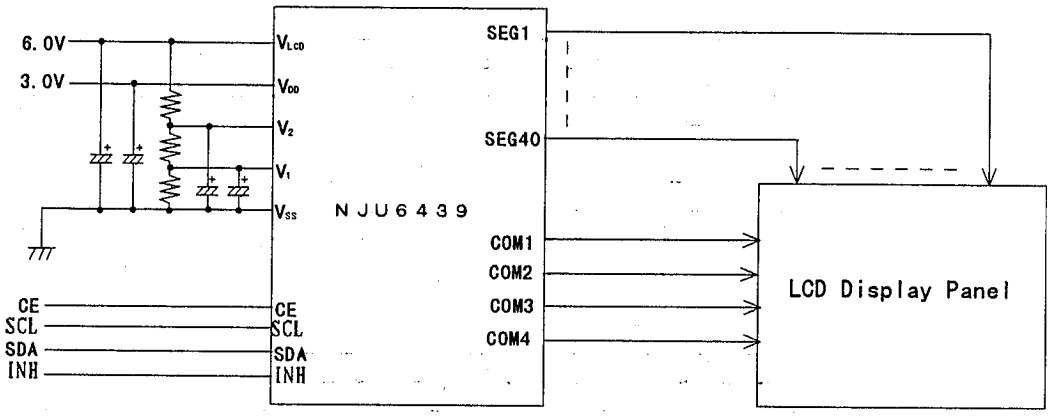
・Input Timing Characteristics



■ LCD Driving Waveform(1/4DUTY・1/3BIAS)



■ APPLICATION CIRCUIT



(Note) The internal display data is undefined when V_{DD} is just turned on.
To avoid the meaningless display, please keep the INH terminal at "H" until proper display data has been transferred.
In order to set the initial condition, 160-bit blank data or the first 160-bit data to be displayed should be transferred.

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MEMO