# 8-CHARACTER 2-LINE DOT MATRIX LCD CONTROLLER DRIVER WITH EXTENSION FUNCTION

## ■ GENERAL DESCRIPTION

The NJU6408B is a Dot Matrix LCD controller driver for 8-character 2-line display with extension function up to 40-character 2-line display.

It contains microprocessor interface circuits, instruction decoder controller, character generator ROM/RAM, high voltage operation common and segment drivers, and extension driver interface circuits.

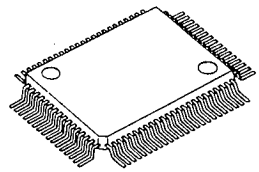
The microprocessor interface circuits which operate by 2MHz frequency, can be connected directly to 4/8bit microprocessor.

The character generator consists of 12k bits ROM and 64 bytes RAM. The standard version ROM is coded with 240 characters including capital and small letter fonts and some of Japanese fonts.

The high voltage operation 16-common and 40-segment drivers operate up to 13.5V, and drive up to 8-character 2-line display in single NJU6408B use.

The extension driver interface circuits enable combinations with NJU6407C or NJU6417C to increase the display capacity up to 40-character 2-line or 80-character 1-line.

## ■ PACKAGE OUTLINE



NJU6408BF

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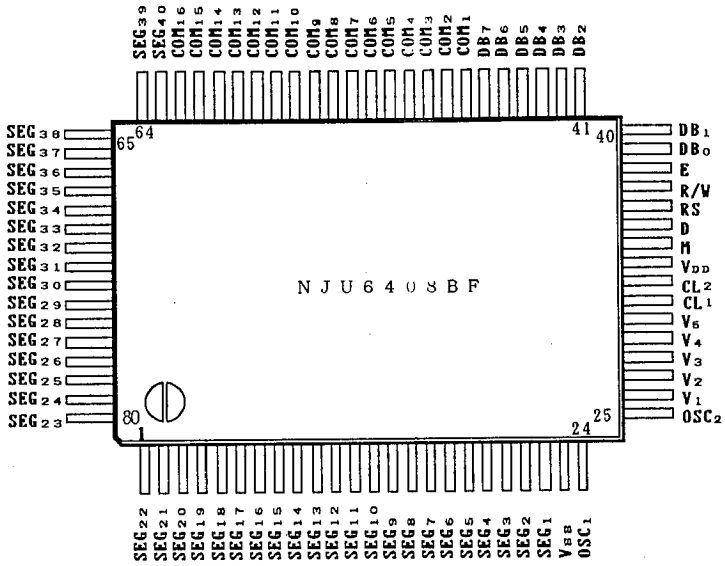
## ■ FEATURES

- 5 x 7 and 5 x 10 Fonts with Cursor Display
- 4/8 Bits Microprocessor Direct Interface
- Display Data RAM ( 80 x 8 bits ) ; Maximum 80 Characters
- Character Generator ROM ( 12,000 bits ) ; 240 Characters for 5 x 10 Dots
- Character Generator RAM ( 64 x 8 bits ) ; 8 Patterns(5x7 Dots) and 4 Patterns(5x10 Dots)
- Microprocessor can access to Display Data RAM and Character Generator RAM
- High Voltage LCD Driver ; 16-Common / 40-Segment
- Programmable Duty Ratio ; 1/8 Duty for 5x 7 Dots + Cursor, 1 Line
  1/11 Duty for 5x10 Dots + Cursor, 1 Line
  1/16 Duty for 5x 7 Dots + Cursor, 2 Lines
- Number of Maximum Display Characters

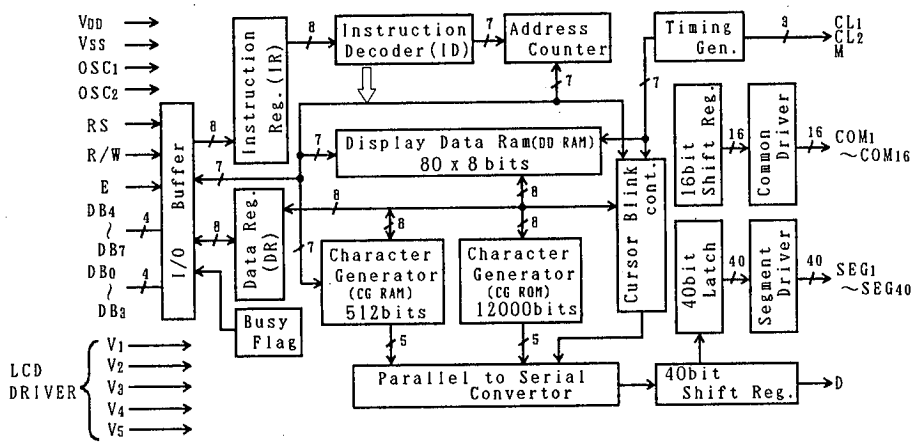
| Display Line | Duty factor | Extension | NJU6408B | NJU6407C/07CR | Display Capacity |
|---|---|---|---|---|---|
| 1 Line | 1/8,1/11 Duty | Not provided | 1 pc | - | 8-character 1-line |
| | | Provided | | 9 pcs | 80-character 1-line |
| 2 Lines | 1/16 Duty | Not provided | | - | 8-character 2-line |
| | | Provided | | 4 pcs | 40-character 2-line |

- Useful Instruction Set ; Clear Display, Return Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift
- Power On Initialize Circuits On-chip
- Oscillation Circuit On-chip ( External Resistor or Ceramic Resonator Required )
- Low Power Consumption
- Operating Voltage ( Except LCD Driving Voltage ) --- 5 V
- Package Outline --- Chip/QFP 80
- C-MOS Technology

## ■ PIN CONFIGURATION




## ■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

| NO. | SYMBOL | F U N C T I O N |
|---|---|---|
| 26～30 | $V_1$～$V_5$ | LCD Driving Power Source |
| 33 | $V_{DD}$ | Power Source ( + 5V ) |
| 23 | $V_{SS}$ | Power Source ( 0V ) |
| 24,25 | $OSC_1$, $OSC_2$ | Oscillation Terminals; External R or Ceramic Resonator connect to these terminals.<br>For external clock operation, the clock should be input on $OSC_1$. |
| 36 | RS | Register selection signal input<br>"0" : Instruction Register (Writing)<br>Busy Flag, Address Counter (Reading)<br>"1" : Data Register (Writing/Reading) |
| 37 | R/W | Read/Write selection signal input<br>"0" : Write , "1" : Read |
| 38 | E | Read/Write activation signal input |
| 43～46 | $DB_4$～$DB_7$ | 3-state Data Bus(Upper) to transfer the data between MPU and NJU6408B.<br>$DB_7$ is also used for the Busy Flag reading. |
| 39～42 | $DB_0$～$DB_3$ | 3-state Data Bus(Lower) to transfer the data between MPU and NJU6408B.<br>These bus are not used in the 4bit operation. |
| 31 | $CL_1$ | Data Latch Clock Output Terminal : To latch the serial data D sent to the Extension Driver. |
| 32 | $CL_2$ | Data Shift Clock Output Terminal : Shifts the serial data D. |
| 34 | M | Alternating signal for LCD Driving Output Terminal |
| 35 | D | Serial Data Output Terminal : The serial character pattern data output correspond to the each common signals.<br>"0" : No-active , "1" : Active |
| 47～62 | $COM_1$～$COM_{16}$ | LCD Common driving signal<br>No use terminals output no-active signal, or $COM_9$～$COM_{16}$ output no-active signal in the 1/8 duty operation and $COM_{12}$～$COM_{16}$ output no-active signal in the 1/11 duty operation. |
| 1～22<br>63～80 | $SEG_{22}$～$SEG_1$<br>$SEG_{40}$～$SEG_{23}$ | LCD Segment driving signal |

## ■ FUNCTIONAL DESCRIPTION

### (1) Description for each blocks

#### (1−1) Register

The NJU6408B incorporates two 8-bit registers, an Instruction Register(IR) and a Data Register(DR). The Register(IR) stores instruction codes such as "Clear Display" and "Return Home", and address data for Display Data RAM(DD RAM) and Character Generator RAM(CG RAM).

The MPU can write the instruction code and address data to the Register(IR), but it cannot read out from the Register(IR).

The Register(DR) is a temporary stored register, the data stored in the Register(DR) is written into the DD RAM or CG RAM and read out from the DD RAM or CG RAM.

The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM or CG RAM by internal operation.

When the address data for the DD RAM or CG RAM is written into the Register(IR), the addressed data in the DD RAM or CG RAM is transferred to the Register(DR). By the MPU read out the data in the Register(DR), the data transmitting process is performed completely.

After reading the data in the Register(DR) by the MPU, the next address data in the DD RAM or CG RAM is transferred automatically to the Register(DR) to provide for the next MPU reading.

These two registers are selected by the selection signal RS as shown below.

Table 1. shows register operation controlled by RS and R/W signals.

Table 1. Register Operation

| RS | R/W | Selected Register | Operation |
|---|---|---|---|
| 0 | 0 | IR | Write |
| 0 | 1 | | Read busy flag($DB_7$) and address counter($DB_0$～$DB_6$) |
| 1 | 0 | DR | Write (Register(DR) to DD RAM or CG RAM) |
| 1 | 1 | | Read (DD RAM or CG RAM to Register(DR)) |

#### (1−2) Busy Flag (BF)

When the internal circuits are in the operation mode, the busy flag(BF) is "1", and any instruction reading is inhibited.

The busy flag(BF) is output at $DB_7$ when RS="0" and R/W="1" as shown in table 1.

The next instruction should be written after the busy flag(BF) goes to "0".

#### (1−3) Address Counter (AC)

The address counter(AC) addressing the DD RAM and CG RAM.

When the address setting instruction is written into the Register(IR), the address information is transferred from Register(IR) to the Counter(AC). The selection of either the DD RAM or CG RAM is also determined by this instruction.

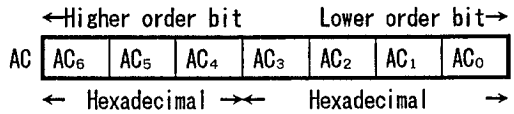
After writing (or reading) the display data to (or from) the DD RAM or CG RAM, the Counter (AC) increments (or decrements) automatically.

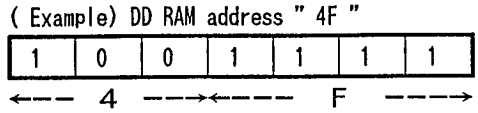
The address data in the Counter(AC) is output from $DB_6$～$DB_0$ when RS="0" and R/W="1" as shown in Table 1.

### (1−4) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consists of 80 x 8 bits stores up to 80-character display data represented in 8-bit code.

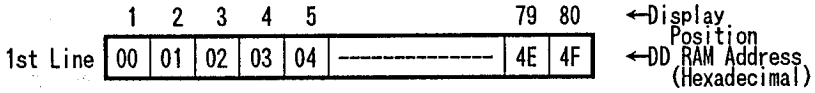
The unused display data memory area in the DD RAM can be used as a general data memory area. The DD RAM address data set in the address counter(AC) is represented in Hexadecimal.



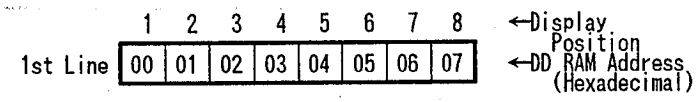

#### (1−4−1) 1-Line Display ( Function set code N=0 )

The relation between DD RAM address and display position on the LCD is shown below.

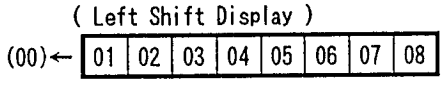


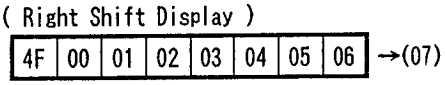

( a ) 8-character 1-line display using one NJU6408B.

In case of the 8-character display using one NJU6408B, the relation between DD RAM address and display positions on the LCD is as follows:

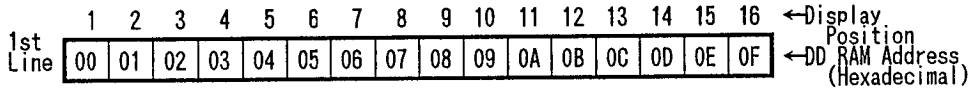



When the display shift is performed, the DD RAM address changes as follows:

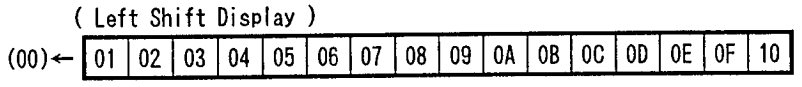


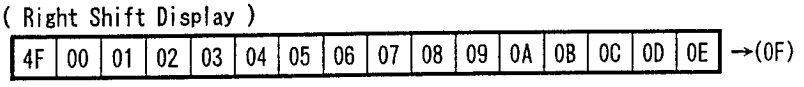




( b ) 16-character 1-line display using one NJU6408B and one NJU6407C.



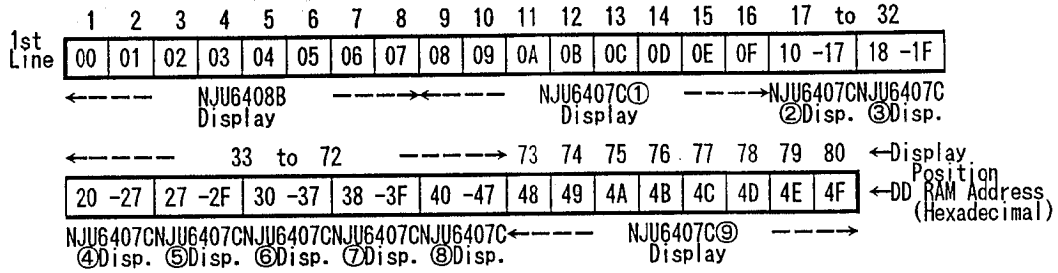

When the display shift is performed, the DD RAM address changes as follows:



( c ) More than 16-character 1-line display using one NJU6408B and more than 2 of NJU6407C.

As each additional NJU6407C can add another 8-character, up to 80-character can be displayed by connecting nine(9) of NJU6407C externally.




## (1−4−2) 2-Line Display ( Function set code N=1 )

The relation between DD RAM address and display position on the LCD is shown below:

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | | 37 | 38 | 39 | 40 | ← |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1st Line | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | ------ | 24 | 25 | 26 | 27 | ← |
| 2nd Line | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | ------ | 64 | 65 | 66 | 67 | ← |

Display Position

DD RAM Address (Hexadecimal)

Note : In the 2-line display mode, the 1st and 2nd line address are defined as $(00)_H$ to $(27)_H$ and $(40)_H$ to $(67)_H$. Please note that the end of 1st line address and the beginning of 2nd line address are not consecutive.

( a ) 8-character 2-line display using one NJU6408B.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | ← |
|---|---|---|---|---|---|---|---|---|---|
| 1st Line | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | ← |
| 2nd Line | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | ← |

Display Position

DD RAM Address (Hexadecimal)

When the display shift is performed, the DD RAM address changes as follows:

( Left Shift Display )

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| (00)← | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 |
| (40)← | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |

( Right Shift Display )

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 →(07) |
| | 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 →(47) |

( b ) 16-character 2-line display using one NJU6408B and one NJU6407C.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | ←Display Position |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1st Line | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | ← DD RAM Address (Hexadecimal) |
| 2nd Line | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | |

←— NJU6408B Display —→←— NJU6407C Display —→

When the display shift is performed, the DD RAM address changes as follows:

( Left Shift Display )

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (00)← | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 |
| (40)← | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 |

( Right Shift Display )

| | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | →(0F) |
| 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | →(4F) |

( c ) More than 16-character 2-line display using one NJU6408B and more than 2 of NJU6407C.

As each additional NJU6407C can add another 8-character 2-line, up to 40-character 2-line can be displayed by connecting four(4) of NJU6407C externally.

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| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1st Line | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 | 12 | 13 |
| 2nd Line | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 | 51 | 52 | 53 |

←— NJU6408B Display —→←— NJU6407C① Display —→← NJU6407C② Disp.

| 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | ←Display Position |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | ← DD RAM Address (Hexadecimal) |
| 54 | 55 | 56 | 57 | 58 | 59 | 5A | 5B | 5C | 5D | 5E | 5F | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | |

—→←— NJU6407C③ Display —→←— NJU6407C④ Display —→

## (1−5) Character Generator ROM (CG ROM)

The Character Generator ROM(CG ROM) generates 5 x 7 dots or 5 x 10 dots character patterns represented in 8-bit character codes.

The storage capacity is up to 240 kinds of 5 x 10 dots character patterns (In case of 5 x 7 dots display mode, upper 5 x 7 dots of 5 x 10 dots are displayed).

The correspondence between character code and standard character pattern of NJU6408B is shown in Table 2-1 to 2-3.

User-defined character patterns ( Custom Font ) are also available by mask option.

Table 2-1. CG ROM Character Pattern ( ROM version -00 )

| Lower 4 bit ( Hexadecimal ) \ Upper 4 bit ( Hexadecimal ) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | CGRAM (01)/(01) | | | | | | | | | | | | | | | |
| 1 | (02)/(01) | | | | | | | | | | | | | | | |
| 2 | (03)/(02) | | | | | | | | | | | | | | | |
| 3 | (04)/(02) | | | | | | | | | | | | | | | |
| 4 | (05)/(03) | | | | | | | | | | | | | | | |
| 5 | (06)/(03) | | | | | | | | | | | | | | | |
| 6 | (07)/(04) | | | | | | | | | | | | | | | |
| 7 | (08)/(04) | | | | | | | | | | | | | | | |
| 8 | (01)/(05) | | | | | | | | | | | | | | | |
| 9 | (02)/(05) | | | | | | | | | | | | | | | |
| A | (03)/(06) | | | | | | | | | | | | | | | |
| B | (04)/(06) | | | | | | | | | | | | | | | |
| C | (05)/(07) | | | | | | | | | | | | | | | |
| D | (06)/(07) | | | | | | | | | | | | | | | |
| E | (07)/(08) | | | | | | | | | | | | | | | |
| F | (08)/(08) | | | | | | | | | | | | | | | |

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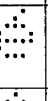
Table 2-2. CG ROM Character Pattern ( ROM version -01 )

| Lower 4 bit ( Hexadecimal ) | Upper 4 bit ( Hexadecimal ) | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 0 | CGRAM (01) / (01) |  | |  |  |  |  |  |  |  | |  |  |  |  |  |
| 1 | (02) / (01) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 2 | (03) / (02) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3 | (04) / (02) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 4 | (05) / (03) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 5 | (06) / (03) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 6 | (07) / (04) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 7 | (08) / (04) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 8 | (01) / (05) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 9 | (02) / (05) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A | (03) / (06) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B | (04) / (06) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C | (05) / (07) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D | (06) / (07) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E | (07) / (08) |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |
| F | (08) / (08) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Table 2-3. CG ROM Character Pattern ( ROM version -02 )

| Lower 4 bit ( Hexadecimal ) \ Upper 4 bit ( Hexadecimal ) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | CGRAM (01) / (01) |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1 | (02) / (01) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 2 | (03) / (02) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3 | (04) / (02) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 4 | (05) / |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 5 | (06) / (03) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 6 | (07) / (04) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 7 | (08) / (04) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 8 | (01) / (05) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 9 | (02) / (05) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| A | (03) / (06) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B | (04) / (06) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C | (05) / (07) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D | (06) / (07) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| E | (07) / (08) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| F | (08) / (08) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

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## (1－6) Character Generator RAM ( CG RAM )

The character generator RAM ( CG RAM ) can store any kind of character pattern in 5 x 10 or 5 x 7 dots written by the user program to display user's original character pattern.

The CG RAM can store 8 kind of character in 5 x 7 dots mode and 4 kind of character in 5 x 10 dots mode.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$ - $(07)_H$ or $(08)_H$ - $(0F)_H$ should be written to the DD RAM as shown in Table 2-1 to 2-3.

Table 3-1 and 3-2. show the correspondence among the character pattern, CG RAM address and Data.

Unused memory area of the CG RAM can also be used as the general data memory area.

Table 3-1. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern ( 5 x 7 dots ).

| Character Code (DD RAM Data) | CG RAM Address | Character Pattern (CG RAM Data) |
|---|---|---|
| 7 6 5 4 3 2 1 0 ←— —→ Upper bit Lower bit | 5 4 3 2 1 0 ←— —→ Upper bit Lower bit | 7 6 5 4 3 2 1 0 ←— —→ Upper bit Lower bit |
| 0 0 0 0 * 0 0 0 | 0 0 0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 | * * * 1 1 1 1 0 0 0 0 1 0 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 0 1 * * * 0 0 0 0 0 |
| 0 0 0 0 * 0 0 1 | 0 0 0 0 0 1 0 1 0 0 1 1 0 1 1 1 | * * * 0 0 0 1 0 0 0 0 1 1 1 1 0 0 1 0 0 1 1 1 1 0 0 1 0 0 0 * * * 0 0 0 0 0 |
| | 0 0 0 0 0 1 | * * * |
| 0 0 0 0 * 1 1 1 | 1 1 1 1 0 0 1 0 1 1 1 0 1 1 1 | * * * |

Character Pattern Example (1)

←Cursor Position

Character Pattern Example (2)

←Cursor Position

* : Don't Care

Notes :
1. Character code bit 0 to 2 correspond to the CG RAM add. 3 to 5(3bits:8 patterns).
2. CG RAM address 0 to 2 designate character pattern line position. The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 8th line should be "0". If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above. The bits 5 to 7 of the CG RAM are not appear on the display (no meaning for the display), but memory elements are existing, therefore it can be used as the general purpose RAM.
4. CG RAM character patterns are selected when character code bits 4 to 7 are all "0" and it is addressed by character code bits 0 to 2. Therefore, the address $(00)_H$ and $(08)_H$, $(01)_H$ and $(09)_H$, -------, $(07)_H$ and $(0F)_H$ select the same character pattern as shown in Table 2-1, 2-2, 2-3 and Table 3-1.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.

Table 3-2. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern ( 5 x 10 dots ).

| Character Code (DD RAM Data) 7 6 5 4 3 2 1 0 Upperbit Lowerbit | CG RAM Address 5 4 3 2 1 0 Upper Lower | Character Pattern (CG RAM Data) 7 6 5 4 3 2 1 0 Upperbit Lowerbit | |
|---|---|---|---|
| 0 0 0 0 * 0 0 * | 0 0 : 0 0 0 0 | * * * : 0 0 0 0 0 | |
| | 0 0 : 0 0 0 1 | * * * : 0 0 0 0 0 | |
| | 0 0 : 0 0 1 0 | * * * : 0 0 0 0 0 | |
| | 0 0 : 0 0 1 1 | * * * : 0 0 0 0 0 | |
| | 0 0 : 0 1 0 0 | * * * : 0 0 0 0 0 | |
| | 0 0 : 0 1 0 1 | * * * : 0 0 0 0 0 | Character Pattern Example (3) |
| | 0 0 : 0 1 1 0 | * * * : 0 0 0 0 0 | |
| | 0 0 : 0 1 1 1 | * * * : 0 0 0 0 0 | |
| | 0 0 : 1 0 0 0 | * * * : 0 0 0 0 0 | |
| | 0 0 : 1 0 0 1 | * * * : 0 0 0 0 0 | |
| | 0 0 : 1 0 1 0 | * * * : 0 0 0 0 0 | ←Cursor Position |
| | 0 0 : 1 0 1 1 | * * * : * * * * * | |
| | 0 0 : 1 1 0 0 | * * * : * * * * * | |
| | 0 0 : 1 1 0 1 | * * * : * * * * * | |
| | 0 0 : 1 1 1 0 | * * * : * * * * * | |
| | 0 0 : 1 1 1 1 | * * * : * * * * * | |
| | 0 1 : 0 0 0 0 | * * * : | |
| | 0 1 : 0 0 0 1 | * * * : | |

* : Don't Care

| | | | |
|---|---|---|---|
| 0 0 0 0 * 1 1 * | 1 1 : 1 0 0 1 | * * * : | |
| | 1 1 : 1 0 1 0 | * * * : | |
| | 1 1 : 1 0 1 1 | * * * : * * * * * | |
| | 1 1 : 1 1 0 0 | * * * : * * * * * | |
| | 1 1 : 1 1 0 1 | * * * : * * * * * | |

Notes : 1. Character code bit 1 and 2 correspond to the CG RAM address 4 and 5(2bits:4 patterns).
2. CG RAM address 0 to 3 designate character pattern line position. The 11th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 11th line should be "0". If there is "1" in the 11th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position are the same as 5 x 7 dots mode.
4. CG RAM character patterns are selected when character code bits 4 to 7 are all "0" and it is addressed by character code bits 1 and 2. Therefore, the address $(00)_H$,$(01)_H$,$(08)_H$ and $(09)_H$, $(02)_H$,$(03)_H$,$(10)_H$ and $(1A)_H$ for example, select the same character pattern as shown in Table 2-1, 2-2, 2-3 and Table 3-2.
5. "1" for CG RAM data corresponds to display On and "0" for display Off.

### (1−7) Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM, CG ROM and other internal circuits operation.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

This circuits also generate timing signals to control the extension driver like as NJU6407C.

### (1−8) LCD Driver

LCD driver consist of 16-common driver and 40-segment driver.

When the character font and line number are selected by a program, the required common drivers output the common driving waveform and the other common drivers output non-selection waveform automatically.

The extension driver for example NJU6407C's segment driver structure is as same as NJU6408B segment driver. The 40 bits of character pattern data are shifted in the shift-register and latched when the 40 bits shift performed completely. This latched data controls display driver to output LCD driving waveform.

The serial data output transfers the serial data to the cascade connection extension driver like as NJU6407C, to extend display capacity.

Since the serial data always transfer from the last character pattern (last address display data in the DD RAM) and latched when the top of character pattern (top address display data in the DD RAM) read out from the DD RAM, the NJU6408B always display from the top character and every extended extension driver display following character than front.



### (1−9) Cursor Blinking Control Circuit

This circuits controls cursor On/Off and cursor position character blinks.

The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).

When the address counter is $(08)_H$, a cursor position is shown as follows:

| | $AC_6$ | $AC_5$ | $AC_4$ | $AC_3$ | $AC_2$ | $AC_1$ | $AC_0$ |
|---|---|---|---|---|---|---|---|
| (AC) | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

1-Line Display

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | ---- |

← Display position

← DD RAM address (Hexadecimal)

↑ Cursor position

2-Line Display

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | ---- |
| 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | ---- |

← Display position

← DD RAM address (Hexadecimal)

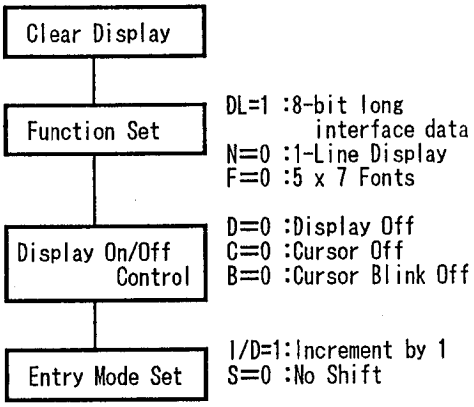
↑ Cursor position

(Note) The cursor or blinks also appear when the address counter (AC) selects the CG RAM. But the displayed cursor and blink are meaningless.
If the AC storing the CG RAM address data, the cursor and blink are displayed in the meaningless position.

### (2) Power on Initialization by internal circuits

The NJU6408B is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 10 ms after $V_{DD}$ rises to 4.5V.

Initialization flow is shown below:




NOTE
If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the Internal Power on Initialization Circuits will not operate and initialization will not be performed.
In this case the initialization by MPU software is required.

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### (3) Instructions

The NJU6408B incorporates two registers, an Instruction Register(IR) and a Data Register(DR). These two registers store control information temporarily to allow interface between NJU6408B and MPU or peripheral ICs operating different cycles. The operation of NJU6408B is determined by this control signal from MPU. The control information includes register selection signals (RS), read/write signals (R/W) and data bus signals ($DB_0$ to $DB_7$).

Table 4. shows each instruction and its operating time.

Note) The execution time mentioned in Table 4. based on fcp or fosc=250kHz.
If the oscillation frequency is changed, the execution time is also changed.

Table 4. Table of Instructions

| INSTRUCTIONS | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | DESCRIPTION | EXEC TIME |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Display clear and sets DD RAM address 0 in AC. | 1.64ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | Sets DD RAM address 0 in AC and returns display being shifted to original position. DD RAM contents remain unchanged | 1.64ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets cursor move direction and specifies shift of display are performed in data read/write. I/D=1:Increment, I/D=0:Decrement S=1:Accompanies display shift | 40us |
| Display On/Off Control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B). | 40us |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | * | * | Moves cursor and shifts display without changing DD RAM contents S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to the right R/L=0 : Shift to the left | 60us |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | F | * | * | Sets interface data length(DL), number of display lines(N) and character font(F). DL=1 : 8 bits , DL=0 : 4 bits N=1 : 2 lines , N=0 : 1 line F=1 : 5x10 dots, F=0 : 5x7 dots | 40us |
| Set CG RAM Address | 0 | 0 | 0 | 1 | ←— | $A_{CG}$ | | | | —→ | Sets CG RAM address. After this instruction, the data is transferred on CG RAM. | 40us |
| Set DD RAM Address | 0 | 0 | 1 | ←— | $A_{DD}$ | | | | | —→ | Sets DD RAM address. After this instruction, the data is transferred on DD RAM. | 40us |
| Read Busy Flag & Address | 0 | 1 | BF | ←— | AC | | | | | —→ | Reads busy flag and AC contents. BF=1 : Internally operating BF=0 : Can accept instruction | 0us |
| Write Data to CG & DD RAM | 1 | 0 | ←— | Write Data | | | | | | —→ | Writes data into DD or CG RAMs. | 40us |
| Read Data from CG or DD RAM | 1 | 1 | ←— | Read Data | | | | | | —→ | Reads data from DD or CG RAMs. | 60us |
| Explanation of Abbreviation | DD RAM : Display data RAM , CG RAM : Character generator RAM<br>$A_{CG}$ : CG RAM address , $A_{DD}$ : DD RAM address, Corresponds to cursor address<br>AC : Address counter used for both of DD and CG RAMs | | | | | | | | | | | |

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## (3−1) Description of each instructions

### (a) Clear Display

| | RS | R/W | $DB_7$ | $DB_6$ | $DB_5$ | $DB_4$ | $DB_3$ | $DB_2$ | $DB_1$ | $DB_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Clear display instruction is executed when the code "1" is written into $DB_0$. When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address 0 is set into the address counter and entry mode is set increment.

If the cursor or blink are displayed, they are returned to the left end of the LCD (the left end of the 1st line in the 2-line display mode).

The (S) of entry mode does not change.

Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

### (b) Return Home

| | RS | R/W | $DB_7$ | $DB_6$ | $DB_5$ | $DB_4$ | $DB_3$ | $DB_2$ | $DB_1$ | $DB_0$ | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | * = Don't care |

Return home instruction is executed when the code "1" is written into $DB_1$. When this instruction is executed, the DD RAM address 0 is set into the address counter. Display is returned its original position if shifted, the cursor or blink are returned to the left end of the LCD (the left end of the 1st line in the 2-line display mode) if the cursor or blink are on the display.

The DD RAM contents do not change.

### (c) Entry Mode Set

| | RS | R/W | $DB_7$ | $DB_6$ | $DB_5$ | $DB_4$ | $DB_3$ | $DB_2$ | $DB_1$ | $DB_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S |

Entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into $DB_2$ and the codes of (I/D) and (S) are written into $DB_1$(I/D) and $DB_0$(S), as shown below.

(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

| I/D | Function |
|---|---|
| 1 | Address increment: The address of the DD RAM or CG RAM increment ( +1) when the read/write, and the cursor or blink move to the right. |
| 0 | Address decrement: The address of the DD RAM or CG RAM decrement ( −1) when the read/write, and the cursor or blink move to the left. |

| S | Function |
|---|---|
| 1 | Entire display shift<br>The shift direction is determined by I/D: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM. |
| 0 | The display does not shifting. |

(d) Display On/Off Control

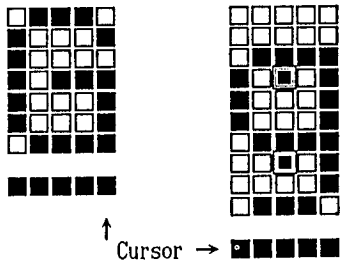
| | RS | R/W | $DB_7$ | $DB_6$ | $DB_5$ | $DB_4$ | $DB_3$ | $DB_2$ | $DB_1$ | $DB_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Display On/Off control instruction which controls the whole display On/Off, the cursor On /Off and the cursor position character Blink, is executed when the code "1" is written into $DB_3$ and the codes of (D), (C) and (B) are written into $DB_2$(D), $DB_1$(C) and $DB_0$(B), as shown below.

| D | Function |
|---|---|
| 1 | Display On. |
| 0 | Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1. |

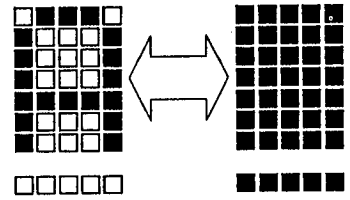
| C | Function |
|---|---|
| 1 | Cursor On. The cursor is displayed by 5 dots on the 8th line in 5 x 7 Font mode and on the 11th line in 5 x 10 Font mode. |
| 0 | Cursor Off. Even if the display data write, the I/D etc does not change. |

| B | Function |
|---|---|
| 1 | The cursor position character is blinking. Blinking rate is 379.2ms at $f_{CP}$ or $f_{OSC}$=270kHz and 409.6ms at $f_{CP}$=250kHz. The blink is displayed alternatively with all on (it means all black) and character display. The cursor and the blink can be displayed simultaneously. |
| 0 | The character does not blink. |




Character Font 5 x 7 dots

(1) Cursor display example



Alternating display

(2) Blink display example

(e) Cursor/Display Shift

| | RS | R/W | $DB_7$ | $DB_6$ | $DB_5$ | $DB_4$ | $DB_3$ | $DB_2$ | $DB_1$ | $DB_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | * | * |

* = Don't care

The Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display. In the 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly, each line moves only horizontally.

The 2nd line display does not shift into the 1st line position.

The contents of address counter(AC) does not change by operation of the display shift only.

This instruction is executed when the code "1" is written into $DB_4$ and the codes of (S/C) and (R/L) are written into $DB_3$(S/C) and $DB_2$(R/L), as shown below.

| S/C | R/L | Function |
|---|---|---|
| 0 | 0 | Shifts the cursor position to the left ((AC) is decremented by 1) |
| 0 | 1 | Shifts the cursor position to the right ((AC) is incremented by 1) |
| 1 | 0 | Shifts the entire display to the left and the cursor follows it. |
| 1 | 1 | Shifts the entire display to the right and the cursor follows it. |

(f) Function Set

| | RS | R/W | $DB_7$ | $DB_6$ | $DB_5$ | $DB_4$ | $DB_3$ | $DB_2$ | $DB_1$ | $DB_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 0 | 1 | DL | N | F | * | * |

* = Don't care

Function set instruction which sets the interface data length and number of display lines and character font, is executed when the code "1" is written into $DB_5$ and the codes of (DL), (N) AND (F) are written into $DB_4$(DL), $DB_3$(N) and $DB_2$(F), as shown below.

(DL) sets the interface data length, (N) sets the number of display lines either the 1-line or 2-line and (F) sets the display Font either 5 x 7 dots or 5 x 10 dots.

NOTE

This function set instruction must be performed at the head of the program prior to all other existing instructions(except Busy flag/Address read). This function set instruction can not be executed afterwards unless the interface data length change.

| DL | Function |
|---|---|
| 1 | Set the interface data length to 8-bit ($DB_7$ to $DB_0$) |
| 0 | Set the interface data length to 4-bit ($DB_7$ to $DB_4$)<br>The data must be sent or received twice in this mode. |

| N | F | Display lines | Character Font | Duty ratio | Note |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 5 x 7 dots | 1/8 | |
| 0 | 1 | 1 | 5 x 10 dots | 1/11 | |
| 1 | 0 | 2 | 5 x 7 dots | 1/16 | Character Font 5 x 10 dots can not display 2-line. |

(g) Set CG RAM Address

| | RS | R/W | $DB_7$ | $DB_6$ | $DB_5$ | $DB_4$ | $DB_3$ | $DB_2$ | $DB_1$ | $DB_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 0 | 1 | A | A | A | A | A | A |

←Higher order bit  Lower order bit →

Set CG RAM address set instruction is executed when the code "1" is written into $DB_6$ and the address is written into $DB_5$ to $DB_0$ as shown above.

The address data mentioned by binary code " AAAAAA " is written into the address counter (AC) together with the CG RAM addressing condition. After this instruction execution, the data writing/reading is performed into/from the CG RAM.

(h) Set DD RAM Address

| | RS | R/W | $DB_7$ | $DB_6$ | $DB_5$ | $DB_4$ | $DB_3$ | $DB_2$ | $DB_1$ | $DB_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 0 | 1 | A | A | A | A | A | A | A |

←Higher order bit  Lower order bit→

Set DD RAM address instruction is executed when the code "1" is written into $DB_7$ and the address is written into $DB_6$ to $DB_0$ as shown above.

The address data mentioned by binary code " AAAAAAA " is written into the address counter (AC) together with the DD RAM addressing condition. After this instruction execution, the data writing/reading is performed into/from the DD RAM.

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Note : In case of the 1-line display, the address data is $(00)_H$ to $(4F)_H$, and during the 2-line display, the address is $(00)_H$ to $(27)_H$ for the 1st line and $(40)_H$ to $(67)_H$ for the 2nd line.

(i) Read Busy Flag & Address

| | RS | R/W | $DB_7$ | $DB_6$ | $DB_5$ | $DB_4$ | $DB_3$ | $DB_2$ | $DB_1$ | $DB_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 0 | 1 | BF | A | A | A | A | A | A | A |

←Higher order bit  Lower order bit→

This instruction reads out the internal status of the NJU6408B. When this instruction is executed, the busy flag (BF) which indicate internal operation is read out from $DB_7$ and the address of the CG RAM or DD RAM is read out from $DB_6$ to $DB_0$ (the address for the CG RAM or DD RAM is determined by the previous instruction).

(BF)="1" indicates that internal operation is in progress. The next instruction is inhibited when (BF)="1". Check the (BF) status before the next write operation.

(j) Write Data to CG RAM or DD RAM

| | RS | R/W | $DB_7$ | $DB_6$ | $DB_5$ | $DB_4$ | $DB_3$ | $DB_2$ | $DB_1$ | $DB_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 0 | D | D | D | D | D | D | D | D |

←Higher order bit Lower order bit→

Write Data to CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).

By the execution of this instruction, the binary 8 bit data " DDDDDDDD " are written into the CG RAM or DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction. After this instruction execution, the address increment(+1) or decrement (-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

(k) Read Data from CG RAM or DD RAM

| | RS | R/W | $DB_7$ | $DB_6$ | $DB_5$ | $DB_4$ | $DB_3$ | $DB_2$ | $DB_1$ | $DB_0$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Code | 1 | 1 | D | D | D | D | D | D | D | D |

←Higher order bit Lower order bit→

Read Data from CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and (R/W).

By the execution of this instruction, the binary 8 bit data " DDDDDDDD " are read out from the CG RAM or DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction.

Before executing this instruction, either the CG RAM address set or DD RAM address set must be executed, otherwise the first read out data are invalidated.

When this instruction is serially executed, the next address data is normally read from the second read.

The address set instruction is not required if the cursor shift instruction is executed just beforehand(only DD RAM reading).

The cursor shift instruction has same function as the DD RAM address set, so that after reading the DD RAM, the address increment or decrement is executed automatically according to the entry mode.

But display shift does not occur regardless of the entry mode.

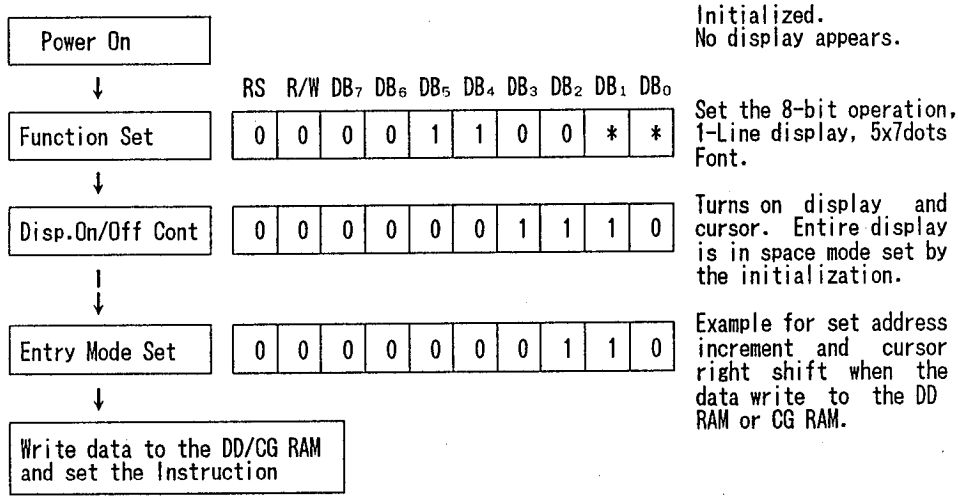
Note: The address counter (AC) is automatically incremented or decremented by 1 after write instruction to either of the CG RAM or DD RAM. Even if the read instruction is executed after this instruction, the addressed data can not be read out correctly. For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

### (3−2) Initialization using the internal reset circuits

(a) 8-character 1-line display in 8-bit operation (Using internal reset circuits).

At the 8-character 1-line display, the Function set, Display On/Off Control and Entry Set Instruction must be executed before the data input, as shown below.

The DD RAM of the NJU6408B can store up to 80 characters, as explained before, therefore the advertising moving display is available when combined with the display shift operation. Since the display shift operation changes only display position and the DD RAM contents remain unchanged, display data which are entered first can be output when the return home operation is performed.

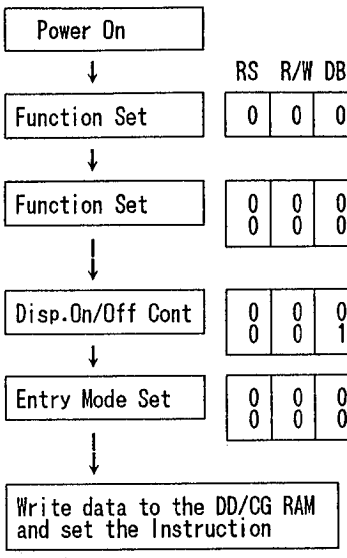



(b) 8-character 1-line in 4-bit operation (Using internal reset circuits).

In the 4-bit operation, the function set must be performed by the user programming.

When the power is turned on, 8-bit operation is selected automatically, therefore the first input is performed under 8-bit operation. In this operation, full instruction can not input because of terminals $DB_0$ to $DB_3$ are no connection. Therefore, same instruction must be rewritten on the RS, R/W and $DB_7$ to $DB_4$, as shown below. Since one operation is completed by the two accesses in the 4-bit operation mode, rewrite is required to set the instruction code in full.

8-character 1-line in 4-bit operation is shown as follows:




Initialized.
No display appears.

Set the 4-bit operation.
This step is executed in 8-bit mode set by the initialization.

Set the 4-bit operation, 1-line display, 5 x 7 dots Font.
The 4-bit operation starts from this step.

Turn on display and cursor.
Entire display is in space mode set by the initialization.

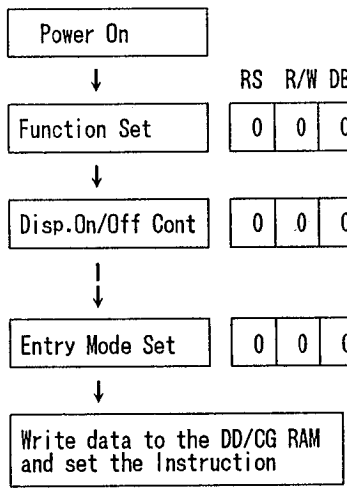
Example for set address increment and cursor right shift when the data write to the DD RAM or CG RAM.

(c) 8-character 2-line in 8-bit operation (Using internal reset circuits).

In the 2-line display, the cursor moves automatically from the 1st to the 2nd line after the 40th character of the 1st line has been written. Therefore, if the display character is only 8 characters in the 1st line, the DD RAM address must be set by the user programing to change the cursor position to the 2nd line.

The 1st and 2nd line displays will shift at the same time.

When the displayed data is shifted repeatedly, each line moves only horizontally. The 2nd line display does not shift into the 1st line position.




Initialized.
No display appears.

Set the 8-bit operation, 2-line display, 5 x 7dots Font.

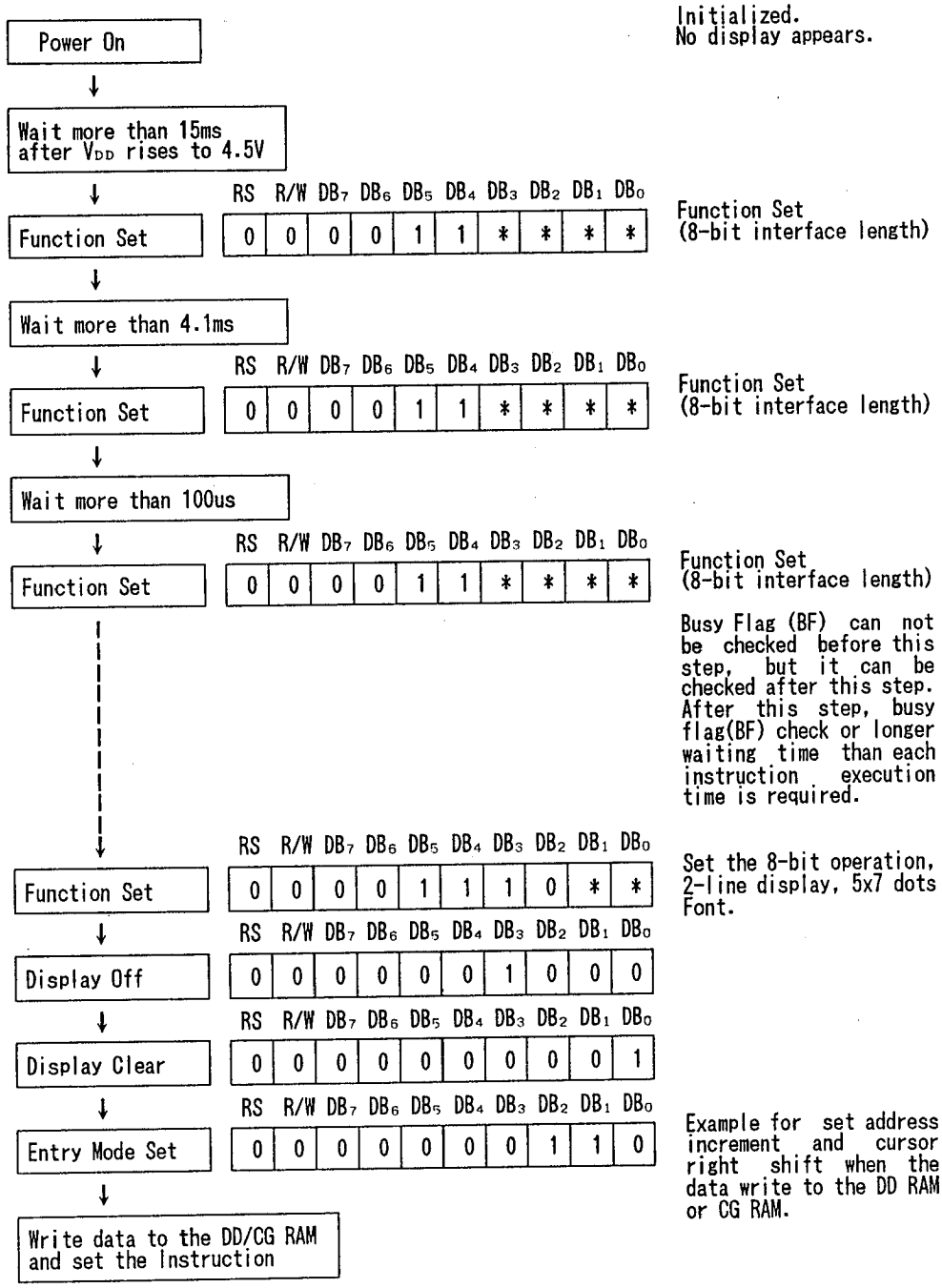
Turns on display and cursor. Entire display is in space mode set by the initialization.

Example for set address increment and cursor right shift when the data write to the DD or CG RAM.

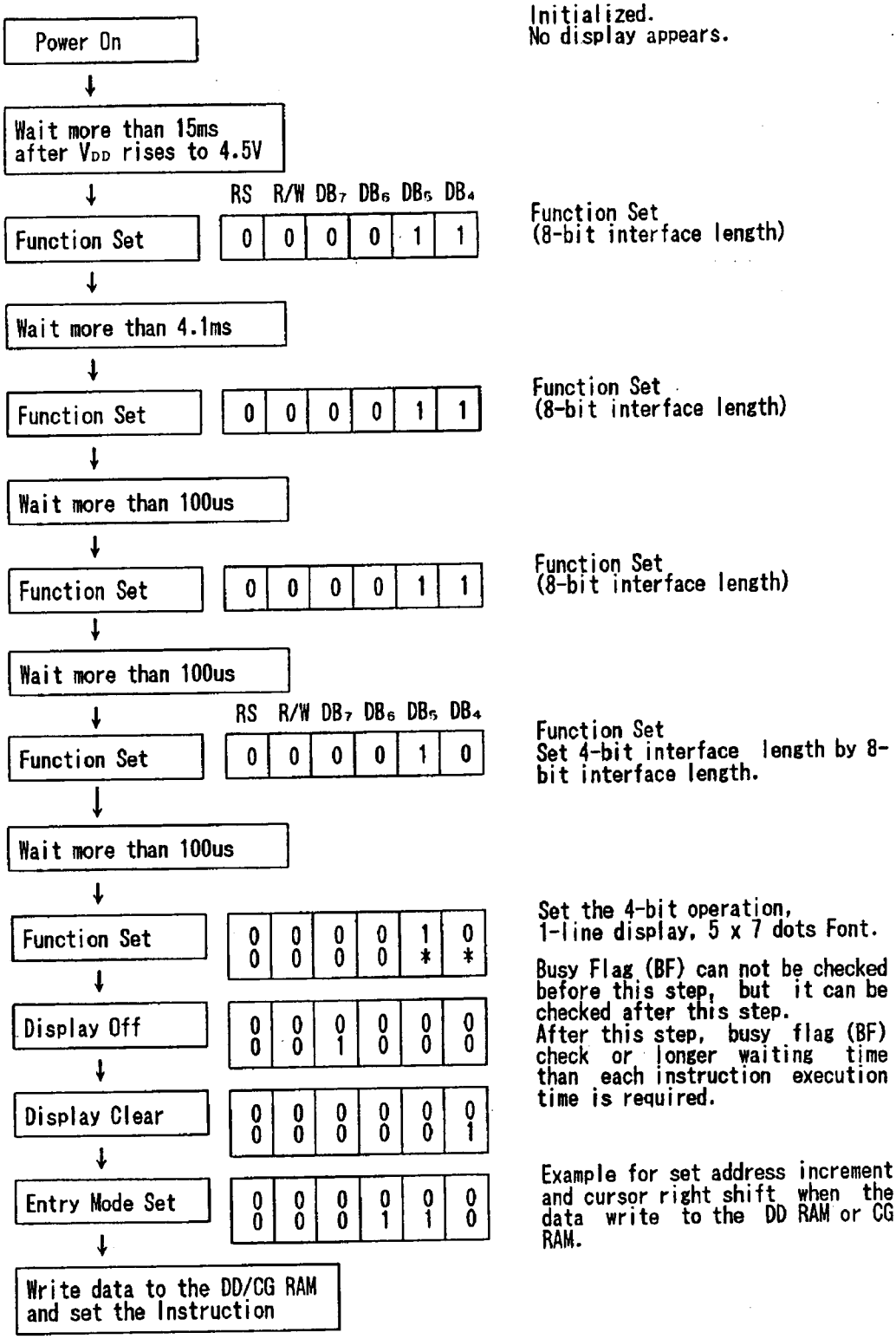
### (3-3) Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6408B must be initialized by the instruction.

(a) Initialization by Instruction in 8 bit interface length.



(b) Initialization by Instruction in 4-bit interface length




5

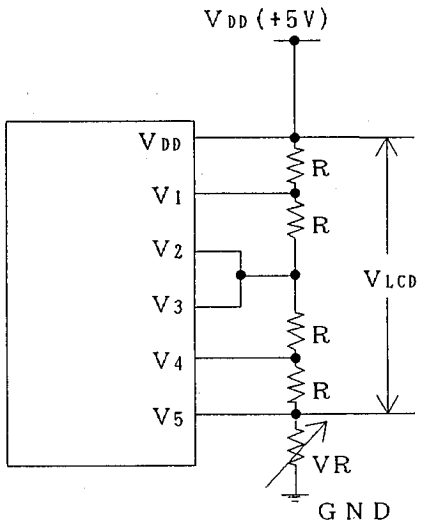
## (4) LCD DISPLAY

### (4−1) Power Supply for LCD Driving

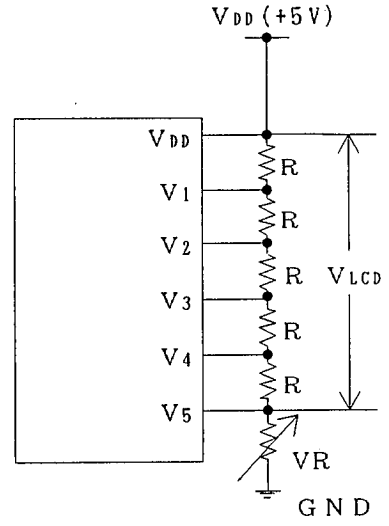
The terminals $V_1$ to $V_5$ require various constant voltage to generate LCD driving waveform. This constant voltage must be changed according to the duty ratio as shown below. The $V_{LCD}$ is a peak level of LCD driving voltage and each voltage is generated by the bleeder resistance as shown below.

Table 5. Relation between LCD driving voltage and Duty ratio.

| Power supply | Duty Ratio | 1/8 , 1/11 | 1/16 |
|---|---|---|---|
| | Bias | 1/4 | 1/5 |
| $V_1$ | | $V_{DD}$ to $1/4V_{LCD}$ | $V_{DD}$ to $1/5V_{LCD}$ |
| $V_2$ | | $V_{DD}$ to $1/2V_{LCD}$ | $V_{DD}$ to $2/5V_{LCD}$ |
| $V_3$ | | $V_{DD}$ to $1/2V_{LCD}$ | $V_{DD}$ to $3/5V_{LCD}$ |
| $V_4$ | | $V_{DD}$ to $3/4V_{LCD}$ | $V_{DD}$ to $4/5V_{LCD}$ |
| $V_5$ | | $V_{DD}$ to $V_{LCD}$ | $V_{DD}$ to $V_{LCD}$ |




(a) 1/4 Bias (1/8, 1/11 duty)




(b) 1/5 Bias (1/16 duty)

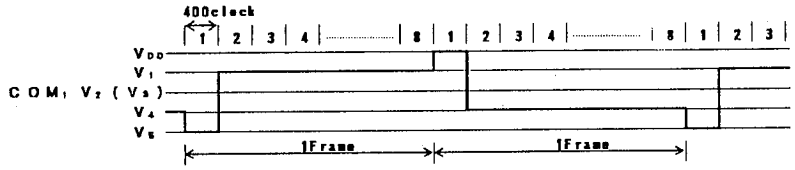
## (4−2) Relation between oscillation frequency and LCD frame frequency.

The NJU6408B requires either one of the oscillation resistance(RF) or ceramic resonator for the internal oscillation, or external clock.

LCD frame frequency example mentioned below is based on 250kHz oscillation.

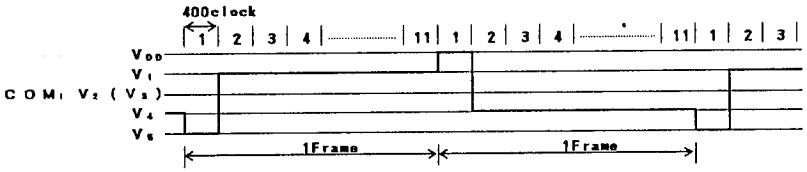
( 1 clock = 4us )

(a) 1/8 duty



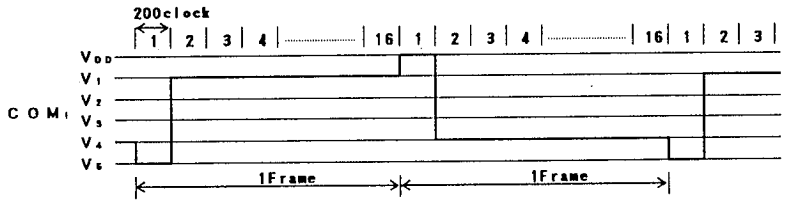

1 frame = 4(us) x 400 x 8 = 12,800(us) = 12.8(ms)
Frame frequency = 1/12.8(ms) = 78.1(Hz)

(b) 1/11 duty




1 frame = 4(us) x 400 x 11 = 17,600(us) = 17.6(ms)
Frame frequency = 1/17.6(ms) = 56.8(Hz)

(c) 1/16 duty




1 frame = 4(us) x 200 x 16 = 12,800(us) = 12.8(ms)
Frame frequency = 1/12.8(ms) = 78.1(Hz)

## (5) Interface with MPU

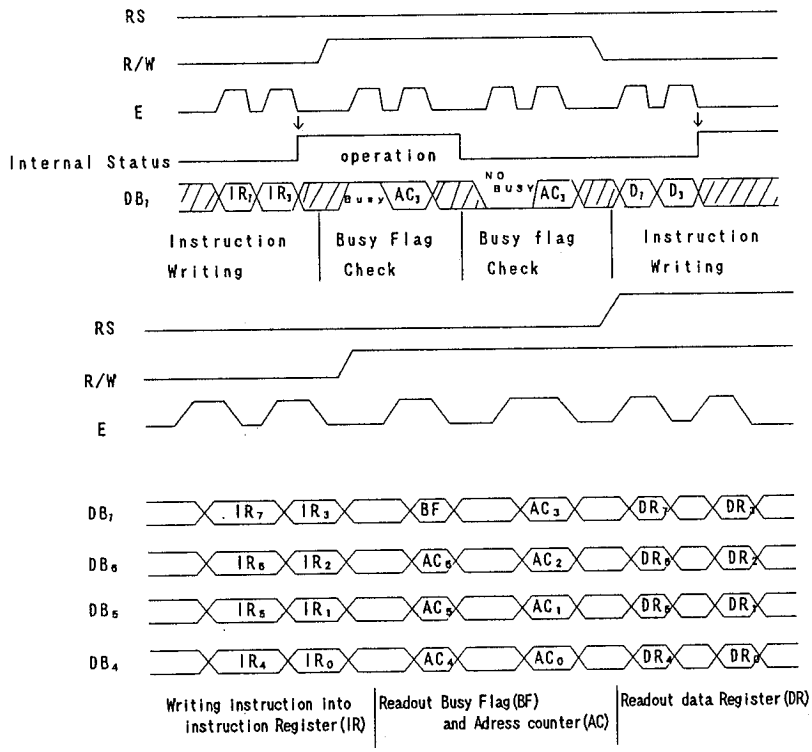
NJU6408B can be interfaced with both of 4/8 bit MPU and the two-time 4-bit or one-time 8-bit data transfer is available.

### (5−1) 4-bit MPU interface

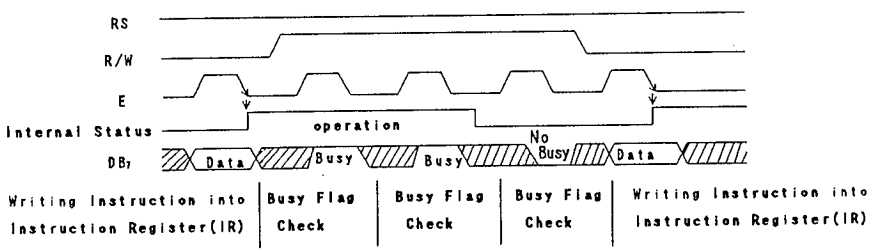
When the interface length is 4-bit, the data transfer is performed by 4 lines connected to $DB_4$ to $DB_7$ ($DB_0$ to $DB_3$ are not used). The data transfer with the MPU is completed by the two-time 4-bit data transfer.

The data transfer is executed in the sequence of upper 4-bit (the data $DB_4$ to $DB_7$ at 8-bit length) and lower 4-bit (the data $DB_0$ to $DB_3$ at 8-bit length).

The busy flag check must be executed after two-time 4-bit data transfer (1 instruction execution). In this case the data of busy flag and address counter are also output twice.




### (5−2) 8-bit MPU interface



## ■ ABSOLUTE MAXIMUM RATINGS

( Ta=25℃ )

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage (1) | $V_{DD}$ | - 0.3 ~ + 7.0 | V |
| Supply Voltage (2) | $V_1$ ~ $V_5$ | $V_{DD}$-13.5 ~ $V_{DD}$+0.3 | V |
| Input Voltage | Vr | - 0.3 ~ $V_{DD}$+0.3 | V |
| Operating Temperature | Topr | - 30 ~ + 80 | ℃ |
| Storage Temperature | Tstg | - 55 ~ + 125 | ℃ |

Note 1) If the LSI are used on condition above the absolute maximum ratings, the LSI may be dastroyed.
Using the LSI within electrical characteristics is strongly recomended for normal operation.
Use beyond the electric characteristics conditions will cause malfunction and poor riliability.

Note 2) All voltage values are specified as $V_{SS}$ = 0 V

Note 3) The relation of $V_{DD} \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_5$ , $V_{DD} > V_{SS} \geqq V_5$ must be maintained.

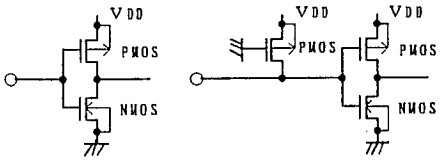
## ■ ELECTRICAL CHARACTERISTICS

( $V_{DD}$=5V±10% , Ta=-20 ~ +75℃ )

| PARAMETER | | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNIT | |
|---|---|---|---|---|---|---|---|---|---|
| Operating Voltage | | $V_{DD}$ | | | 4.5 | 5.0 | 5.5 | V | |
| Input Voltage | 1 | $V_{IH1}$ | All Input and Input/Output Terminals except OSC Terminals | | 2.3 | | $V_{DD}$ | V | 4 |
| | | $V_{IL1}$ | | | | | 0.8 | | |
| | 2 | $V_{IH2}$ | Only OSC Terminal | | $V_{DD}$-1 | | $V_{DD}$ | | |
| | | $V_{IL2}$ | | | | | 1.0 | | |
| Output Voltage | 1 | $V_{OH1}$ | Input/Output Terminals | $-I_{OH}$=0.205mA | 2.4 | | | V | |
| | | $V_{OL1}$ | | $I_{OL}$=1.6mA | | | 0.4 | | |
| | 2 | $V_{OH2}$ | Output Terminals | $-I_{OH}$=0.04mA | 0.9$V_{DD}$ | | | | |
| | | $V_{OL2}$ | | $I_{OL}$=0.04mA | | | 0.1$V_{DD}$ | | |
| Driver On-resist. (COM) | | $R_{COM}$ | ±Id=0.05mA(All com. term.) | | | | 20 | kΩ | 5 |
| Driver On-resist. (SEG) | | $R_{SEG}$ | ±Id=0.05mA(All seg. term.) | | | | 30 | | |
| Input Leakage Current | | $I_{LI}$ | $V_{IN}$=0 ~ $V_{DD}$ | | - 1 | | 1 | uA | 6 |
| Pull-up Resist Current | | $-I_P$ | $V_{DD}$=5V, RS, R/W, DB | | 50 | 125 | 250 | | |
| Operating Current (1) | | $I_{DD1}$ | Ceramic Resonator Osc. $V_{DD}$=5V, $f_{OSC}$=250kHz | | | 0.55 | 0.8 | mA | 7 |
| Operating Current (2) | | $I_{DD2}$ | CR Oscillation( Ext. R ) $V_{DD}$=5V, $f_{OSC}$=$f_{CP}$=270kHz | | | 0.35 | 0.6 | | |
| Ext. Clk | Operating Freq. | fcp | External clock inputs to OSC1, OSC2 open | | 125 | 250 | 350 | kHz | 8 |
| | Duty | Duty | | | 45 | 50 | 55 | % | |
| | Rise Time | trcp | | | | | 0.2 | us | |
| | Fall Time | tfcp | | | | | 0.2 | | |
| Int. Osc | Oscillation Frequency | fosc | CR Osc. Rf=91kΩ±2% | | 190 | 270 | 350 | kHz | 9 |
| | | | Ceramic resonator | | 245 | 250 | 350 | | 10 |
| LCD Driving Voltage | | $V_{LCD1}$ | $V_{DD}$ - $V_5$ | 1/5 Bias | $V_{DD}$-3.0 | | $V_{DD}$-13.5 | V | 11, 12 |
| | | $V_{LCD2}$ | | 1/4 Bias | | | | | |

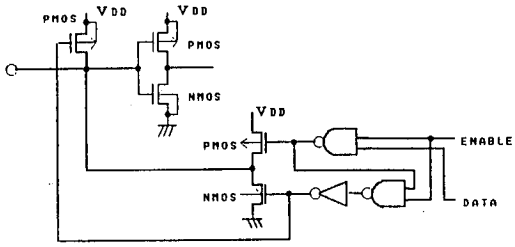
Note 4) Input/Output structure except LCD driver are shown below:

Input Terminal Structure




E Terminal RS,R/W Terminals

Input/Output Terminal Structure




$DB_0$ to $DB_7$ TerminalS

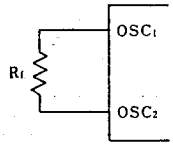
Note 5) $R_{COM}$ and $R_{SEG}$ are the resistance values between power supply terminals($V_{DD}$, $V_1$, $V_4$, $V_5$) and each common terminal($COM_1$ to $COM_{16}$), and supply voltage ($V_{DD}$, $V_2$, $V_3$, $V_5$) and each segment terminals($SEG_1$ to $SEG_{40}$)respectively, and measured when the current Id is flown on every common and segment terminals at a same time.

Note 6) Except pull-up resistance current and output driver current.

Note 7) Except Input/output current.

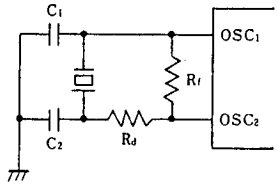
Note 8) Apply to external oscillation mode.

Note 9) Apply to internal CR oscillation using a oscillation resistance Rf
As the oscillating frequency is affected by the stray capacitance of the terminals $OSC_1$ and $OSC_2$, shorter connection length of these terminals are required.



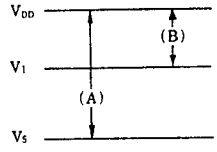

$R_f$ : 91kΩ ± 2%

Note 10) Apply to external ceramic resonator oscillation.
Ceramic resonator specification example.
Rf = 1MΩ ± 10%
$C_1$ = 680pF
$C_2$ = 680pF
Rd = 3.3kΩ
As this circuit example mentioned only for standard application, it can not guaranty the characteristics of oscillation.
Please check the external parts value before production.




Note 11) Apply to the output voltage from each COM and SEG are less than ±0.15V against the LCD driving constant voltage ($V_{DD}$, $V_1$, $V_2$, $V_3$, $V_4$, $V_5$) at no load condition.

Note 12) Mentioned condition of $V_1$ and $V_5$ do not guarantee the right operation of this LSI. Right LCD driving voltage is specified in "Electrical Characteristics"




(A) = $V_{DD} - V_5$
(B) = $V_{DD} - V_1$
(A) ≧ 1.5V
(B) ≦ 0.25×(A)

- Bus timing characteristics ($V_{DD}$ = 5.0V±10%, $V_{SS}$ = 0V, Ta = -20 ~ +75℃)

Write operation ( Write from MPU to NJU6408B )

| PARAMETER | | SYMBOL | MIN | MAX | CONDITION | UNIT |
|---|---|---|---|---|---|---|
| Enable Cycle Time | | $t_{CYCE}$ | 500 | | fig.1 | ns |
| Enable Pulse Width | "High" level | $P_{WEH}$ | 220 | | | |
| Enable Rise Time, Fall Time | | $t_{Er}$, $t_{Ef}$ | | 20 | | |
| Set up Time | RS, R/W, E | $t_{AS}$ | 40 | | | |
| Address Hold Time | | $t_{AH}$ | 10 | | | |
| Data Set up Time | | $t_{DSW}$ | 60 | | | |
| Data Hold Time | | $t_H$ | 10 | | | |

Timing Characteristics (Write operation)

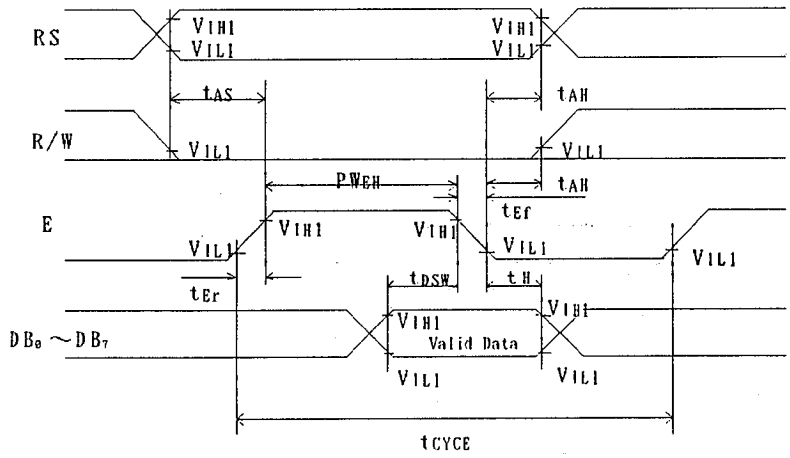



fig. 1

Read operation ( Read from NJU6408B to MPU )

| PARAMETER | | SYMBOL | MIN | MAX | CONDITION | UNIT |
|---|---|---|---|---|---|---|
| Enable Cycle Time | | $t_{CYCE}$ | 500 | | fig.2 | ns |
| Enable Pulse Width | "High" level | $P_{WEH}$ | 220 | | | |
| Enable Rise Time, Fall Time | | $t_{Er}$, $t_{Ef}$ | | 20 | | |
| Set up Time | RS, R/W, E | $t_{AS}$ | 40 | | | |
| Address Hold Time | | $t_{AH}$ | 10 | | | |
| Data Delay Time | | $t_{DDW}$ | | 120 | | |
| Data Hold Time | | $t_{DDH}$ | 20 | 100 | | |

Timing Characteristics (Read operation)

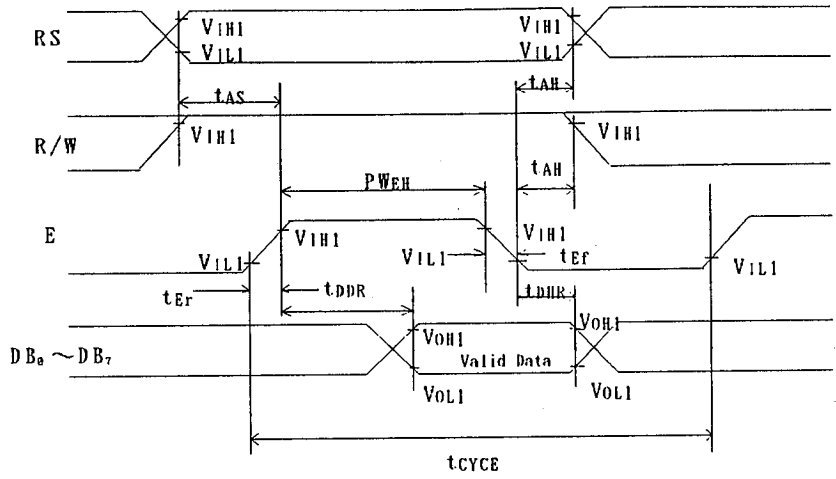



fig. 2

• Segment extension Timing Characteristics ($V_{DD}$ = 5.0V±10%, $V_{SS}$ = 0V, Ta = -20 ~ +75°C)

| PARAMETER | | SYMBOL | MIN | MAX | CONDITION | UNIT |
|---|---|---|---|---|---|---|
| Clock Pulse Width | "High" level | $t_{CWH}$ | 800 | | fig.3 | ns |
| | "Low" level | $P_{CWL}$ | 800 | | | |
| Clock Set up Time | | $t_{CSU}$ | 500 | | | |
| Data Set up Time | | $t_{SU}$ | 300 | | | |
| Data Hold Time | | $t_{DH}$ | 300 | | | |
| M Delay Time | | $t_{DM}$ | -1000 | 1000 | | |
| Clock rise Time, Fall Time | | $t_{ct}$ | | 100 | | |

Interface signals with extension driver NJU6407C

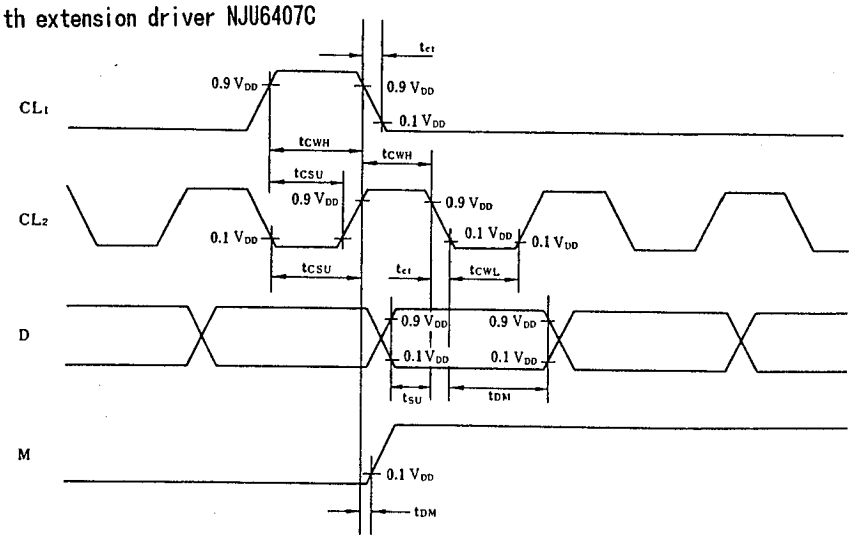
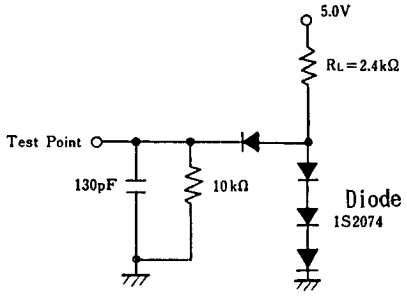
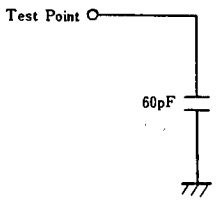



fig.3

$DB_0$ to $DB_7$ load circuit



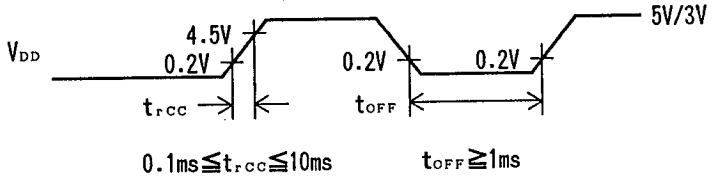

Segment extension signal load circuit




• Power Supply Condition when using the internal initialization circuit(Ta = -20 ~ +75℃)

| PARAMETER | SYMBOL | MIN | MAX | CONDITION | UNIT |
|---|---|---|---|---|---|
| Power Supply Rise Time | $t_{rcc}$ | 0.1 | 10 | | ms |
| Power Supply OFF Time | $t_{OFF}$ | 1 | | | |

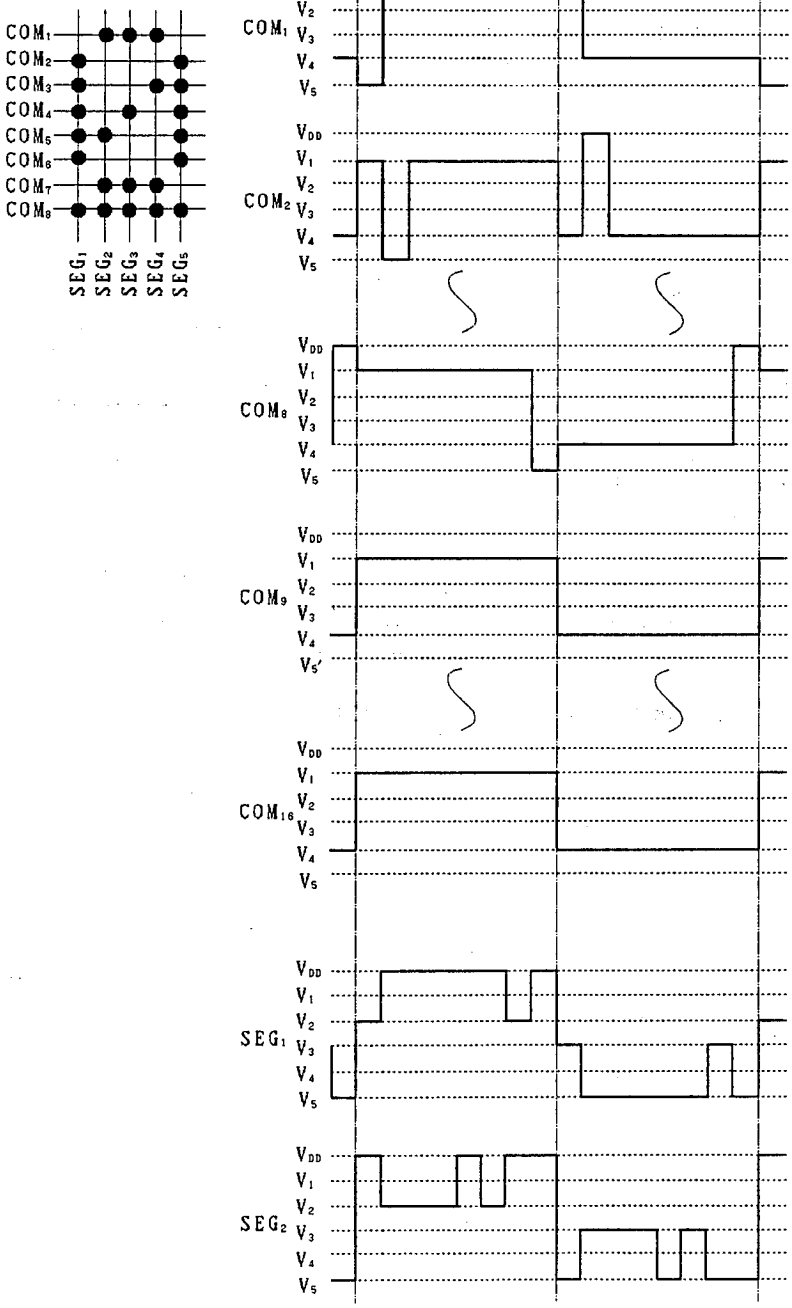
Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction.
(Refer to initialization by the instruction)




$t_{OFF}$ specifies the power off time in a short period off or cyclical on/off.

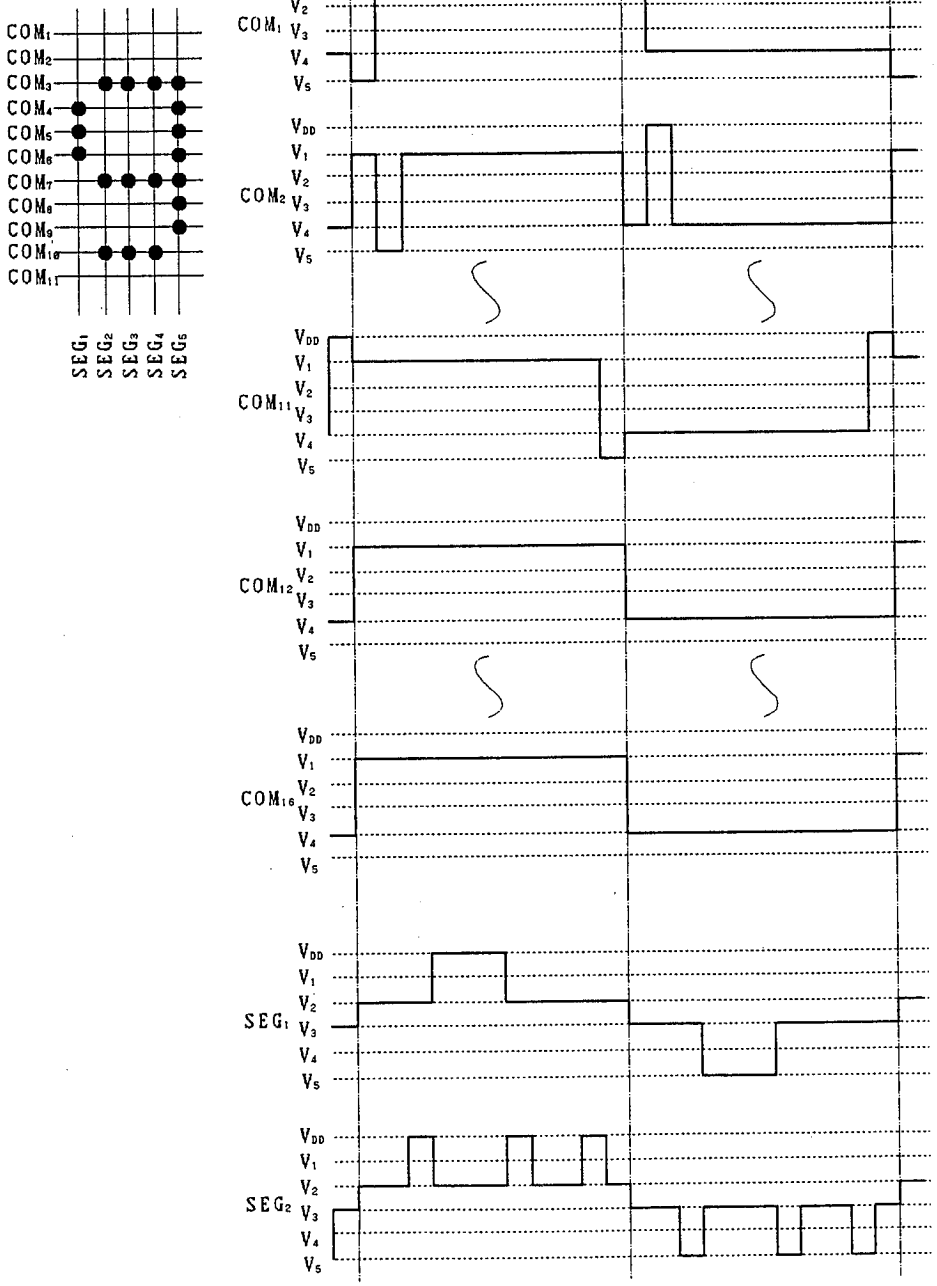
■ LCD DRIVING WAVE FORM

1/8 Duty Driving



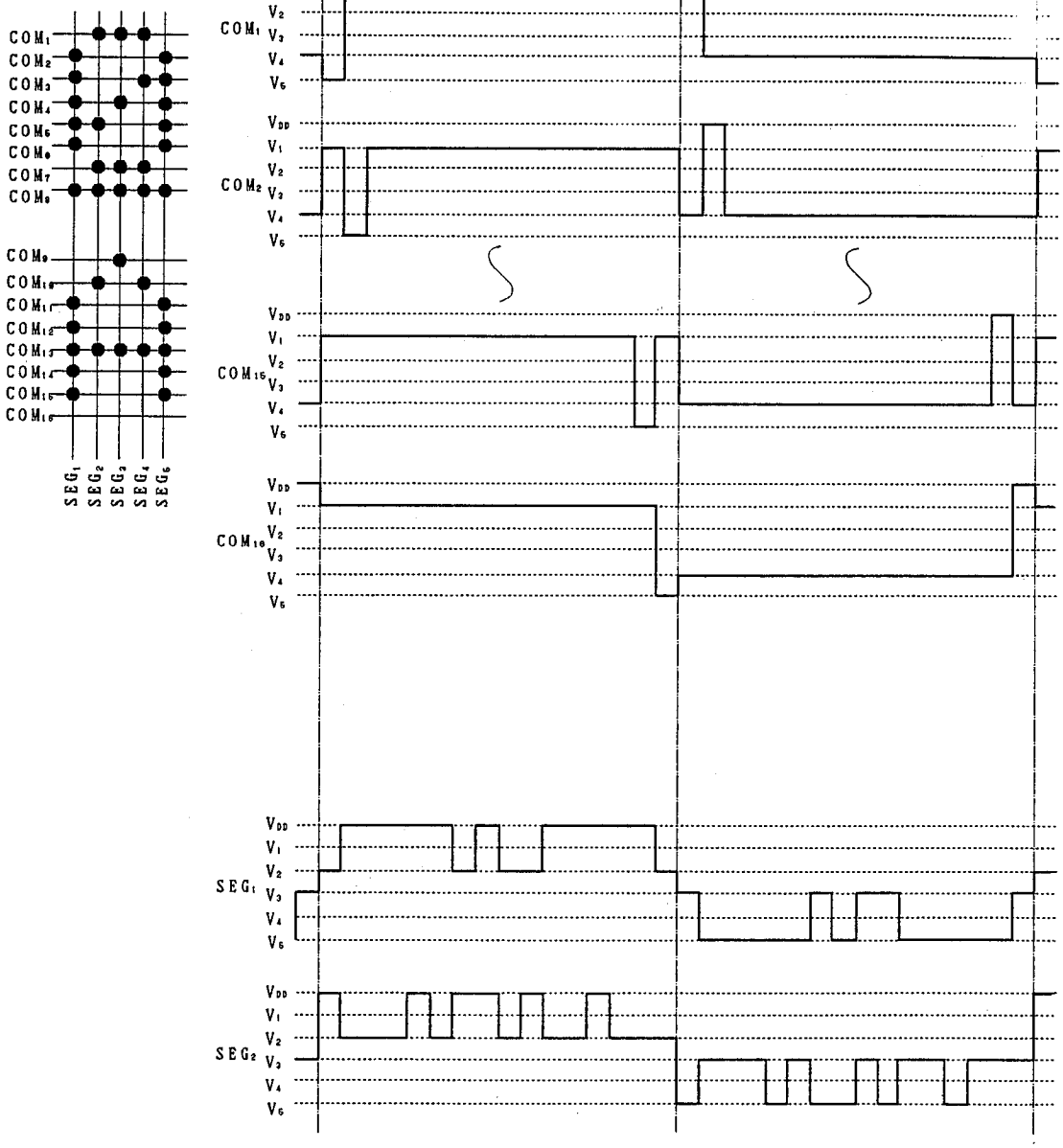
■ LCD DRIVING WAVE FORM

1/11 Duty Driving



■ LCD DRIVING WAVE FORM

1/16 Duty Driving



## ■ APPLICATION CIRCUITS

### (1) Interface with LCD Panel

#### (1−1) Character and Number of Display Line

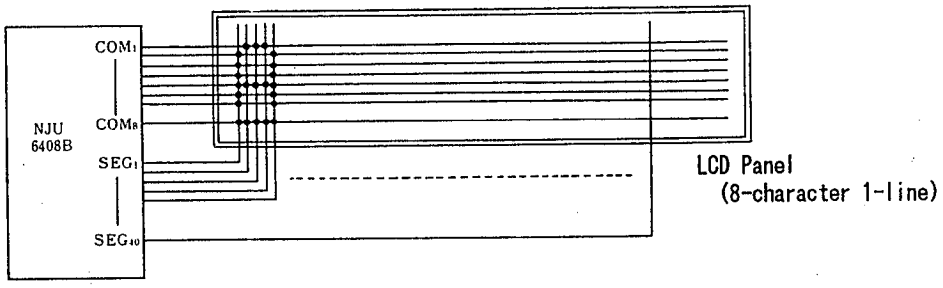
The NJU6408B can display both of 5 x 7 dots font with cursor and 5 x 10 dots font with cursor.

The number of display line is up to two lines for 5 x 7 dots font and one line for 5 x 10 dots font. Therefore, the common line must be of the following 3 types according to the line number and font combination.

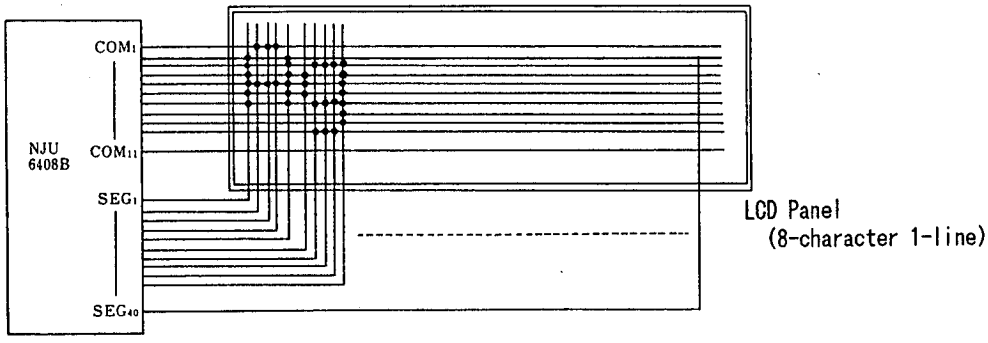
| Line Number | Character Font | Common Line | Duty Ratio |
|---|---|---|---|
| 1 | 5 x 7 dots + Cursor | 8 | 1/8 |
| 1 | 5 x 10 dots + Cursor | 11 | 1/11 |
| 2 | 5 x 7 dots + Cursor | 16 | 1/16 |

Display line number and character font can be selected by the user programing (refer Table 4.).

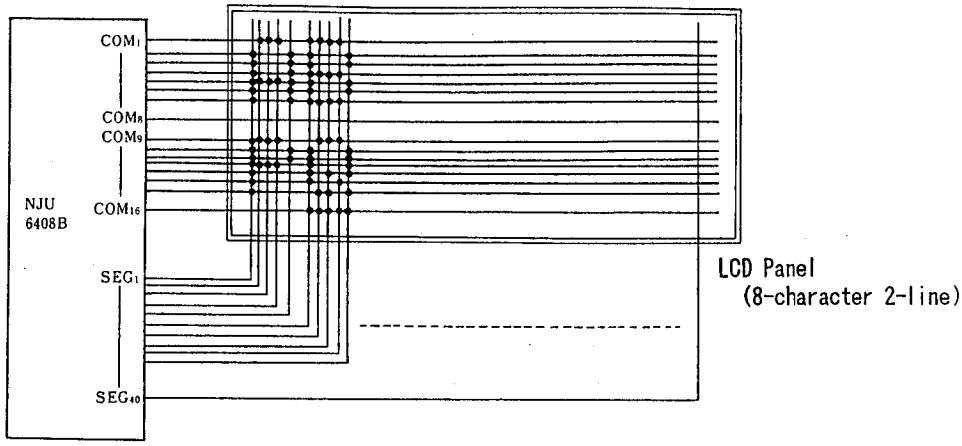
#### (1−2) Connection between NJU6408B and LCD panel




(a) 5x7 Dot 8-character 1-line example (1/4 bias,1/8 duty)




(b) 5x10 Dot 8-character 1-line example (1/4 bias,1/11 duty)



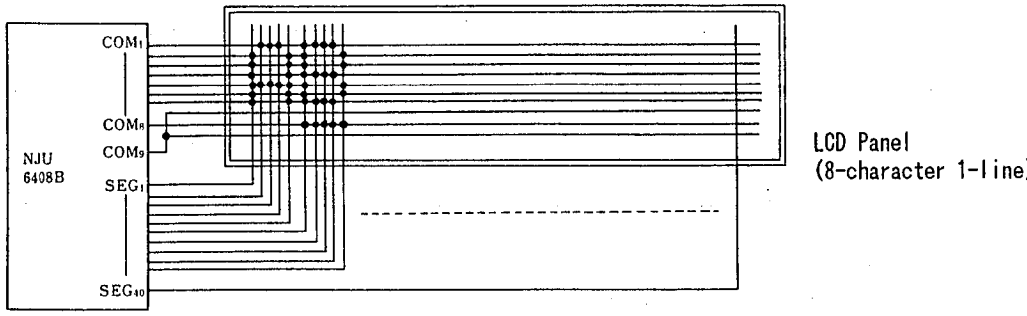

(c) 5x7 Dot 8-character 2-line example (1/5 bias,1/16 duty)

One NJU6408B can drives up to 8 characters for one line and up to 16 characters for two lines because of 1 character is driven by 5 segment lines.

Unused common terminals mentioned in the above example (a) and (b) always output non-select signals.

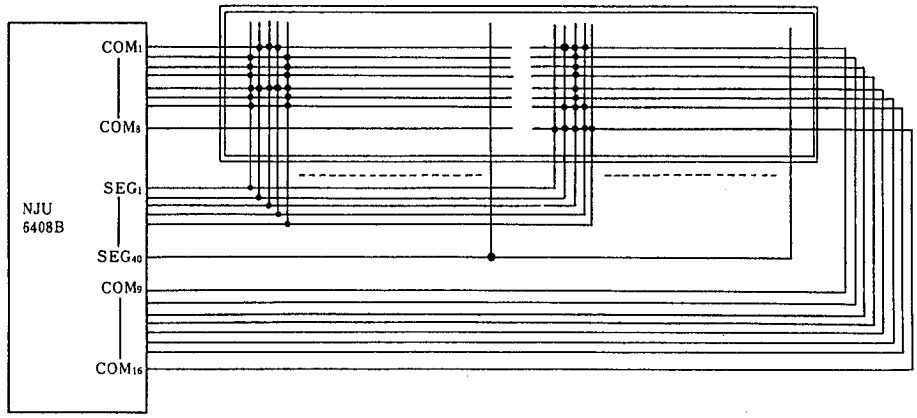
If the LCD panel has unused column electrode, following connection can avoid bad influence of cross-talk etc. occurred by floating condition.

5

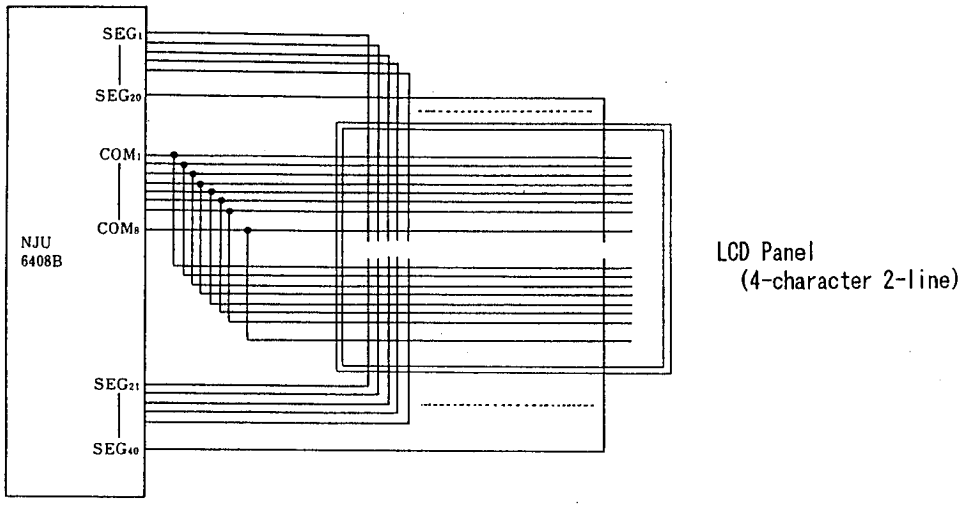



### (1−3) Other matrix LCD panel connection example

Following 16-character 1-line and 4-character 2-line displays are also available.




(a) 5x7 16-character 1-line example (1/5 bias,1/16 duty)




(b) 5x7 4-character 2-line example (1/4 bias,1/8 duty)

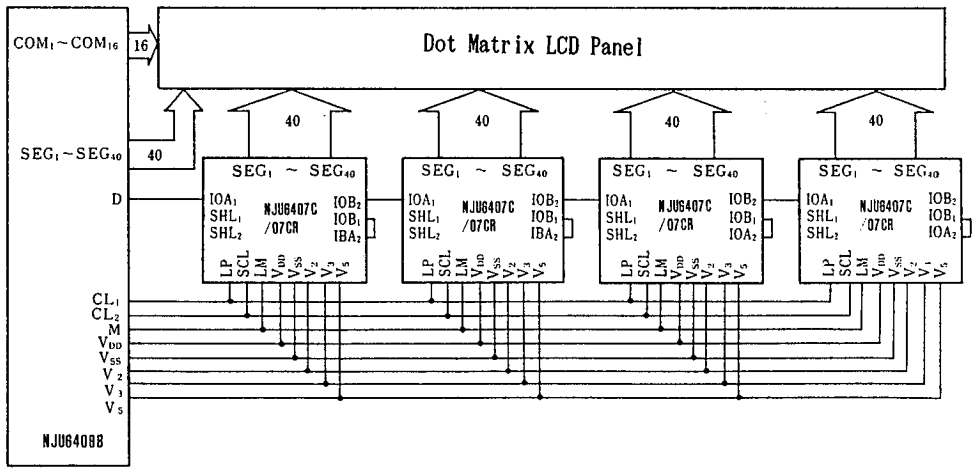
**(2) Connection with extension driver NJU6407C example**
(40 character 2-line Display NJU6408B + NJU6407C x 4)

The NJU6408B can extend its display capacity by connecting NJU6407C as extension Driver. In this application, the NJU6407C is used as a segment driver.

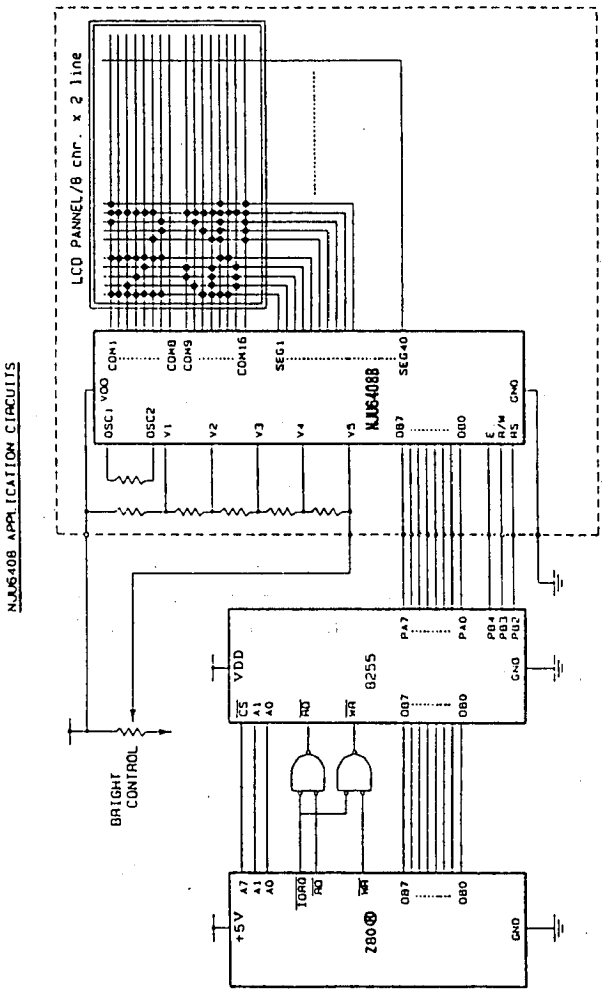
The control signal $CL_1$, $CL_2$, M and D for NJU6407C are supplied from the NJU6408B and power source is common with NJU6408B.

The maximum connecting unit number of NJU6407C is up to 9 for one line display (duty ratio 1/8 or 1/11) and up to 4 for 2 lines display (duty ratio 1/16). The maximum display capacity is limited to 80 characters which is the maximum memory capacity of NJU6408B.

1-line display, 2-line display, 5 x 7 dots font and 5 x 10 dots font application require same connections shown below.



(3) 8-bit MPU interface example ( Full application circuits )

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MEMO

NJR:

NJU6408BFC1-06A NJU6408BFC1-00A NJU6408BFC1 NJU6408BFG1 NJU6408BFC1-01 NJU6408BFC1-02 NJU6408BFC1-07 NJU6408BFC1-00 NJU6408BFC1-01A