PRELIMINARY

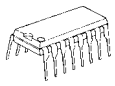
4-BIT SINGLE CHIP TINY CONTROLLER

■ GENERAL DESCRIPTION

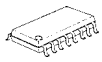
The **NJU3101** is the C-MOS 4-bit Single Chip Tiny Controller consisting of the 4-bit CPU Core, Input / Output Selectable I/O ports, Program ROM, Data RAM, and Oscillator Circuit (CR or Ceramic or X'tal). It is packaged in 16-pin package (DIP or DMP form). Therefore it provides a cost and space effective replacement with only few external components for control-logic circuit using standard logic ICs (i.e. 74HC) or other small controllers.

The **NJU3101** is suitable for battery operated appliances because of low operating current, wide operating voltage range, and STANDBY function (HALT mode).

■ PACKAGE OUTLINE



NJU3101D

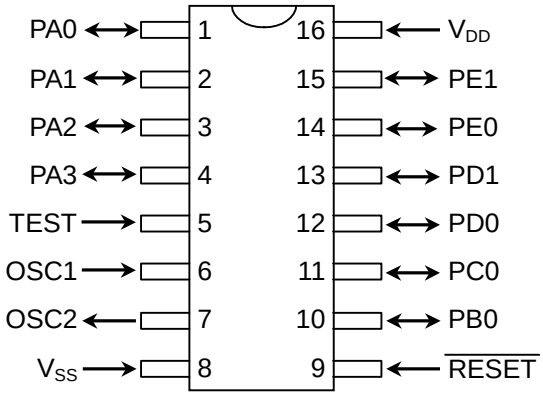


NJU3101M

■ FEATURES

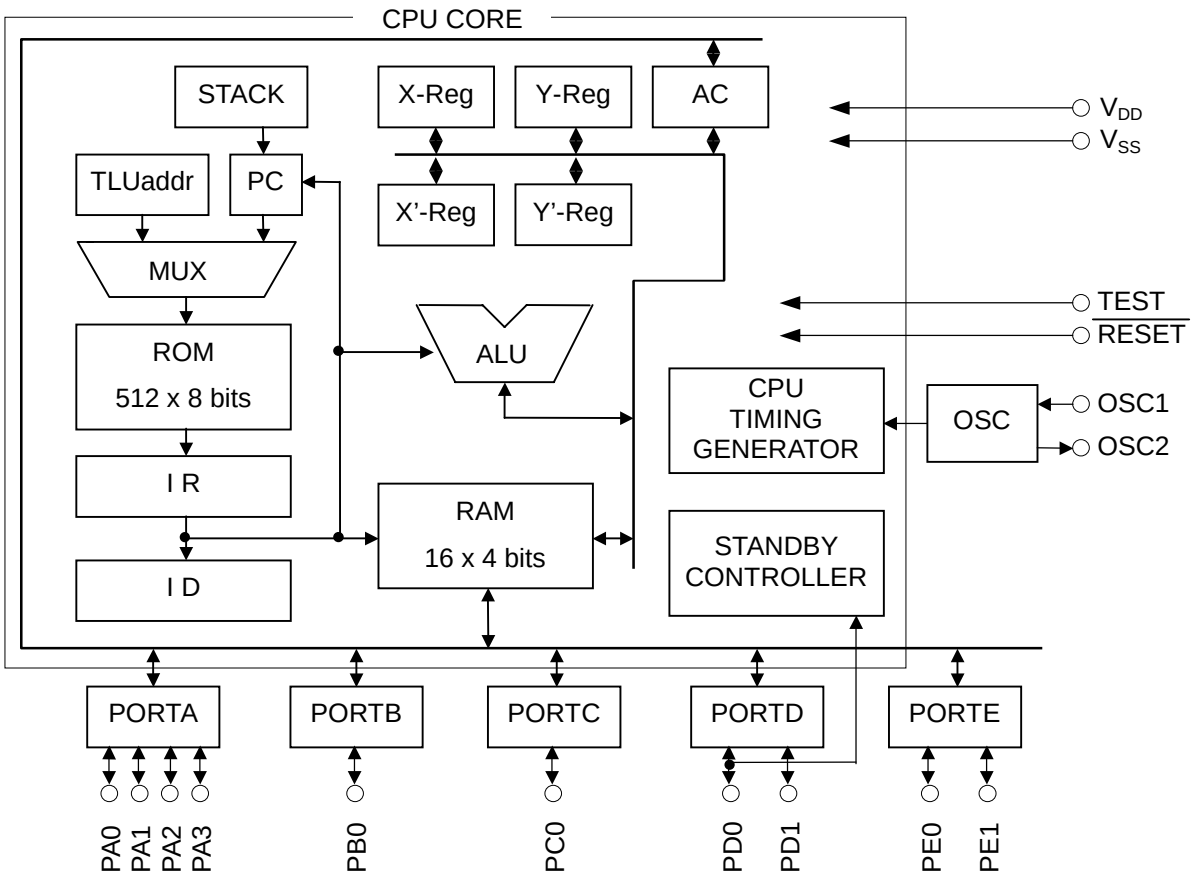
- Internal Program ROM 512 X 8 bits
- Internal Data RAM 16 X 4 bits
- Input / Output Port 10 lines
  (Input / Output direction of each PORT is selected by the mask option.)
- High Output Current terminal (2 lines)
  N-Channel FET Open Drain Type (I_{OL})
  15mA at V_{DD}=5V
- Instruction Set 58 instructions
- Subroutine Nesting 8 levels
- Pulse Edge Detector
  The rising or falling edge of a pulse is selected by the mask option.
- Instruction Executing Time $6/f_{OSC}$ sec
- Operating Frequency Range 30kHz – 4MHz
- Internal Oscillator
  CR, or Ceramic, or X'tal oscillation and External clock input
- STANDBY function (HALT mode)
- Wide operating voltage range 2.4V – 5.5V
- C-MOS technology
- Package outline DIP16 / DMP16

■ PIN CONFIGURATION



26/Mar/2001

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	INPUT/OUTPUT	F U N C T I O N
1 2 3 4	PA0 PA1 PA2 PA3	INPUT/OUTPUT INPUT/OUTPUT INPUT/OUTPUT INPUT/OUTPUT	4-bit Input / Output PORTA. Selects a terminal circuit for PORT grouped with 4 lines from follows by the mask option. • C-MOS Input Terminal with Pull-up Resistance(IA) • C-MOS Input Terminal(IC) • C-MOS Output Terminal(OB)
5	TEST	INPUT	Maker Testing Terminal with Pull-down Resistance The terminal is recommended to connect to GND.
6 7	OSC1 OSC2	INPUT OUTPUT	Internal Oscillator Terminals. Connects a device selected from the ceramic or the crystal resonator, or the resistor, to these terminals for the internal oscillator. In the external clock operation, OSC1 is the external clock input terminal and OSC2 is normally open terminal.
8	V_{SS}	–	Power Source (0V)
9	$\overline{\text{RESET}}$	INPUT	RESET Terminal. When the low level input-signal, the system is initialized.
10 11	PB0 PC0	INPUT/OUTPUT INPUT/OUTPUT	1-bit Input / Output PORTB and PORTC. Selects a terminal circuit for each PORT from follows by the mask option. • C-MOS Input Terminal with Pull-up Resistance(IA) • C-MOS Input Terminal(IC) • Nch-FET Open-Drain Output Terminal with Pull-up Resistance(OA) • Nch-FET Open-Drain Output Terminal(OC)
12 13	PD0 PD1	INPUT/OUTPUT	2-bit Input / Output PORTD. Selects a terminal circuit for PORT grouped with 2 lines from follows by the mask option. • C-MOS Input Terminal with Pull-up Resistance(IA) • C-MOS Input Terminal(IC) • C-MOS Output Terminal(OB) When the ports are selected as the input terminal, PD0 operates also as RESTART signal input terminal to return from STANDBY mode, and PD1 operates also as the Edge Detector Terminal.
14 15	PE0 PE1	INPUT/OUTPUT INPUT/OUTPUT	2-bit Input / Output PORTE. Selects a terminal circuit for PORT grouped with 2 lines from follows by the mask option. • C-MOS Schmitt Trigger Input Terminal with Pull-up Resistance(IB) • C-MOS Schmitt Trigger Input Terminal(ID) • C-MOS Output Terminal(OB)
16	V_{DD}	–	Power Source (2.4V – 5.5V)

Note) INPUT/OUTPUT : Input or Output is selected by the mask option.

■ INTERNAL SYSTEM DESCRIPTION

The **NJU3101** is a C-MOS 4-Bit Single Chip Tiny Controller consisted of Original CPU Core, Selectable Input-Output(I/O) Ports(MAX. 10 lines), Program ROM(512 bytes), Data RAM(16 nibbles), and Oscillator Circuit which can select a type from four oscillators types(i.e. Ceramic or X'tal or CR oscillation or External clock operation).

The CPU block in the **NJU3101** is consisted of ALU(Arithmetic Logic Unit) executing the binary adding, subtracting or logical calculating, AC(Accumulator), four Registers, STACK allowing the 8-level subroutine-nesting, Program Counter indicating 512 addresses sequentially, and Timing generator.

The **NJU3101** can be applied to the various markets because of the rich and efficient instruction set(58 instructions), wide operating voltage range(2.4V to 5.5V), low operating current, and STANDBY function reducing the power supply current.

(1) INTERNAL REGISTER

- Accumulator(AC)

  Accumulator(AC) is structured by the 4-bit register. It holds a data or a result of calculation, and executes the shift-operation(ROTATE) or the data transference between the other registers and Data Memory(RAM).

  Accumulator condition is unknown on the “RESET” operation.

- X-register(X-reg)

  X-register(X-reg) operates as the 4-bit register.

  The X-reg condition is unknown on the “RESET” operation.

- Y-register(Y-reg)

  Y-register(Y-reg) operates as the 4-bit register or the RAM address pointer.

  The Y-reg condition is unknown on the “RESET” operation.

- X'-register(X'-reg)

  X'-register(X'-reg) operates as the 4-bit register or a part of Program Memory(ROM) address pointer for looking data in the ROM(TRM instruction) up function.

  The X’-reg condition is unknown on the “RESET” operation.

- Y'-register(Y'-reg)

  Y'-register(Y'-reg) operates as the 4-bit register or the peripheral register number(PHYn) pointer.

  The Y’-reg condition is unknown on the “RESET” operation.

(2) INTERNAL FLAG

- RPC flag(RPC)

  RPC flag(RPC) changes the instruction table. Several instructions perform either of the dual tasks in accordance with the RPC flag condition. The RPC flag condition selects either of two couples of registers which are X- and Y-reg, or X'- and Y'-reg. X- or Y-reg is selected when the RPC flag condition is "0"(RPC=0). X'- or Y'-reg is selected when the RPC flag condition is "1"(RPC=1). The RPC flag condition is set to "1"(RPC=1) by SRPC instruction, and is set to “0”(RPC=0) by RRPC instruction.

  The RPC flag condition is set to “0” on the “RESET” operation.

- CARRY flag(CY)

  When the carry occurs after the adding calculation, the CARRY flag(CY) condition is set to "1"(CY=1), and when no carry, the CY flag condition is set to "0"(CY=0). When the borrow occurs after the subtracting calculation, the CY flag condition is set to "0"(CY=0), and when no borrow, the CY flag condition is set to "1"(CY=1). The bit-operation instruction operates the bit data rotation on the CY flag combined with Accumulator or the other register.

  The CY flag condition is set to "1"(CY=1) by SEC instruction and is set to "0"(CY=0) by CLC instruction. The CY flag condition is kept until the end of the next instruction executing cycle. The CY flag condition is unknown on the “RESET” operation.

- STATUS flag(ST)

STATUS flag(ST) is the conditional flag in accordance with the result of the instruction execution. Its condition is in accordance with follows:

1) to be same as CY flag condition.
2) to be set the condition to "0"(ST=0) when the result of the logical calculation(AND, OR, XOR, YNEA) is zero.
3) to be set the condition to "0"(ST=0) when the result of the comparison(CMP) is zero.

However, ST flag condition is always set to "1"(ST=1) except above three.

ST flag controls the branch operation. Branch instruction does not branch when ST flag condition is "0", and branches when ST flag condition is "1". ST flag condition is kept until the end of the next instruction executing cycle.

The ST flag condition is unknown on the “RESET” operation.

(3) FUNCTIONAL BLOCK

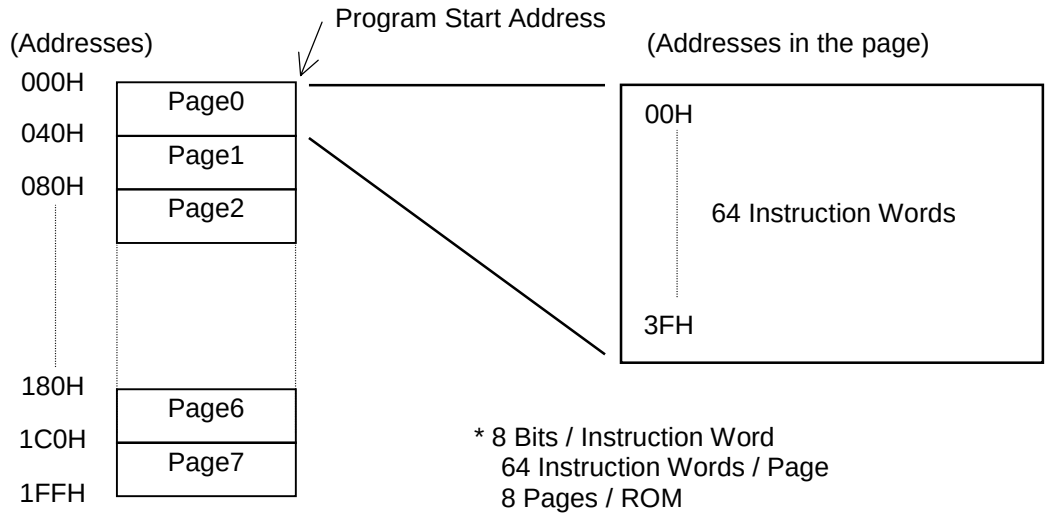
- ARITHMETIC LOGIC UNIT(ALU)

ARITHMETIC LOGIC UNIT(ALU) is a 4-bit binary paralleled calculation circuit operating binary addition, binary subtraction, comparison, logical AND, logical OR, exclusive OR, and SHIFT(Rotation). And it also can detect CARRY, BORROW or ZERO in accordance with the result of each calculation.

- PROGRAM MEMORY(ROM)

PROGRAM MEMORY(ROM) consists of 8 pages, and a page consists of 64 bytes memory capacity. Therefore the **NJU3101** prepares the 512-byte ROM for the application program. The ROM address is indicated by the Program Counter(PC).

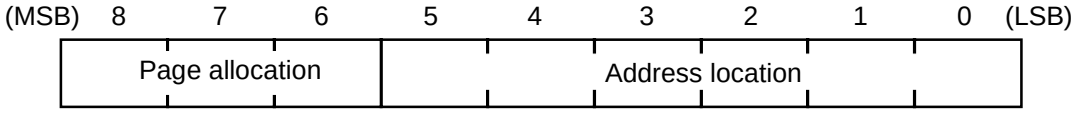
[PROGRAM MEMORY AREA]



- PROGRAM COUNTER(PC)

PROGRAM COUNTER(PC) consisted of the 9-bit binary counter stores the address for the next operating instruction in ROM. Data figures limited from b0 to b5 on the PC indicate the address in a page, and data figures limited from b6 to b8 on the PC indicate the page in ROM. Although the ROM address can be indicated 512 addresses continuously, the target address of JMP instruction is restricted by Paging structure in ROM.

The PC condition is set to “0” on the “RESET” operation.

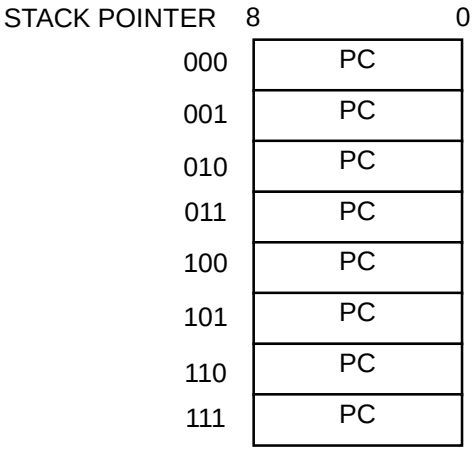


JMP instruction can branch to the optional address in the page. The target address is indicated by the data figures limited from b0 to b5(6 bits) on PC as shown in above. The paging structure can reduce the program size in ROM and the JMP instruction execution time against JPL instruction because JMP instruction is consisted of one byte(8 bits) length. JPL and CALL instructions can branch to the optional address without considering the paging structure, because they consist of two bytes(16 bits) length including the 9 bits of PC.

- STACK

STACK consists of the 8 by 9 bits registers. It holds the data of PC automatically when the subroutine call (CALL). PC gets the held data from STACK when the return (RET) operation.

[Structure of STACK]



- STACK POINTER(SP)

STACK POINTER(SP) consists of the 3 bits binary counter. SP indicates the number of next operating position in the STACK. It counts one up(increment) after the subroutine call(CALL), and it counts one down(decrement) after the return(RET) operation.

Data storing operation to STACK after that SP overflowed(over than 7) or under flowed(under than 0), breaks the former held data in STACK. Therefore the subroutine nesting level must be cautioned in the application program.

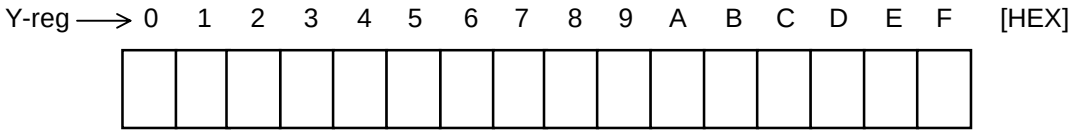
SP condition is set to "0" on “RESET” operation.

- DATA MEMORY(RAM)

DATA MEMORY(RAM) is formed with the 4-bit length a word. The **NJU3101** prepares 16 words(64 bits) RAM. The data formed with the 4-bit length a word can be read/written from/to RAM, and the data formed with the 1-bit length in a word can be set, reset, or tested by the bit-operation instruction.

The RAM address is indicated indirectly by Y-reg.

[RAM ADDRESS MAP]



- PERIPHERAL REGISTERs(PH)

PERIPHERAL REGISTERs(PH) controlling I/O Ports or the ROM address are selected by the data in Y'-reg.

The Peripheral Register assigned for each I/O Port can get the signal data from the external application by reading operation, or can output the signal data to the external application by writing operation in accordance with the type of input or output selected by the mask option. Although the data can be read from the Peripheral Register assigned as the Output, it sometimes takes the incorrect data of the Output Port.

[PERIPHERAL REGISTER TABLE]

Y'-register	Register No.	Peripheral Register Name
1H	PHY1	PORTA Output or PORTA Input
2H	PHY2	PORTB Output or PORTB Input
3H	PHY3	PORTC Output or PORTC Input
4H	PHY4	PORTD Output or PORTD Input
5H	PHY5	PORTE Output or PORTE Input
DH	PHY13	ROM Addressing Register

- ROM ADDRESSING REGISTER(PHY13)

ROM ADDRESSING REGISTER(PHY13) indicates the address of ROM with Accumulator and X'-reg for the data transference operation(TRM) from ROM to RAM. The effective bit on ROM Addressing Register(PHY13) is b0, and the other three bits, b1, b2 and b3, are not related.

The PHY13 condition is unknown on “RESET” operation.

[ROM ADDRESSING]

no used			A8	A7	A6	A5	A4	A3	A2	A1	A0
b3	b2	b1	b0	b3	b2	b1	b0	b3	b2	b1	b0
PHY13				X'				AC			

■ INPUT OUTPUT PORT

The **NJU3101** prepares 10 Input-Output lines maximum for the interface to an external application circuit. All lines are assigned to each Peripheral Register, and are shared to five groups which are PORTA, PORTB, PORTC, PORTD, and PORTE.

Data reading operation from the peripheral register can input the actual signal through the input terminal. Data writing operation to the peripheral register can output the actual signal through the output terminal. All terminals can select the direction of input or output of each PORT by the mask option.(refer ■INPUT OUTPUT TERMINAL TYPE)

[The read conditions from the assigned peripheral register as output]

Port / PHYn	Output Terminal Types	Read Data of Peripheral Register b3	b2	b1	b0
A / PHY1	C-MOS Output	*	*	*	*
B / PHY2	N-channel FET OPEN-DRAIN Output With Pull-Up Resistance	0	0	0	*
	N-channel FET OPEN-DRAIN Output	0	0	0	1
C / PHY3	N-channel FET OPEN-DRAIN Output With Pull-Up Resistance	0	0	0	*
	N-channel FET OPEN-DRAIN Output	0	0	0	1
D / PHY4	C-MOS Output	0	0	*	*
E / PHY5	C-MOS Output	0	0	*	*

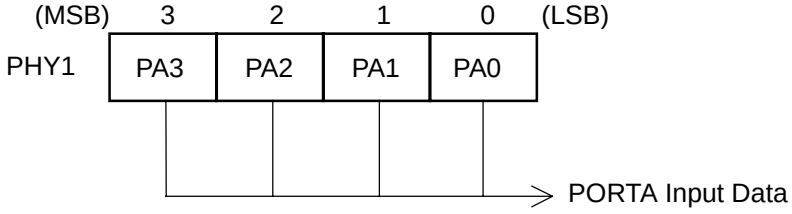
* : Output Terminal data

(1) INPUT OUTPUT PORT

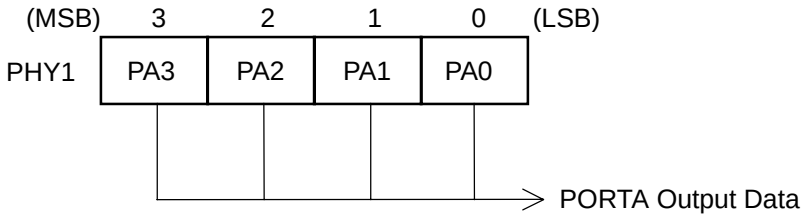
- PORTA(PA0–PA3)

PORTA is a 4-bit input-output PORT. When the PORT is set as the output, the signal is output through the output terminal by writing data to the PORTA register(PHY1). When the PORT is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY1.

[READING PORTA INPUT DATA (PHY1)]



[WRITING PORTA OUTPUT DATA (PHY1)]

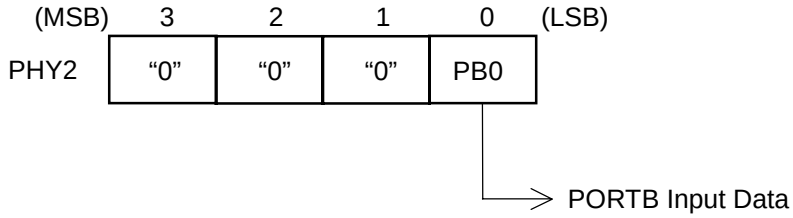


- PORTB(PB0)

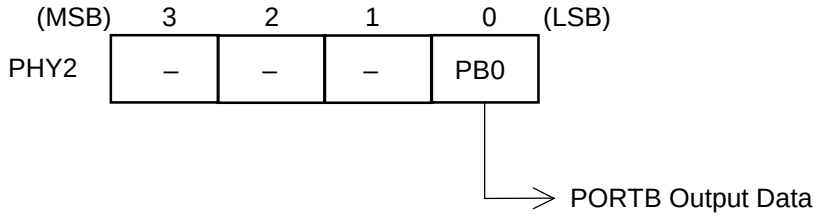
PORTB is a 1-bit input-output PORT. When the PORT is set as the output, the signal is output through the output terminal by writing data to the PORTB register(PHY2). When the PORT is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY2.

Though the output circuit is Nch open drain type, the C-MOS input buffer is connected to the same terminal. Therefore, the operating current of the chip by the short circuit current when the middle level voltage between V_{DD} and V_{SS} is input to this terminal.

[READING PORTB INPUT DATA (PHY2)]



[WRITING PORTB OUTPUT DATA (PHY2)]

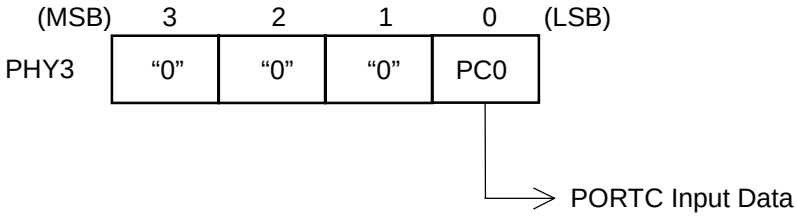


- PORTC(PC0)

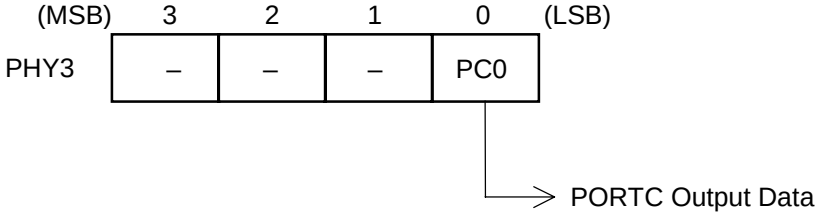
PORTC is a 1-bit input-output PORT. When the PORT is set as the output, the signal is output through the output terminal by writing data to the PORTC register(PHY3). When the PORT is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY3.

Though the output circuit is Nch open drain type, the C-MOS input buffer is connected to the same terminal. Therefore, the operating current of the chip by the short circuit current when the middle level voltage between V_{DD} and V_{SS} is input to this terminal.

[READING PORTC INPUT DATA (PHY3)]



[WRITING PORTC OUTPUT DATA (PHY3)]



- PORTD(PD0, PD1)

PORTD is a 2-bit input-output PORT. When the PORT is set as the output, the signal is output through the output terminal by writing data to the PORTD register(PHY4). When the PORT is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY4.

When this PORTD is set as the input, these two ports perform the extra functions as follows:

a) PD0 TERMINAL

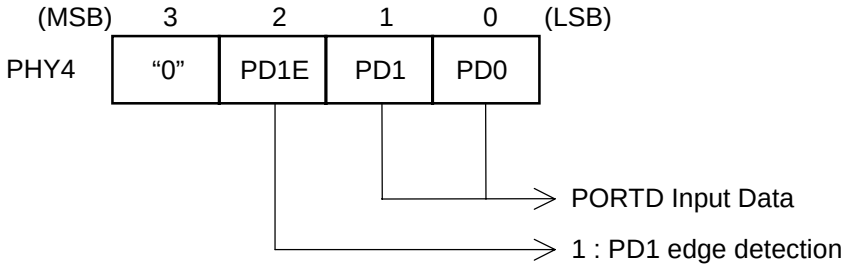
PD0 TERMINAL performs the extra function as the restart signal input terminal to return from the "STANDBY" mode. When the rising edge of the signal from the external circuit is input into the PD0 terminal in mode of "STANDBY", the "STANDBY" mode is released and the CPU starts the execution again from the suspended address of the program. (refer ■STANDBY FUNCTION)

b) PD1 TERMINAL

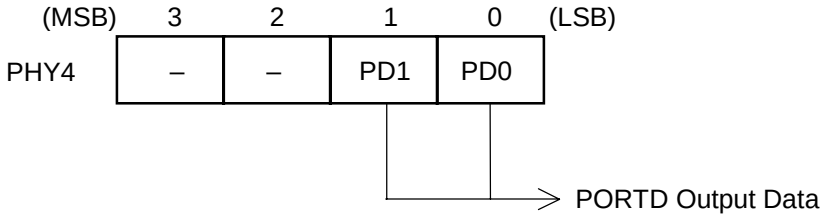
PD1 TERMINAL performs the extra function as the edge detector terminal. When the PD1 terminal detects the edge of the signal from the external circuit, the third bit(b2) condition of PHY4 is set to "1". The “b2” of PHY4 is set to “1” even when the edge is input during the “STANDBY” mode. The condition of “b2” is kept until the writing operation to PHY4.

The polarity as low to high or high to low of the input signal edge can be selected by the mask option.

[READING PORTD INPUT DATA (PHY4)]



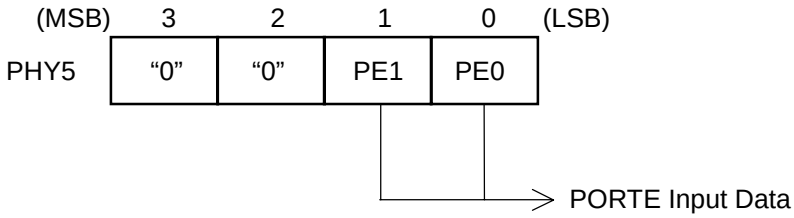
[WRITING PORTD OUTPUT DATA (PHY4)]



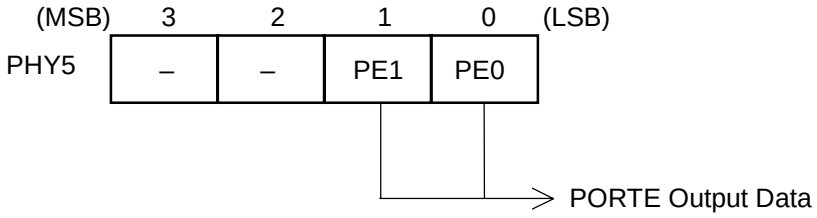
- PORTE(PE0, PE1)

PORTE is a 2-bit input-output PORT. When the PORT is set as the output, the signal is output through the output terminal by writing data to the PORTE register(PHY5). When the PORT is set as the input, the external signal is gotten directly through the input terminal by reading data from PHY5.

[READING PORTE INPUT DATA (PHY5)]



[WRITING PORTE OUTPUT DATA (PHY5)]



(2) INPUT OUTPUT PORT OPERATION

a) The output operation example

PA0 and PA1 of PORTA output “H”, and PA2 and PA3 of PORTA output “L”.

```
            :
            :
SRPC                ;
LDI         Y,1     ;PHY1 is pointed
LDI         A,%0011 ;"0011" is stored into Accumulator
TAP                 ;DATA in Accumulator is transmitted to PHY1
            :
            :
```

b) The input operation example

Accumulator gets the input data from PORTD and the bit of the edge detector is reset

```
            :
            :
SRPC                ;
LDI         Y,4     ;PHY4 is pointed
TPA                 ;The input data from PHY4 is transferred to Accumulator
TAP                 ;The bit(b2) of the edge detector is reset
            :
            :
```

The signal from PD0 terminal is stored into the bit0(b0) of Accumulator, the signal from PD1 terminal is stored into the bit1(b1) of Accumulator, the sign of the edge detector from PD1 terminal is stored into the bit2(b2) of Accumulator, and “zero” is stored into the bit3(b3) of Accumulator.

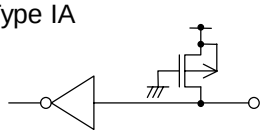
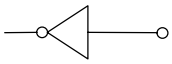
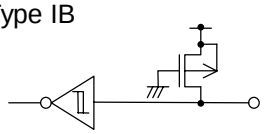
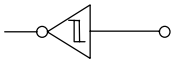
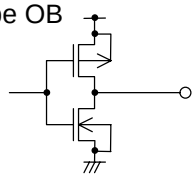
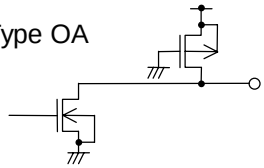
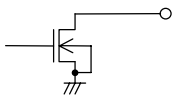
■ INPUT OUTPUT TERMINAL TYPE

PORTA, B, C, D, and E can select a terminal type for each PORT from the follows by the mask option which is the same mask of the program coding into ROM and the others.

- C-MOS OUTPUT (OB)
- N-channel FET OPEN-DRAIN OUTPUT (OC)
- N-channel FET OPEN-DRAIN OUTPUT WITH PULL-UP RESISTANCE (OA)

- C-MOS INPUT (IC)
- SCHMITT TRIGGER C-MOS INPUT (ID)
- C-MOS INPUT WITH PULL-UP RESISTANCE (IA)
- SCHMITT TRIGGER C-MOS INPUT WITH PULL-UP RESISTANCE (IB)

[INPUT OUTPUT TERMINAL TYPE]

	Types	With Pull-up	Without Pull-up	Terminals
INPUT TERMINAL	C-MOS	Type IA 	Type IC 	PA0–PA3, PB0, PC0, PD0, PD1
	SCHMITT TRIGGER	Type IB 	Type ID 	PE0, PE1
OUTPUT TERMINAL	C-MOS		Type OB 	PA0–PA3, PD0, PD1, PE0, PE1
	N-channel(Nch) OPEN DRAIN	Type OA 	Type OC 	PB0, PC0

■ STANDBY FUNCTION

STANDBY FUNCTION halts the IC operation and reduces the current consumption.

The STANDBY function starts by the HLT instruction. After the HLT instruction execution cycle, the internal oscillator operation is stopped and all of the operation is halted. In case of the external clock operation, the clock is stopped automatically delivering into the internal system by the internal circuit, and all of the operation is halted as same as the internal oscillator operation. This is STANDBY mode.

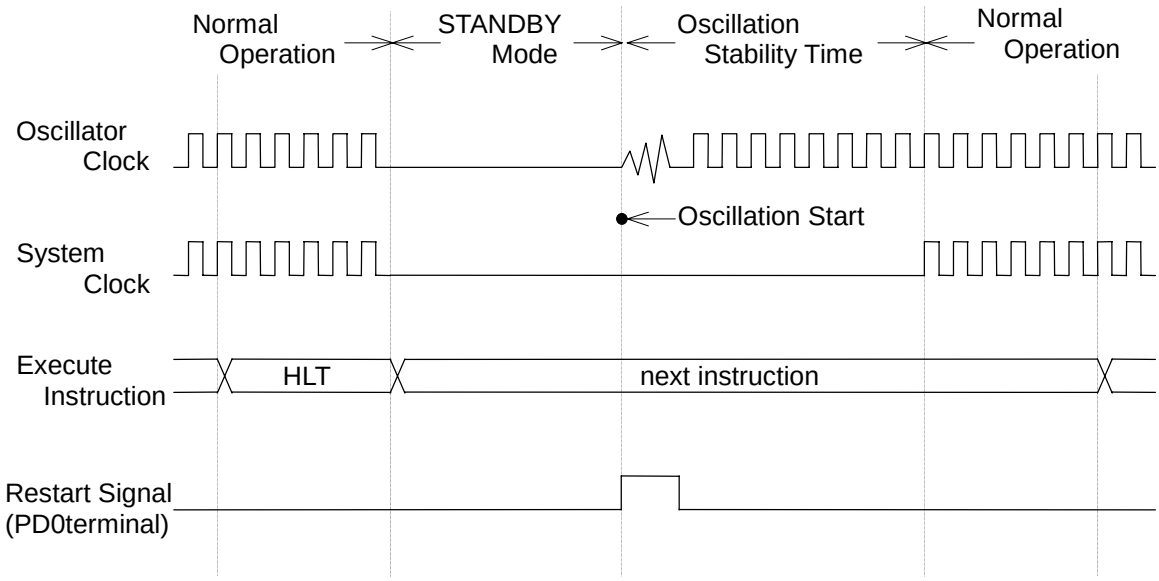
In the STANDBY mode, the operating current can be reduced. Though the clock into the internal system is stopped and all of the operation is halted, all conditions of Program Counter, Registers, and data in RAM are kept certainly.

Two ways to release from the STANDBY mode are prepared. One way is the reset operation that when the reset signal is input to RESET terminal, the operation starts from the initial condition. The other way is the re-start operation that when the restart signal is input to PD0 terminal, the operation starts from the kept Program Counter location which is the program address after the final operation. In case of the restart signal operation, if the rising signal, low to high, is input to PD0 terminal, the internal oscillator circuit starts at first. After the stabilized clock from the internal oscillator was counted eight times, the clock is started delivering into the internal system. Then the NJU3101 starts to operate from the kept Program Counter location with all of the kept conditions.(See *1)

In case of the external clock operation, the external clock must be started to supply to the OSC1 terminal before the STANDBY mode is released. The external clock is recommended to stop supplying to the OSC1 terminal for reducing the power consumption during the STANDBY mode.

*1: When the restart signal is input to PD0 terminal to release the STANDBY mode, PORTD must be selected as the input by the mask option.

[STANDBY MODE TIMING CHART]



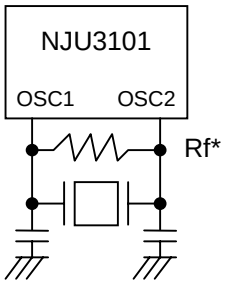
■ CLOCK GENERATION

The system clock is generated in the internal oscillator circuit with the external crystal or ceramic resonator, or the resistor connected to OSC1 and OSC2 terminals. Furthermore, the **NJU3101** can operate by the external clock to the OSC1 terminal for the system clock. In the external clock operation, the OSC2 terminal must be opened.

The typical application examples for each oscillator circuit are shown in follows. However a Crystal or a Ceramic operation requires the considered evaluation, because the oscillator operates in accordance with the characteristics of each component.

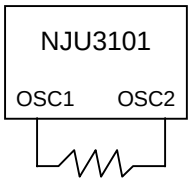
[OSCILLATOR APPLICATION EXAMPLES]

1) X'tal/Ceramic oscillation

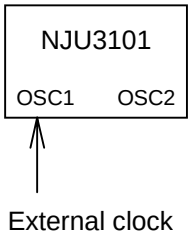


The resistor Rf* is sometimes required to connect when the Crystal operation.

2) CR oscillation



3) External clock input

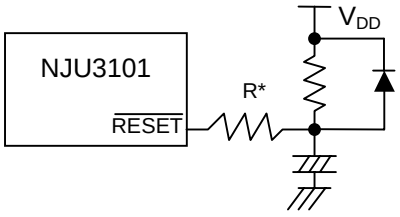


■ RESET OPERATION

All of the internal circuits are initialized by inputting the low level signal to the RESET terminal.

A circuit example for Power On Reset Operation with a resistor, a capacitor, and a diode is shown in bellow. Power On Reset Operation requires to keep the low level of the input signal to RESET terminal until the stabilized oscillation of the internal oscillator. Therefore the constants on the reset circuit must be decided in accordance with the characteristics of the clock generator circuit.

[An example of Power On Reset circuit]



R*:A resistor as RESET terminal protector. It is required depending on the condition of an application.

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

P A R A M E T E R	SYMBOL	R A T I N G S	UNIT
Supply Voltage	V_{DD}	-0.3 – +7.0	V
Input Voltage	V_{IN}	-0.3 – V_{DD}+0.3	V
Output Voltage	V_{OUT}	-0.3 – V_{DD}+0.3	V
Operating Temperature	T_{opr}	-20 – +75	°C
Storage Temperature	T_{stg}	-55 – +125	°C

■ ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS 1 (V_{DD}=4.5 – 5.5V, V_{SS}=0V, Ta=-20 – 75°C)

PARAMETER	SYMBOL	C O N D I T I O N S	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	V_{DD}	3.6		5.5	V	
Supply Current	I_{DD1}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz X'tal Oscillation In Reset		2.0	4.0	mA	*3
	I_{DD2}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz Ceramic Oscillation In Reset		2.0	4.0	mA	*3
	I_{DD3}	V_{DD} V_{DD}=5V, f_{OSC}=2MHz CR Oscillation In Reset		1.9	3.8	mA	*3
	I_{DD4}	V_{DD} V_{DD}=5V, STANDBY Mode			4.0	µA	*3
High-Level Input Voltage	V_{IH1}	PA0 – PA3, PB0, PC0, PD0, PD1	$0.7V_{DD}$		V_{DD}	V	*1
	V_{IH2}	PE0, PE1, $\overline{RESET}$	$0.8V_{DD}$		V_{DD}	V	*1
	V_{IH3}	OSC1	V_{DD}-1.0		V_{DD}	V	
Low-Level Input Voltage	V_{IL1}	PA0 – PA3, PB0, PC0, PD0, PD1	0		$0.3V_{DD}$	V	*1
	V_{IL2}	PE0, PE1, $\overline{RESET}$	0		$0.2V_{DD}$	V	*1
	V_{IL3}	OSC1	0		1.0	V	
High-Level Input Current	I_{IH}	V_{DD}=5.5V, V_{IN}=5.5V PA0 – PA3, PB0, PC0, PD0, PD1, PE0, PE1, $\overline{RESET}$			10	µA	*1
Low-Level Input Current	I_{IL1}	V_{DD}=5.5V, V_{IN}=0V Without Pull-up Resistance PA0 – PA3, PB0, PC0, PD0, PD1, PE0, PE1, $\overline{RESET}$			-10	µA	*1
	I_{IL2}	V_{DD}=5.5V, V_{IN}=0V With Pull-up Resistance PA0 – PA3, PB0, PC0, PD0, PD1, PE0, PE1			-100	µA	*1
High-Level Output Voltage	V_{OH}	I_{OH}=-100µA PA0 – PA3, PD0, PD1, PE0, PE1	V_{DD}-0.5			V	*2
Low-Level Output Voltage	V_{OL1}	I_{OL1}=400µA PA0 – PA3, PD0, PD1, PE0, PE1			0.5	V	*2
	V_{OL2}	I_{OL2}=15mA PB0, PC0			2.0	V	*2
Output Leakage Current	I_{OD}	V_{DD}=5.5V, V_{OH}=5.5V PB0, PC0			10	µA	*2
Input Capacitance	C_{IN}	Except V_{DD},V_{SS} terminals f_{OSC}=1MHz		10	20	pF	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

■ ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS 2 (V_{DD}=2.4 – 3.6V, V_{SS}=0V, Ta=-20 – 75°C)

PARAMETER	SYMBOL	C O N D I T I O N S	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD}	V_{DD}	2.4		3.6	V	
Supply Current	I_{DD1}	V_{DD} V_{DD}=3V, f_{OSC}=1MHz X'tal Oscillation In Reset		1.0	2.0	mA	*3
	I_{DD2}	V_{DD} V_{DD}=3V, f_{OSC}=1MHz Ceramic Oscillation In Reset		1.0	2.0	mA	*3
	I_{DD3}	V_{DD} V_{DD}=3V, f_{OSC}=1MHz CR Oscillation In Reset		0.9	1.8	mA	*3
	I_{DD4}	V_{DD} V_{DD}=3V, STANDBY Mode			2.0	µA	*3
High-Level Input Voltage	V_{IH1}	PA0 – PA3, PB0, PC0, PD0, PD1	$0.8V_{DD}$		V_{DD}	V	*1
	V_{IH2}	PE0, PE1, $\overline{RESET}$	$0.85V_{DD}$		V_{DD}	V	*1
	V_{IH3}	OSC1	V_{DD}-0.3		V_{DD}	V	
Low-Level Input Voltage	V_{IL1}	PA0 – PA3, PB0, PC0, PD0, PD1	0		$0.2V_{DD}$	V	*1
	V_{IL2}	PE0, PE1, $\overline{RESET}$	0		$0.15V_{DD}$	V	*1
	V_{IL3}	OSC1	0		0.3	V	
High-Level Input Current	I_{IH}	V_{DD}=3.6V, V_{IN}=3.6V PA0 – PA3, PB0, PC0, PD0, PD1, PE0, PE1, $\overline{RESET}$			10	µA	*1
Low-Level Input Current	I_{IL1}	V_{DD}=3.6V, V_{IN}=0V Without Pull-up Resistance PA0 – PA3, PB0, PC0, PD0, PD1, PE0, PE1, $\overline{RESET}$			-10	µA	*1
	I_{IL2}	V_{DD}=3.6V, V_{IN}=0V With Pull-up Resistance PA0 – PA3, PB0, PC0, PD0, PD1, PE0, PE1			-100	µA	*1
High-Level Output Voltage	V_{OH}	I_{OH}=-80µA PA0 – PA3, PD0, PD1, PE0, PE1	V_{DD}-0.5			V	*2
Low-Level Output Voltage	V_{OL1}	I_{OL1}=350µA PA0 – PA3, PD0, PD1, PE0, PE1			0.5	V	*2
	V_{OL2}	I_{OL2}=5mA PB0, PC0			1.0	V	*2
Output Leakage Current	I_{OD}	V_{DD}=3.6V, V_{OH}=3.6V PB0, PC0			10	µA	*2
Input Capacitance	C_{IN}	Except V_{DD}, V_{SS} terminals f_{OSC}=1MHz		10	20	pF	

*1 Input/output port is set as an Input terminal.
*2 Input/output port is set as an Output terminal.
*3 Except the current through Pull-up resister.

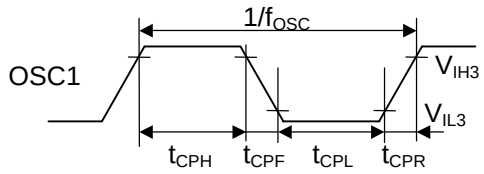
■ ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS (V_{SS}=0V, Ta=-20 – 75°C)

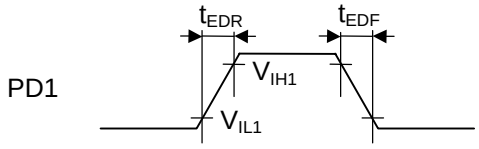
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Operating Frequency	f_{OSC}	V_{DD}=2.4 – 3.6V	X'tal Oscillation	30K		2.0M	Hz
			Ceramic Oscillation	30K		2.0M	
			Resistor Oscillation	30K		1.0M	
			External Clock	30K		2.0M	
		V_{DD}=3.6 – 5.5V	X'tal Oscillation	30K		4.0M	
			Ceramic Oscillation	30K		4.0M	
			Resistor Oscillation	30K		2.0M	
			External Clock	30K		4.0M	
Instruction Cycle Time	t_C				$6/f_{OSC}$		s
External Clock Pulse Width	t_{CPH}	V_{DD}=2.4 – 3.6V		250n		16.6µ	s
	t_{CPL}	V_{DD}=3.6 – 5.5V		125n		16.6µ	
External Clock Rise Time Fall Time	t_{CPR} t_{CPF}	V_{DD}=2.4 – 5.5V				20	ns
$\overline{\text{RESET}}$ Low-Level Width	t_{RST}	V_{DD}=2.4 – 5.5V		$4/f_{OSC}$			s
$\overline{\text{RESET}}$ Rise Time	t_{RSR}	V_{DD}=2.4 – 5.5V				20	ms
Port Input Level Width	t_{PIN}	V_{DD}=2.4 – 5.5V		$6/f_{OSC}$			s
Edge Detection Rise Time Fall Time	t_{EDR} t_{EDF}	V_{DD}=2.4 – 5.5V PD1 terminal				200	ns
Restart Signal Rise Time	t_{STR}	V_{DD}=2.4 – 5.5V PD0 terminal				200	ns

■ AC CHARACTERISTICS TIMING CHART

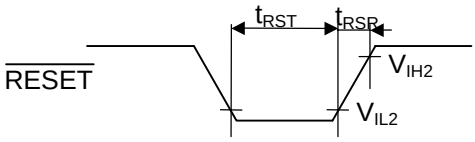
EXTERNAL CLOCK



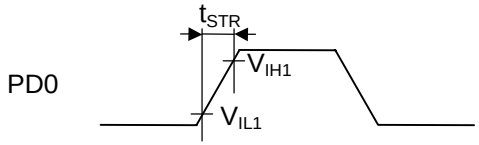
EDGE DETECTOR INPUT



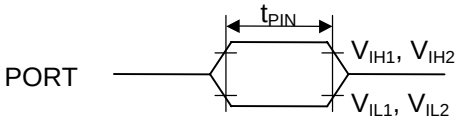
RESET INPUT



RESTART SIGNAL INPUT



PORT INPUT



■ MASK OPTION

The **NJU3101** can set or select the following options by the mask option as same as the mask of the program coding in ROM.

(1) INPUT OUTPUT Terminal Selection

All of input-output terminals select a terminal type from the following table for each group as a PORT by the mask option.

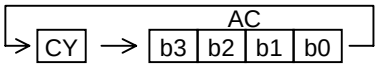
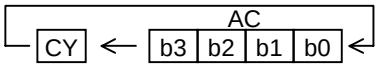
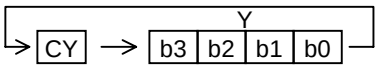
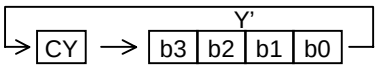
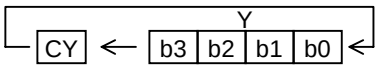
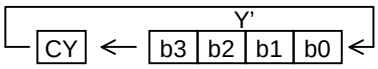
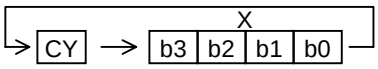
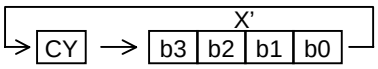
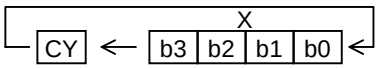
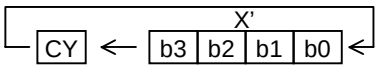
	INPUT TYPE	SYMBOL	OUTPUT TYPE	SYMBOL
PA0 – PA3	C-MOS input with Pull-up	IA	C-MOS output	OB
PD0, PD1	C-MOS input	IC		
PB0, PC0	C-MOS input with Pull-up	IA	N-channel OPEN DRAIN output with Pull-up	OA
	C-MOS input	IC	N-channel OPEN DRAIN output	OC
PE0, PE1	C-MOS SCHMITT TRIGGER input with Pull-up	IB	C-MOS output	OB
	C-MOS SCHMITT TRIGGER input	ID		

(2) Edge Detector Selection

When the PORTD(PHY4) is set as the input, PD1 terminal operates as Edge Detector terminal. The result of edge detection is set into bit2(b2) of PORTD(PHY4). The polarity of the edge, rising as "low to high" or falling as "high to low", is selected by the mask option.

■ MNEMONIC LIST

	Mnemonic	Operation code	Function	Status	Cycle	Memo
DATA TRANSFERENCE	TAY	04	Y←AC	1	1	RPC=0
			Y'←AC	1	1	RPC=1
	TYA	14	AC←Y	1	1	RPC=0
			AC←Y'	1	1	RPC=1
	XAX	1B	AC↔X	1	1	RPC=0
			AC↔X'	1	1	RPC=1
	TAP	26	PH(Y')←AC	1	1	
	TPA	16	AC←PH(Y')	1	1	
	TAPICY	17	PH(Y')←AC, Y←Y+1	*	1	
	TAPDCY	27	PH(Y')←AC, Y←Y-1	*	1	
	TMA	0D	AC←M(X,Y)	1	1	
	TAM	1D	M(X,Y)←AC	1	1	
	TAMICY	0A	M(X,Y)←AC, Y←Y+1	*	1	
	TAMDCY	1A	M(X,Y)←AC, Y←Y-1	*	1	
	TMY	05	Y←M(X,Y)	1	1	RPC=0
			Y'←M(X,Y)	1	1	RPC=1
	XMA	0B	AC↔M(X,Y)	1	1	
	TPMICY	03	M(X,Y)←PH(Y'), Y←Y+1	*	1	
	TMPICY	13	PH(Y')←M(X,Y), Y←Y+1	*	1	
	TRM	23	M(X,Y)←ROM(PHY13,X',AC)	1	2	Y = an even number : ROM of 4bit low-data
						Y = an odd number : ROM of 4bit hi-data
	CLA	80	AC←0	1	1	
	LDI A,#K	80–8F	AC←#K	1	1	#K=0–15
	LDI Y,#K	90–9F	Y←#K	1	1	RPC=0, #K=0–15
			Y'←#K	1	1	RPC=1, #K=0–15
	LDI X,#K	A0–AF	X←#K	1	1	RPC=0, #K=0–15
			X'←#K	1	1	RPC=1, #K=0–15
CALCULATING	ADD A,M	0E	AC←AC+M(X,Y)	*	1	
	INC A	71	AC←AC+1	*	1	
	DEC A	7F	AC←AC-1	*	1	
	ADD A,#K	70–7F	AC←AC+#K	*	1	#K=0–15
	AND A,M	0F	AC←AC∧M(X,Y)	*	1	
	CMP A,M	2E	AC< >M(X,Y)	*	1	
	CMP Y,#K	B0–BF	Y< >#K	*	1	#K=0–15
	INC Y	08	Y←Y+1	*	1	RPC=0
			Y'←Y'+1	*	1	RPC=1
	DEC Y	18	Y←Y-1	*	1	RPC=0
			Y'←Y'-1	*	1	RPC=1
	INC M	09	AC←M(X,Y)+1	*	1	
	DEC M	19	AC←M(X,Y)-1	*	1	
	YNEA	01	Y< >AC	*	1	
	OR A,M	1F	AC←AC∨M(X,Y)	*	1	
	XOR A,M	2F	AC←AC⊕M(X,Y)	*	1	
	NEG	2D	AC←0-AC	1	1	
	SUB A,M	1E	AC←M(X,Y)-AC	*	1	
	AND A,#K	40–4F	AC←AC∧#K	*	1	#K=0–15
	OR A,#K	50–5F	AC←AC∨#K	*	1	#K=0–15

	Mnemonic	Operation code	Function	Status	Cycle	Memo
BRANCH	JPL addr	68–6F	ST=1:PC←addr, ST=0:No branch	1	2	2byte Mnemonic
	JMP addr	C0–FF	ST=1:PC←addr, ST=0:No branch	1	1	
	CALL addr	60–67	ST=1:(SP)←PC+2, SP←SP+1, PC←addr ST=0:No branch	1	2	2byte Mnemonic
	RET	2B	PC←(SP), SP←SP-1	1	1	
BIT OPERATION	SBIT b	30–33	M(X,Y)b←1	1	1	B=0–3
	RBIT b	34–37	M(X,Y)b←0	1	1	B=0–3
	TBIT b	38–3B	ST←M(X,Y)b	*	1	B=0–3
	TBA b	3C–3F	ST←(AC)b	*	1	B=0–3
	RAR	21		*	1	
	RAL	22		*	1	
	RYR	24		*	1	RPC=0
				*	1	RPC=1
	RYL	25		*	1	RPC=0
				*	1	RPC=1
	RXR	28		*	1	RPC=0
				*	1	RPC=1
	RXL	29		*	1	RPC=0
				*	1	RPC=1
	SEC	0C	CY←1	1	1	
	CLC	1C	CY←0	0	1	
	SRPC	10	RPC←1	1	1	
	RRPC	20	RPC←0	1	1	
SPECIAL	NOP	00	No Operation	1	1	
	HLT	07	CPU Halted	1	1	
	MDT	06	Memory Dump Test	–	–	

Note)

←	:Transfer direction	AC	:Accumulator	SP	:Stack pointer
∧	:AND	X	:Xregister	RPC	:RPC flag
∨	:OR	X'	:X'register	CY	:Carry flag
⊕	:Exclusive OR	Y	:Yregister	ST	:Status flag
+	:Add	Y'	:Y'register	#K	:Immediate data
-	:Subtraction	PH	:Peripheral register	addr	:Blanch address
< >	:Comparison	M	:Data memory	( )	:A content of register or memory pointed by the address indicated in ( ).
		ROM	:Program memory		
		PC	:Program counter	b	:Bit position

Status description)

0:After the command execution, ST-flag is always set to "0".

1:After the command execution, ST-flag is always set to "1".

*:Status

[CAUTION]
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