

## TDMA ANTENNA SWITCH GaAs MMIC

### ■GENERAL DESCRIPTION

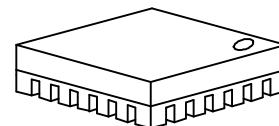
NJG1520PE1 is an antenna switch IC for a digital cellular phone of 800MHz and 1.5GHz band.

The parallel control signals of three bits connect T/R circuits to internal two antennas or external two antennas.

The termination ports with external matching circuits make low interference between diversity antennas.

The Ultra small & thin FFP24-E1 package is applied.

### ■PACKAGE OUTLINE



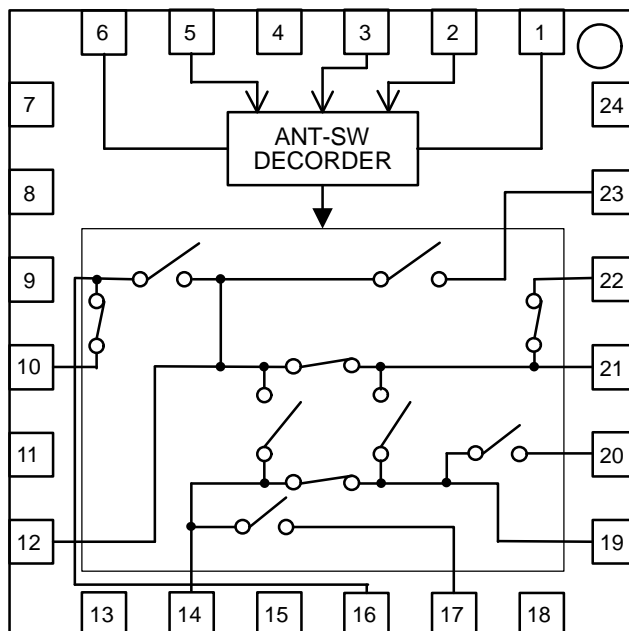
NJG1520PE1

### ■FEATURES

- Low voltage operation -2.5V (TX only) and +3.5V
- Low current consumption 10uA typ. (TX Mode,  $P_{in}=30\text{dBm}$ ), 2uA typ. (RX Mode, No RF Signal)
- Low insertion loss 0.45dB typ. @ (TX-ANT1, TX-EXT1)  $f_{in}=940\text{MHz}$ ,  $P_{in}=30\text{dBm}$   
0.55dB typ. @ (TX-ANT1, TX-EXT1)  $f_{in}=1453\text{MHz}$ ,  $P_{in}=30\text{dBm}$
- Low Adjacent Channel Leakage Power -63dBc typ. @  $V_{DD}=+3.5\text{V}$ ,  $V_{SS}=-2.5\text{V}$ ,  $f_{in}=940\text{MHz}$ ,  $P_{in}=30\text{dBm}$   
-64dBc typ. @  $V_{DD}=+3.5\text{V}$ ,  $V_{SS}=-2.5\text{V}$ ,  $f_{in}=1453\text{MHz}$ ,  $P_{in}=30\text{dBm}$
- Ultra small & thin package FFP24-E1 (Mount Size: 3.5x3.5x0.85mm)

### ■PIN CONFIGURATION

FFP24 Type  
(Top View)



Pin Connection

1. Vss	13. GND
2. CTL3	14. ANT1
3. CTL2	15. GND
4. GND	16. ANT2
5. CTL1	17. TER2
6. VDD	18. GND
7. GND	19. TX
8. GND	20. GND
9. GND	21. EXT1
10. TER1	22. GND
11. GND	23. EXT2
12. RX	24. GND

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## ■ABSOLUTE MAXIMUM RATINGS

(T<sub>a</sub>=+25°C)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
Supply Voltage 1	V <sub>DD</sub>	V <sub>DD</sub> Terminal	6.0	V
Supply Voltage 2	V <sub>SS</sub>	V <sub>SS</sub> Terminal	-4.0~+0.3	V
Control Voltage	V <sub>CTL</sub>	CTL1, CTL2, CTL3 Terminals	6.0	V
Input Power	P <sub>in</sub>	TX, ANT1, EXT1 Terminals V <sub>DD</sub> =3.5V, V <sub>SS</sub> =-2.5V	37	dBm
		RX, ANT2, EXT2 Terminals V <sub>DD</sub> =3.5V, V <sub>SS</sub> =0.0V	28	dBm
Power Dissipation	P <sub>D</sub>		600	mW
Operating Temperature	T <sub>opr</sub>		-40~+85	°C
Storage Temperature	T <sub>stg</sub>		-55~+125	°C

## ■ELECTRICAL CHARACTERISTICS 1 [DC CHARACTERISTICS]

General Conditions: T<sub>a</sub>=+25°C, V<sub>DD</sub>=3.5V, V<sub>SS</sub>=-2.5V

TX, RX, ANT1, ANT2, EXT1, EXT2: terminated (50Ω)

TER1: grounded by 5pF capacitor, TER2: grounded by 10pF capacitor

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Voltage	V <sub>DD</sub>	V <sub>DD</sub> Terminal	2.7	3.5	5.0	V
Negative Supply Voltage	V <sub>SS</sub>	V <sub>SS</sub> Terminal	-3.5	-2.5	-2.0	V
Current Consumption 1	I <sub>DD1</sub>	V <sub>DD</sub> Terminal RX Mode, No RF Signal	-	2.0	5.0	μA
Current Consumption 2	I <sub>SS1</sub>	V <sub>SS</sub> Terminal RX Mode, No RF Signal	-0.1	-	0	uA
Current Consumption 3	I <sub>DD2</sub>	V <sub>DD</sub> Terminal, f <sub>in</sub> =0.1~2GHz TX Mode, P <sub>in</sub> =30dBm	-	10	30	uA
Current Consumption 4	I <sub>SS2</sub>	V <sub>SS</sub> Terminal, f <sub>in</sub> =0.1~2GHz TX Mode, P <sub>in</sub> =30dBm	-30	-10	-	uA
Control Voltage (H)	V <sub>CTL(H)</sub>	CTL1, CTL2, CTL3 Terminals	2.0	3.0	V <sub>DD</sub>	V
Control Voltage (L)	V <sub>CTL(L)</sub>	CTL1, CTL2, CTL3 Terminals	0	0	0.6	V
Control Current	I <sub>CTL</sub>	CTL1, CTL2, CTL3=V <sub>DD</sub> or CTL1, CTL2, CTL3=0V	-1.3	-	1.3	uA
Control terminal Input Impedance	R <sub>in</sub>	CTL1, CTL2, CTL3 Terminals	4	-	-	MΩ

## ■ ELECTRICAL CHARACTERISTICS 2 [800MHz TX Mode]

General Conditions:  $T_a=+25^{\circ}\text{C}$ ,  $V_{DD}=3.5\text{V}$ ,  $V_{SS}=-2.5\text{V}$ ,  $f_{in}=940\text{MHz}$

Tested on PCB circuit as shown below.

Insertion loss of each connectors, striplines, and capacitors are excluded.

TX, RX, ANT1, ANT2, EXT1, EXT2: terminated ( $50\Omega$ )

TER1: grounded by 5pF capacitor, TER2: grounded by 10pF capacitor.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Frequency range 1	$f_{in1}$		885	-	960	MHz
TX-ANT1 Insertion Loss	LOSS1	$P_{in}=30\text{dBm}$	-	0.45	0.60	dB
TX-EXT1 Insertion Loss	LOSS2	$P_{in}=30\text{dBm}$	-	0.50	0.65	dB
TX-RX Isolation	ISL1	$P_{in}=30\text{dBm}$ TX-ANT1, TX-EXT1 passing	24	29	-	dB
TX-ANT1 Isolation	ISL2	$P_{in}=30\text{dBm}$ TX-EXT1 passing	22	27	-	dB
TX-ANT2 Isolation	ISL3	$P_{in}=30\text{dBm}$ TX-ANT1, TX-EXT1 passing	20	25	-	dB
TX-EXT1 Isolation	ISL4	$P_{in}=30\text{dBm}$ TX-ANT1 passing	20	25	-	dB
TX-EXT2 Isolation	ISL5	$P_{in}=30\text{dBm}$ TX-ANT1, TX-EXT1 passing	32	37	-	dB
Input Power at 0.5dB Compression 1	$P_{-0.5}(1)$	TX-ANT1, TX-EXT1 passing	33.5	35.5	-	dBm
Adjacent Channel Leakage Power 1	ACP1	PDC Standard, $\pm 50\text{kHz}$ offset $P_{in}=30\text{dBm}$ Input Signal ACP=-64dBc @ 30dBm	-	-63	-60	dBc
Adjacent Channel Leakage Power 2	ACP2	PDC Standard, $\pm 100\text{kHz}$ offset $P_{in}=30\text{dBm}$ Input Signal ACP=-76dBc @ 30dBm	-	-74	-70	dBc
2nd Harmonics 1	$2f_0(1)$	$P_{in}=30\text{dBm}$ Input Signal 2nd Harmonics=-70dBc	-	-65	-63	dBc
3rd Harmonics 1	$3f_0(1)$	$P_{in}=30\text{dBm}$ Input Signal 3rd Harmonics=-100dBc	-	-64	-62	dBc
VSWR 1	VSWR1	TX-ANT1, TX-EXT1 passing	-	1.2	1.5	
Switching Time 1	$T_D1$	CTL1~3	-	120	500	nsec

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## ■ELECTRICAL CHARACTERISTICS 3 [800MHz RX Mode]

General Conditions:  $T_a=+25^{\circ}\text{C}$ ,  $V_{DD}=3.5\text{V}$ ,  $V_{SS}=0\text{V}$ ,  $f_{in}=885\text{MHz}$

Tested on PCB circuit as shown below.

Insertion loss of each connectors, striplines, and capacitors are excluded.

TX, RX, ANT1, ANT2, EXT1, EXT2: terminated ( $50\Omega$ )

TER1: grounded by 5pF capacitor, TER2: grounded by 10pF capacitor.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Frequency range 2	$f_{in2}$		810	-	885	MHz
RX-ANT1 Insertion Loss	LOSS3	$P_{in}=10\text{dBm}$	-	0.55	0.70	dB
RX-ANT2 Insertion Loss	LOSS4	$P_{in}=10\text{dBm}$	-	0.45	0.60	dB
RX-EXT1 Insertion Loss	LOSS5	$P_{in}=10\text{dBm}$	-	0.80	0.95	dB
RX-EXT2 Insertion Loss	LOSS6	$P_{in}=10\text{dBm}$	-	0.80	0.95	dB
RX-ANT1 Isolation	ISL6	$P_{in}=10\text{dBm}$ RX-ANT2, RX-EXT1, RX-EXT2 passing	21	24	-	dB
RX-ANT2 Isolation	ISL7	$P_{in}=10\text{dBm}$ RX-ANT1, RX-EXT1, RX-EXT2 passing	22	25	-	dB
RX-EXT1 Isolation	ISL8	$P_{in}=10\text{dBm}$ RX-ANT1, RX-ANT2, RX-EXT2 passing	22	25	-	dB
RX-EXT2 Isolation	ISL9	$P_{in}=10\text{dBm}$ RX-ANT1, RX-ANT2, RX-EXT1 passing	20	23	-	dB
Input Power at 1dB Compression 1	$P_{-1}(1)$	RX-ANT1, RX-ANT2, RX-EXT1, RX-EXT2 passing	20	26	-	dBm
VSWR 2	VSWR2	RX-ANT1, RX-ANT2, RX-EXT1, RX-EXT2 passing	-	1.2	1.6	
Switching Time 2	$T_{D2}$	CTL1~3	-	120	500	nsec

## ■ ELECTRICAL CHARACTERISTICS 4 [1.5GHz TX Mode]

General Conditions:  $T_a=+25^{\circ}\text{C}$ ,  $V_{DD}=3.5\text{V}$ ,  $V_{SS}=-2.5\text{V}$ ,  $f_{in}=1453\text{MHz}$

Tested on PCB circuit as shown below.

Insertion loss of each connectors, striplines, and capacitors are excluded.

TX, RX, ANT1, ANT2, EXT1, EXT2: terminated ( $50\Omega$ )

TER1: grounded by 5pF capacitor, TER2: grounded by 10pF capacitor.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Frequency range 3	$f_{in3}$		1429	-	1453	MHz
TX-ANT1 Insertion Loss	LOSS7	$P_{in}=30\text{dBm}$	-	0.55	0.70	dB
TX-EXT1 Insertion Loss	LOSS8	$P_{in}=30\text{dBm}$	-	0.65	0.80	dB
TX-RX Isolation	ISL10	$P_{in}=30\text{dBm}$ TX-ANT1, TX-EXT1 passing	28	33	-	dB
TX-ANT1 Isolation	ISL11	$P_{in}=30\text{dBm}$ TX-EXT1 passing	25	30	-	dB
TX-ANT2 Isolation	ISL12	$P_{in}=30\text{dBm}$ TX-ANT1, TX-EXT1 passing	20	24	-	dB
TX-EXT1 Isolation	ISL13	$P_{in}=30\text{dBm}$ TX-ANT1 passing	20	24	-	dB
TX-EXT2 Isolation	ISL14	$P_{in}=30\text{dBm}$ TX-ANT1, TX-EXT1 passing	35	40	-	dB
Input Power at 0.5dB Compression 2	$P_{-0.5(2)}$	TX-ANT1, TX-EXT1 passing	33.5	35.5	-	dBm
Adjacent Channel Leakage Power 3	ACP3	PDC Standard, $\pm 50\text{kHz}$ offset $P_{in}=30\text{dBm}$ Input Signal ACP=-67dBc @ 30dBm	-	-64	-60	dBc
Adjacent Channel Leakage Power 4	ACP4	PDC Standard, $\pm 100\text{kHz}$ offset $P_{in}=30\text{dBm}$ Input Signal ACP=-76dBc @ 30dBm	-	-72	-70	dBc
2nd Harmonics 2	$2f_0(2)$	$P_{in}=30\text{dBm}$ Input Signal 2nd Harmonics =-80dBc	-	-65	-61	dBc
3rd Harmonics 2	$3f_0(2)$	$P_{in}=30\text{dBm}$ Input Signal 3rd Harmonics =-110dBc	-	-63	-61	dBc
VSWR 3	VSWR3	TX-ANT1, TX-EXT1 Passing	-	1.2	1.6	
Switching Time 3	$T_D3$	CTL1~3	-	120	500	nsec

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## ■ELECTRICAL CHARACTERISTICS 5 [1.5GHz RX Mode]

General Conditions:  $T_a=+25^{\circ}\text{C}$ ,  $V_{DD}=3.5\text{V}$ ,  $V_{SS}=0\text{V}$ ,  $f_{in}=1501\text{MHz}$

Tested on PCB circuit as shown below.

Insertion loss of each connectors, striplines, and capacitors are excluded.

TX, RX, ANT1, ANT2, EXT1, EXT2: terminated ( $50\Omega$ )

TER1: grounded by 5pF capacitor, TER2: grounded by 10pF capacitor.

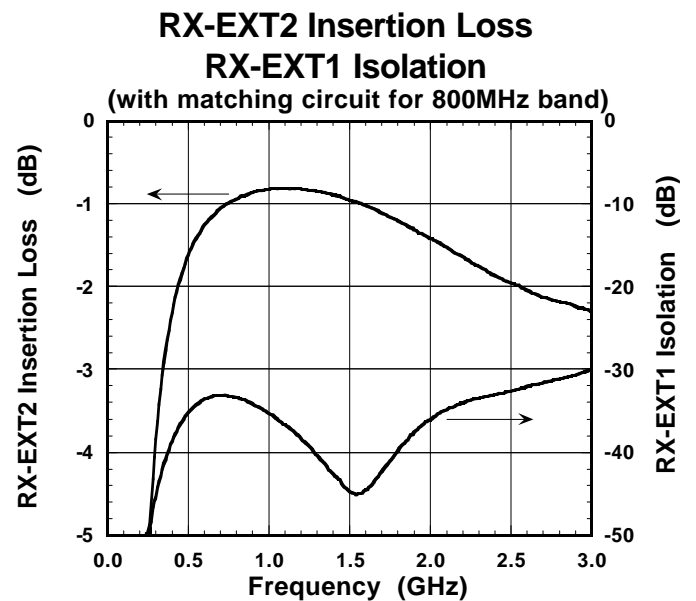
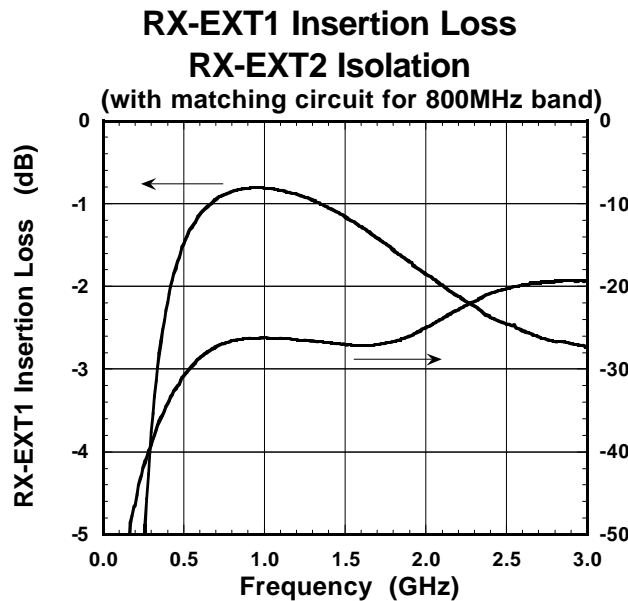
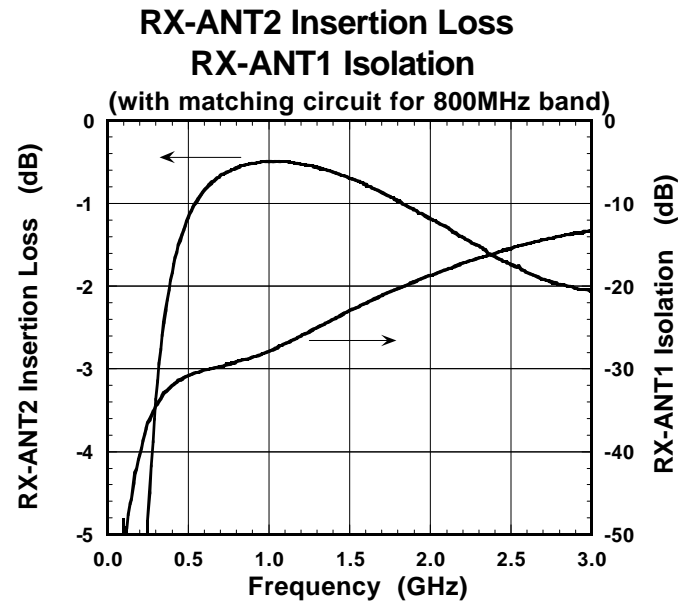
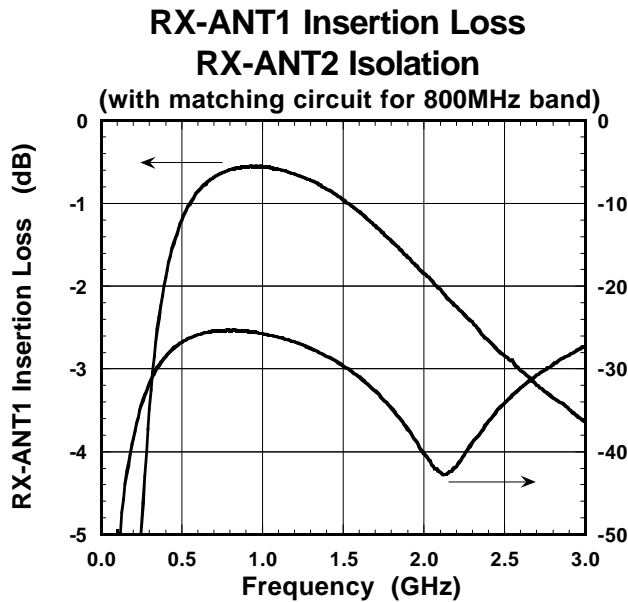
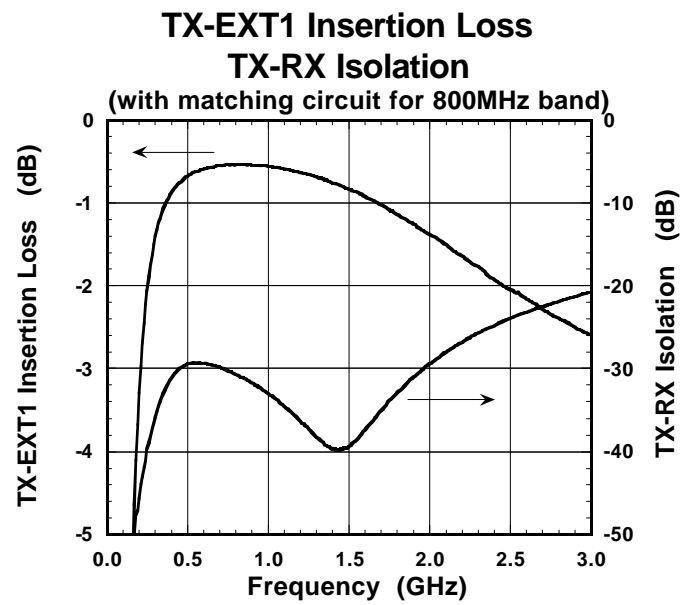
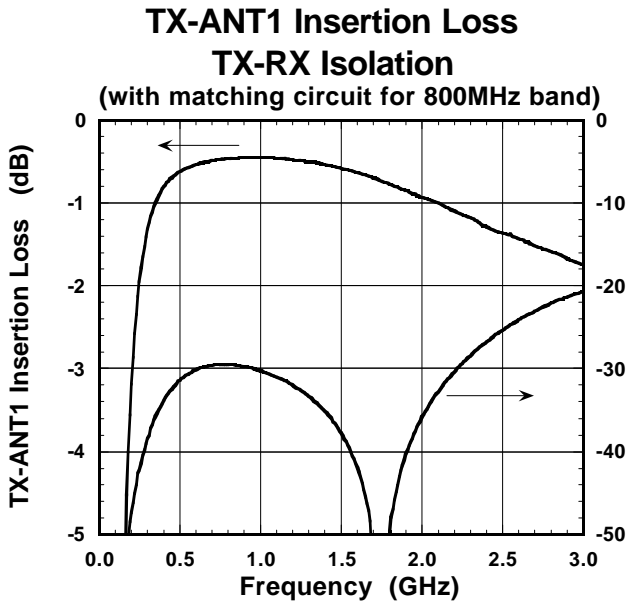
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Frequency range 4	$f_{in4}$		1477	-	1501	MHz
RX-ANT1 Insertion Loss	LOSS9	$P_{in}=10\text{dBm}$	-	0.75	0.85	dB
RX-ANT2 Insertion Loss	LOSS10	$P_{in}=10\text{dBm}$	-	0.65	0.75	dB
RX-EXT1 Insertion Loss	LOSS11	$P_{in}=10\text{dBm}$	-	1.00	1.15	dB
RX-EXT2 Insertion Loss	LOSS12	$P_{in}=10\text{dBm}$	-	0.95	1.10	dB
RX-ANT1 Isolation	ISL15	$P_{in}=10\text{dBm}$ RX-ANT2, RX-EXT1, RX-EXT2 passing	18	22	-	dB
RX-ANT2 Isolation	ISL16	$P_{in}=10\text{dBm}$ RX-ANT1, RX-EXT1, RX-EXT2 passing	20	24	-	dB
RX-EXT1 Isolation	ISL17	$P_{in}=10\text{dBm}$ RX-ANT1, RX-ANT2, RX-EXT2 Passing	23	28	-	dB
RX-EXT2 Isolation	ISL18	$P_{in}=10\text{dBm}$ RX-ANT1, RX-ANT2, RX-EXT1 passing	19	24	-	dB
Input Power at 1dB Compression 2	$P_{-1(2)}$	RX-ANT1, RX-ANT2, RX-EXT1, RX-EXT2 passing	20	26	-	dBm
VSWR 4	VSWR4	RX-ANT1, RX-ANT2, RX-EXT1, RX-EXT2 passing	-	1.2	1.6	
Switching Time 4	$T_D4$	CTL1~3	-	120	500	nsec

## ■ TERMINAL INFORMATION

PIN No.	SYMBOL	DESCRIPTION
1	V <sub>SS</sub>	Negative voltage supply terminal. Please supply negative voltage of -3.5~-2.0V on transmitting state. On receiving state, this terminal is internally disconnected, so the voltage of this terminal(negative, short, or open) does not affect to receiving signal quality. The bypass capacitor should be connected between this terminal and GND for excellent RF performance.
2	CTL3	High-impedance C-MOS input terminal. This terminal is set to High-Level (+2V~V <sub>DD</sub> ) or Low-Level (+0.6V~0V). If the voltage level of this terminal is unstable, please connect a resistor (100KΩ) with GND terminal or V <sub>DD</sub> terminal.
3	CTL2	High-impedance C-MOS input terminal. This terminal is set to High-Level (+2V~V <sub>DD</sub> ) or Low-Level (+0.6V~0V). If the voltage level of this terminal is unstable, please connect a resistor (100KΩ) with GND terminal or V <sub>DD</sub> terminal.
5	CTL1	High-impedance C-MOS input terminal. This terminal is set to High-Level (+2V~V <sub>DD</sub> ) or Low-Level (+0.6V~0V). If the voltage level of this terminal is unstable, please connect a resistor (100KΩ) with GND terminal or V <sub>DD</sub> terminal.
6	V <sub>DD</sub>	Positive voltage supply terminal. The positive voltage (+2.7~+5.0V) have to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
10	TER1	ANT2 termination port. Please connect this port and GND by appropriate capacitor (5pF) to suppress the interference of ANT2 port signal to ANT1 port. The capacitor works as DC voltage (V <sub>DD</sub> ) blocking.
12	RX	RF receiving port. An external capacitor (56pF~100pF) is required to block DC voltage (V <sub>DD</sub> ) .
14	ANT1	RF transmitting/receiving port. An external capacitor (56pF~100pF) is required to block DC voltage (V <sub>DD</sub> ) .
16	ANT2	RF receiving port. An external capacitor (56pF~100pF) is required to block DC voltage (V <sub>DD</sub> ).
17	TER2	ANT2 termination port. Please connect this port and GND by appropriate capacitor (10pF) to suppress the interference of ANT1 port signal to ANT2 port. The capacitor works as DC voltage (V <sub>DD</sub> ) blocking.
19	TX	RF transmitting port. An external capacitor of 56pF~100pF is required to block DC voltage (V <sub>DD</sub> ).
21	EXT1	RF transmitting/receiving port. An external capacitor of 56pF~100pF is required to block DC voltage (V <sub>DD</sub> ).
23	EXT2	RF receiving port. An external capacitor of 56pF~100pF is required to block DC voltage (V <sub>DD</sub> ).
4, 7, 8, 9, 11, 13, 15, 18, 20, 22, 24	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.

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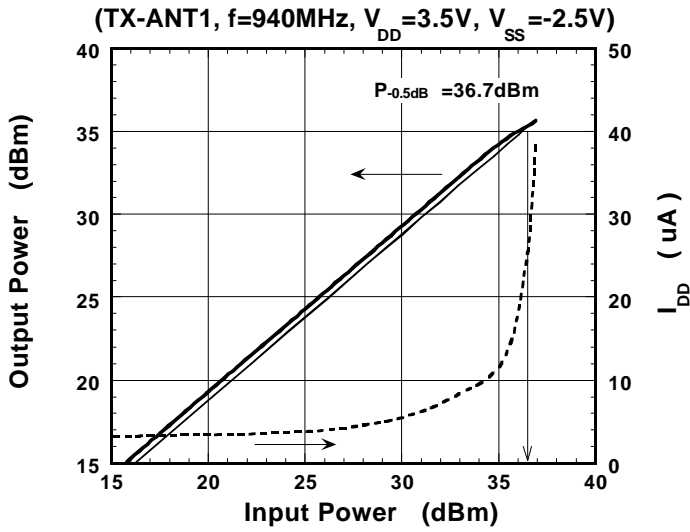
■ TYPICAL CHARACTERISTICS (800MHz Band: Measured on the PCB evaluation circuit)



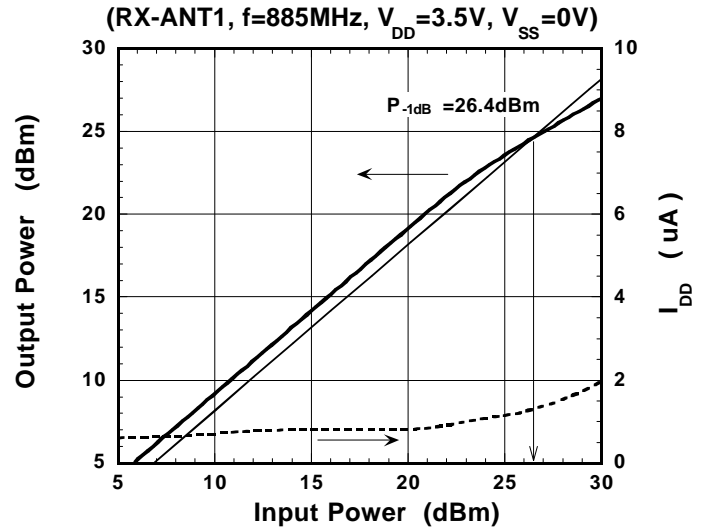


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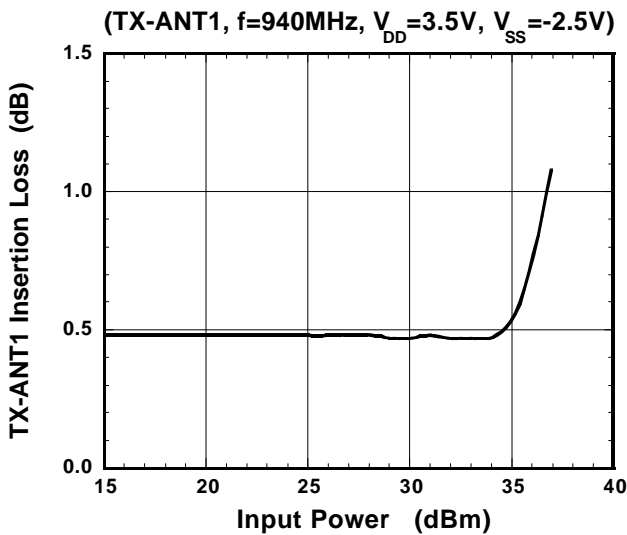
**Output Power,  $I_{DD}$  vs. Input Power**



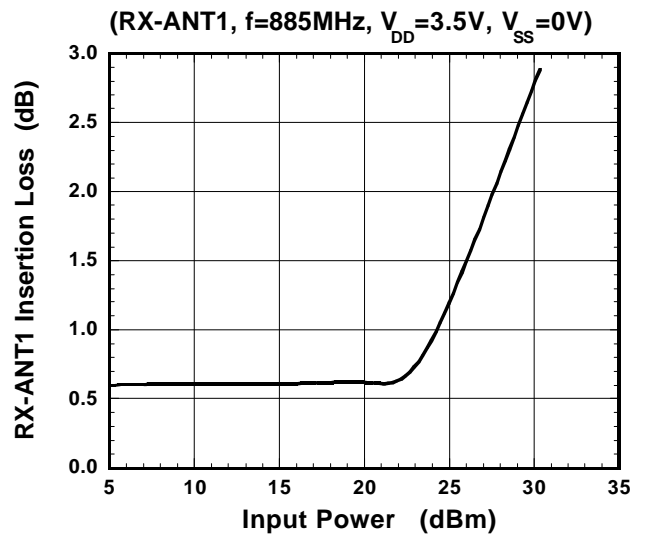
**Output Power,  $I_{DD}$  vs. Input Power**



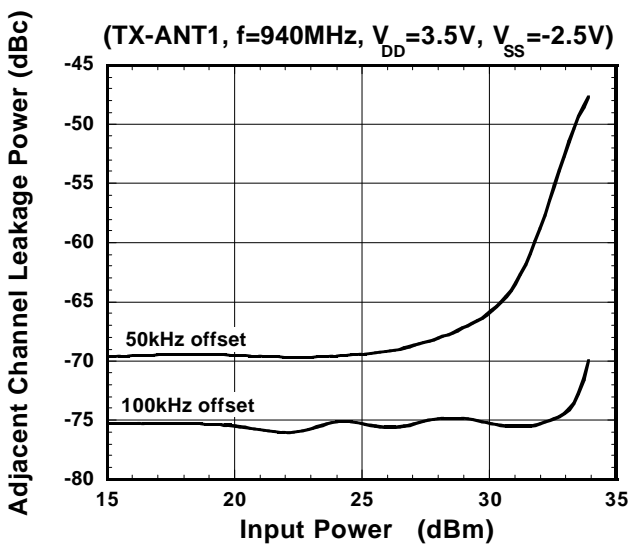
**Insertion Loss vs. Input Power**



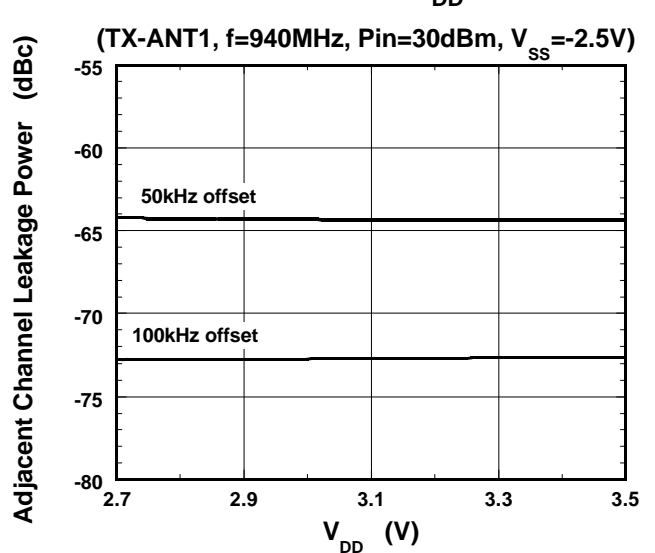
**Insertion Loss vs. Input Power**



**ACP vs. Input Power**



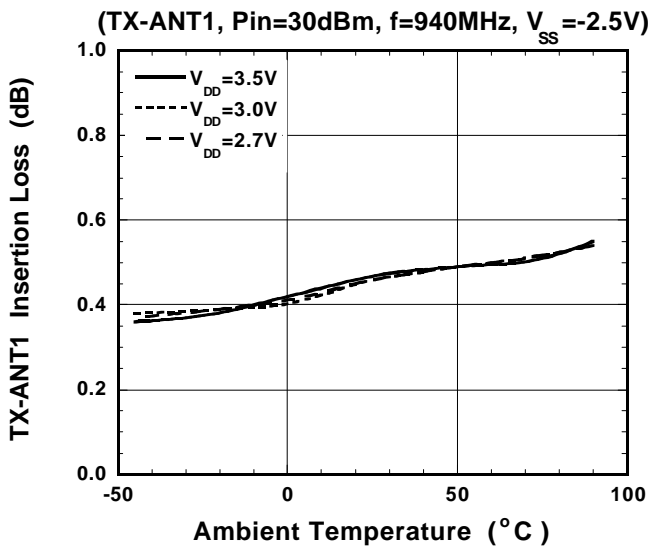
**ACP vs.  $V_{DD}$**



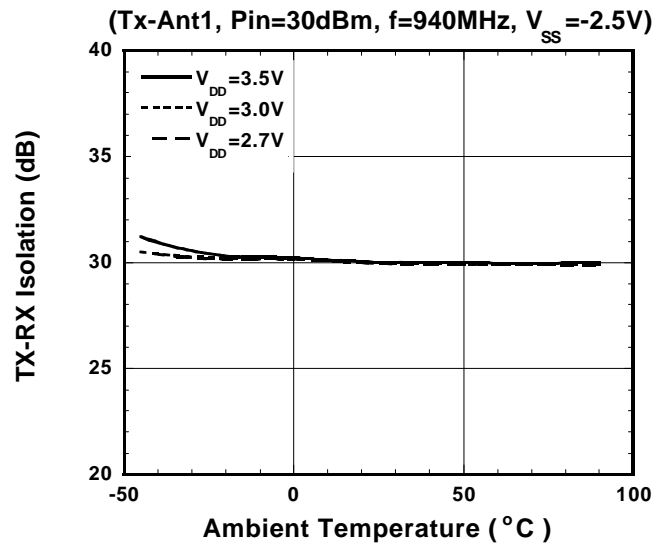
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## ■ TYPICAL CHARACTERISTICS (800MHz Band: Measured on the PCB evaluation circuit)

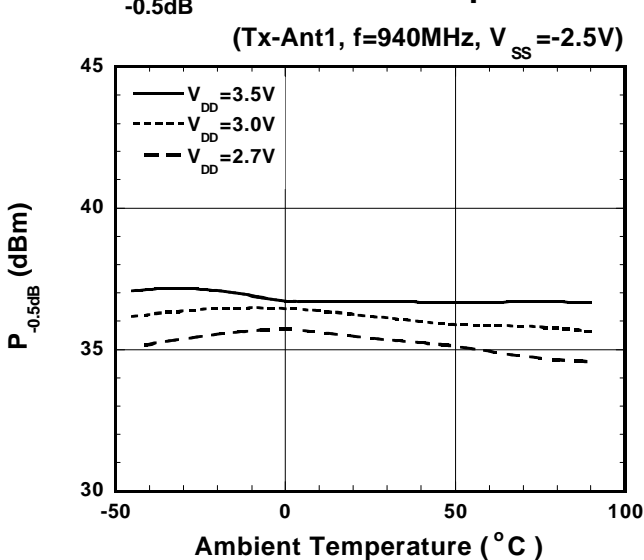
### Loss vs. Ambient Temperature



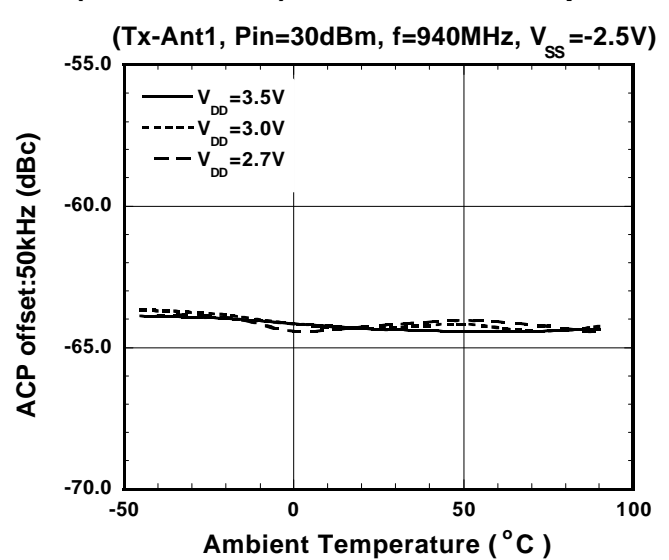
### RX Isolation vs. Ambient Temperature



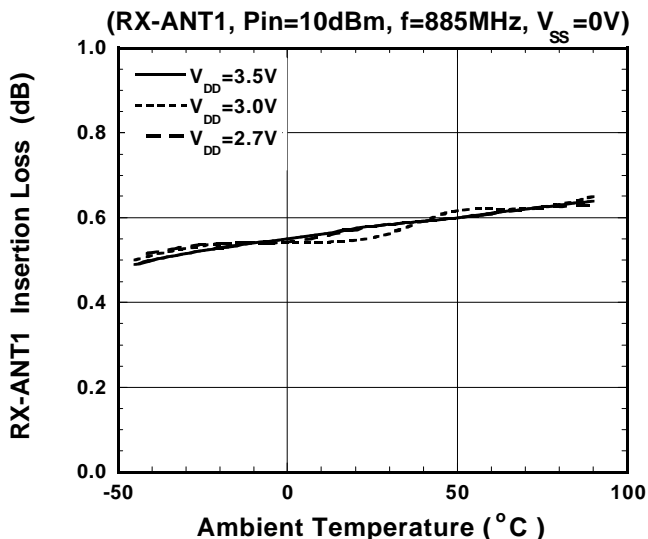
### $P_{-0.5dB}$ vs. Ambient Temperature



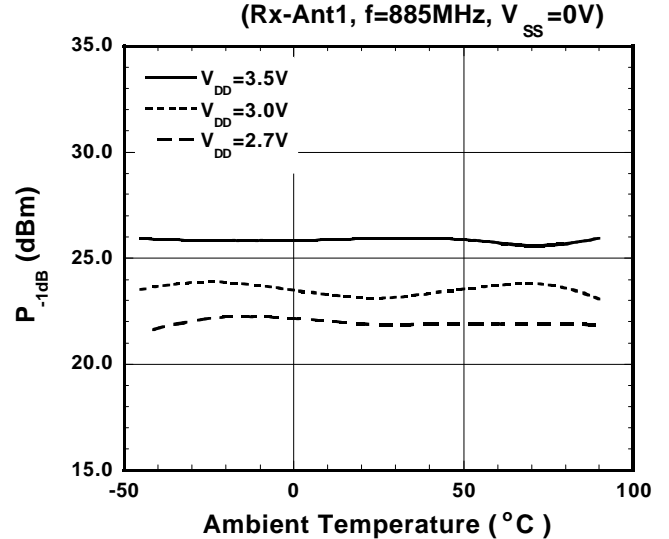
### ACP(offset:50kHz) vs. Ambient Temperature



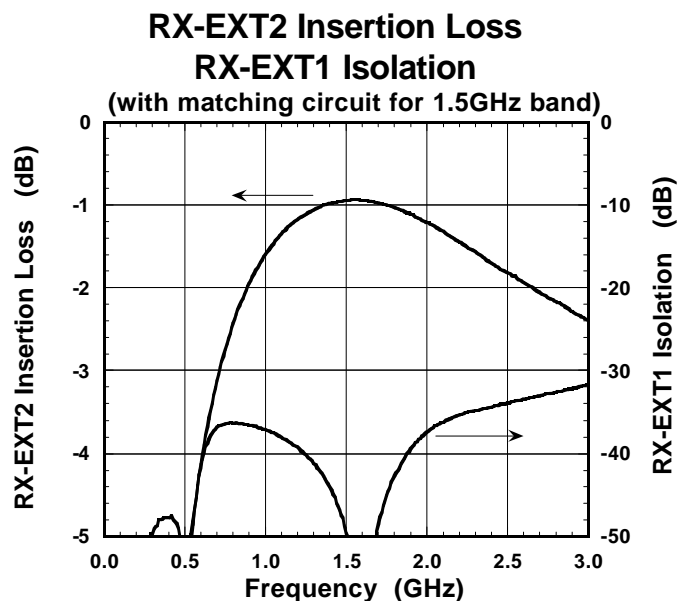
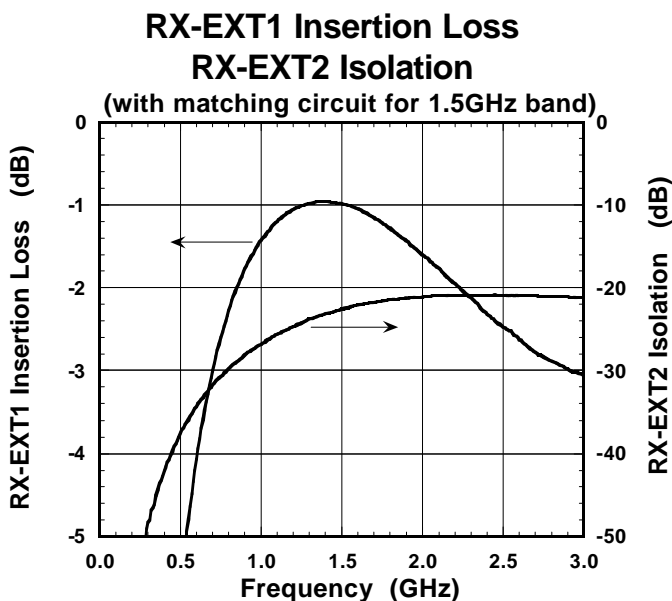
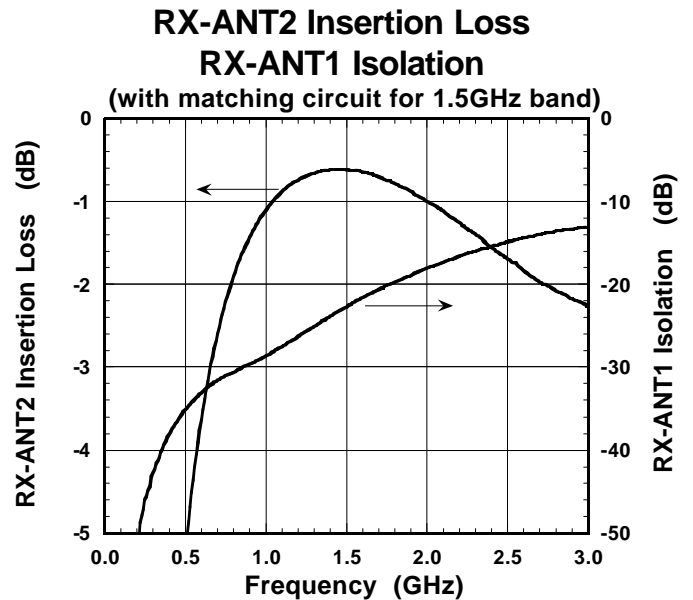
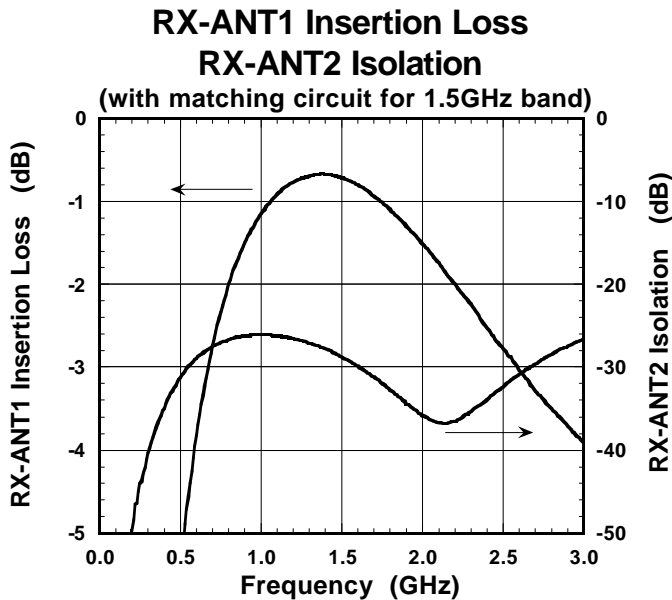
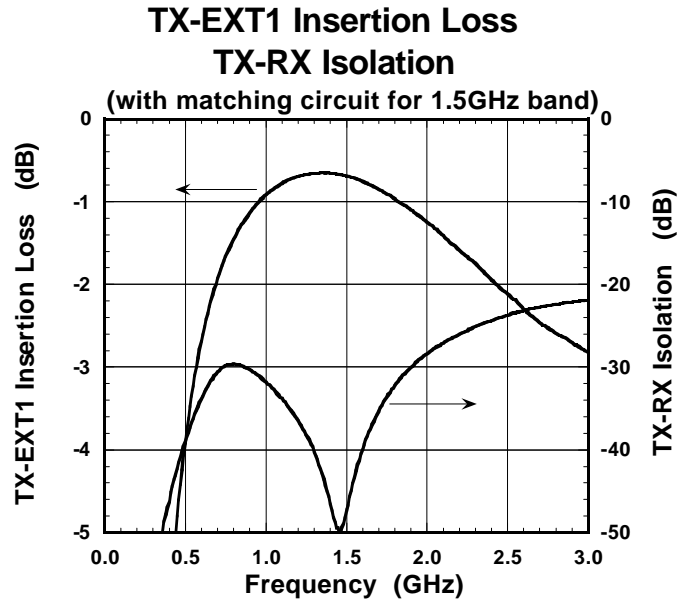
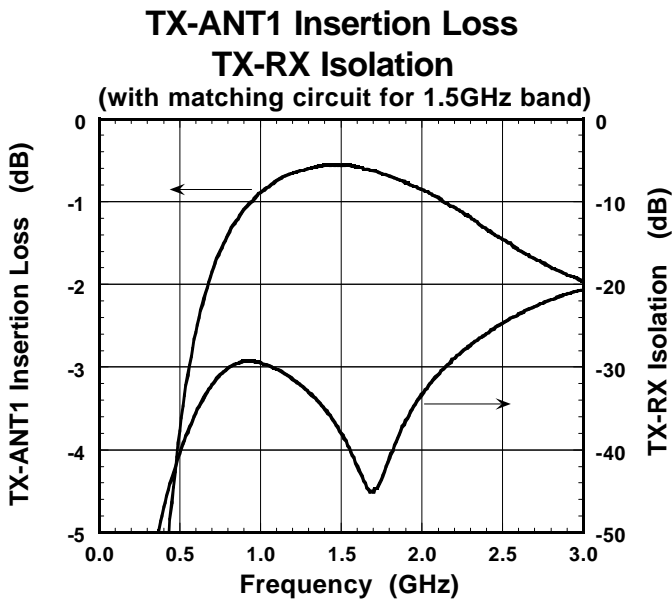
### Loss vs. Ambient Temperature



### $P_{-1dB}$ vs. Ambient Temperature



■ TYPICAL CHARACTERISTICS (1.5GHz Band: Measured on the PCB evaluation circuit)

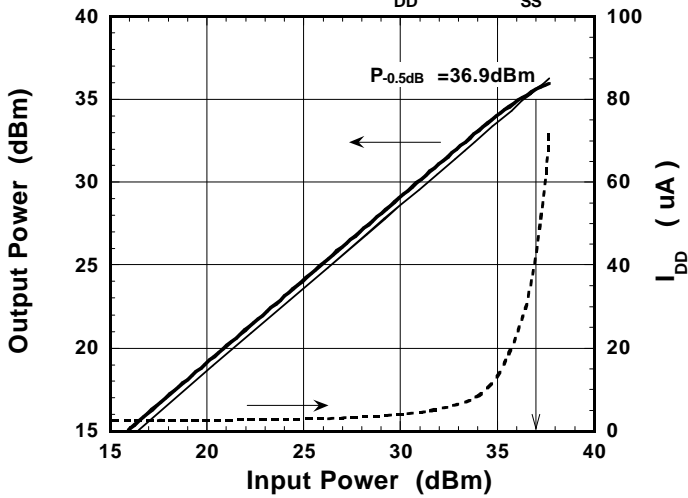


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## ■ TYPICAL CHARACTERISTICS (1.5GHz Band: Measured on the PCB evaluation circuit)

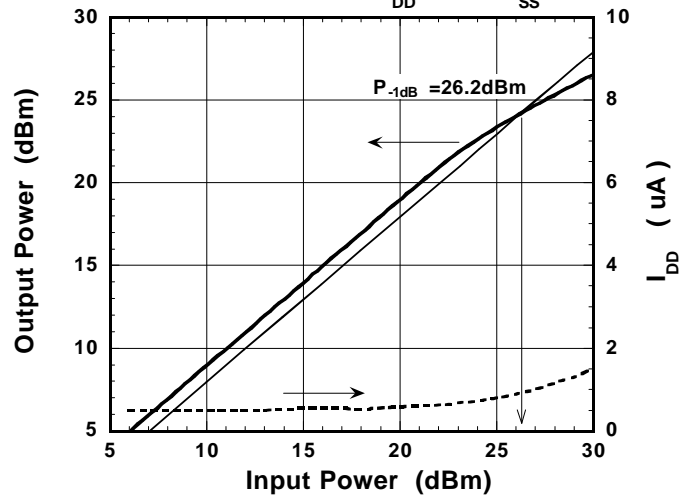
**Output Power,  $I_{DD}$  vs. Input Power**

(TX-ANT1,  $f=1453\text{MHz}$ ,  $V_{DD}=3.5\text{V}$ ,  $V_{SS}=-2.5\text{V}$ )



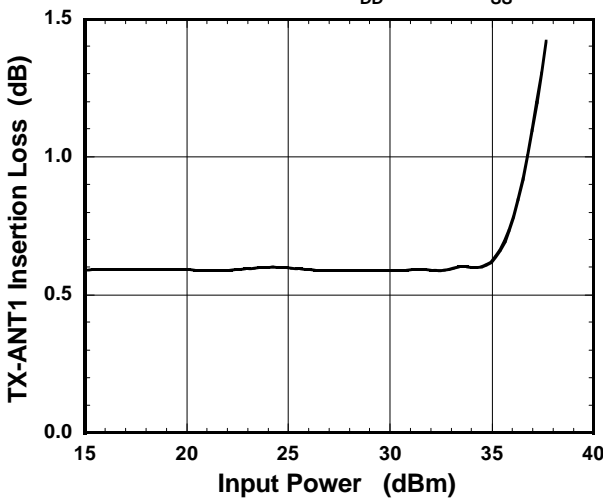
**Output Power,  $I_{DD}$  vs. Input Power**

(RX-ANT1,  $f=1501\text{MHz}$ ,  $V_{DD}=3.5\text{V}$ ,  $V_{SS}=0\text{V}$ )



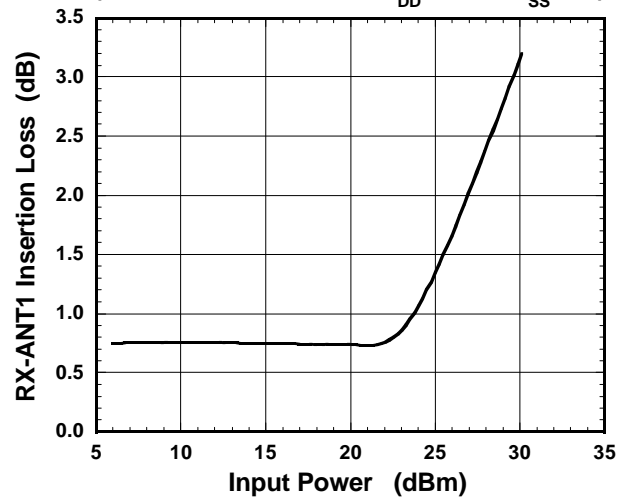
**Insertion Loss vs. Input Power**

(TX-ANT1,  $f=1453\text{MHz}$ ,  $V_{DD}=3.5\text{V}$ ,  $V_{SS}=-2.5\text{V}$ )



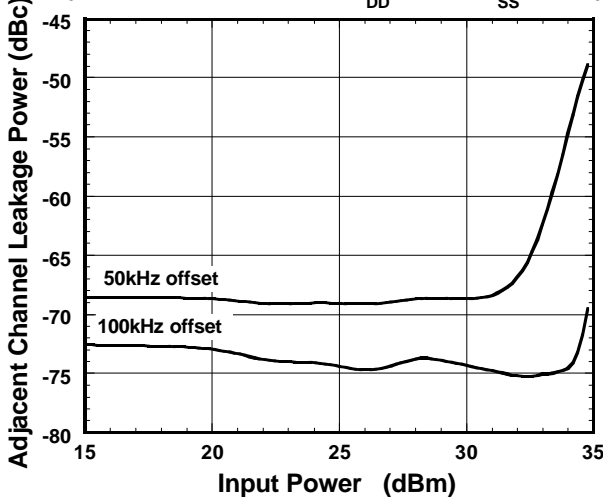
**Insertion Loss vs. Input Power**

(RX-ANT1,  $f=1501\text{MHz}$ ,  $V_{DD}=3.5\text{V}$ ,  $V_{SS}=0\text{V}$ )



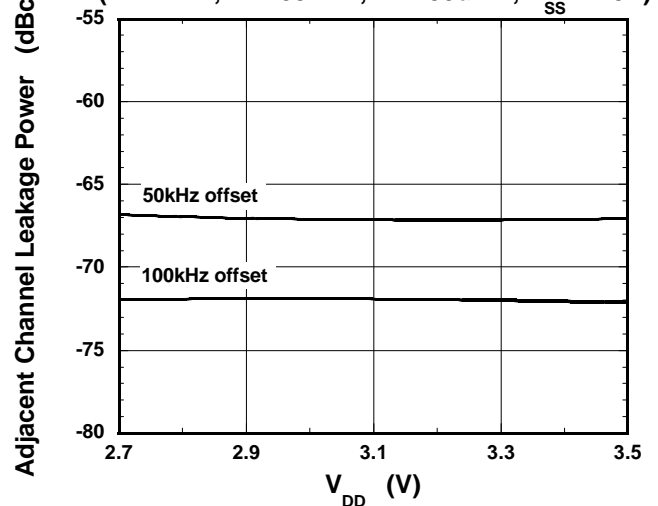
**ACP vs. Input Power**

(TX-ANT1,  $f=1453\text{MHz}$ ,  $V_{DD}=3.5\text{V}$ ,  $V_{SS}=-2.5\text{V}$ )



**ACP vs.  $V_{DD}$**

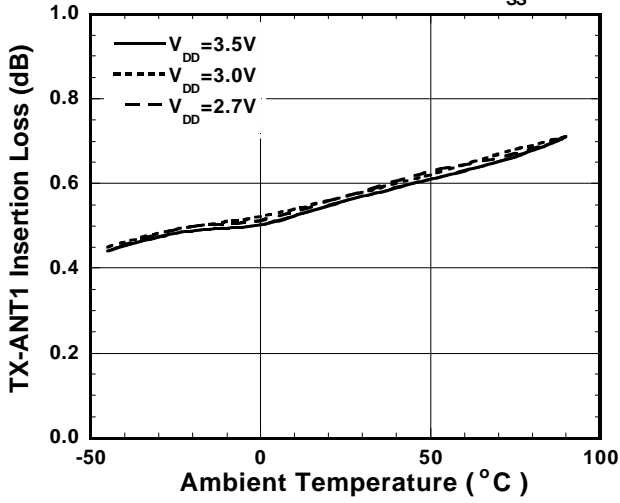
(TX-ANT1,  $f=1453\text{MHz}$ ,  $P_{in}=30\text{dBm}$ ,  $V_{SS}=-2.5\text{V}$ )



■ TYPICAL CHARACTERISTICS (1.5GHz Band: Measured on the PCB evaluation circuit)

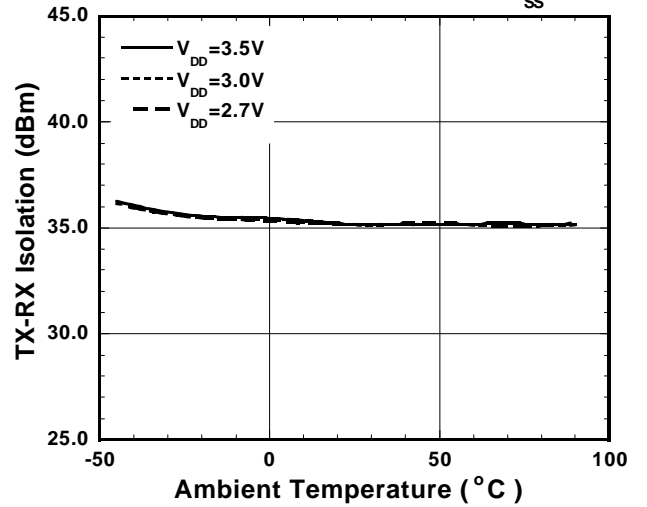
**Loss vs. Ambient Temperature**

(TX-ANT1, Pin=30dBm, f=1453MHz,  $V_{SS}=-2.5V$ )



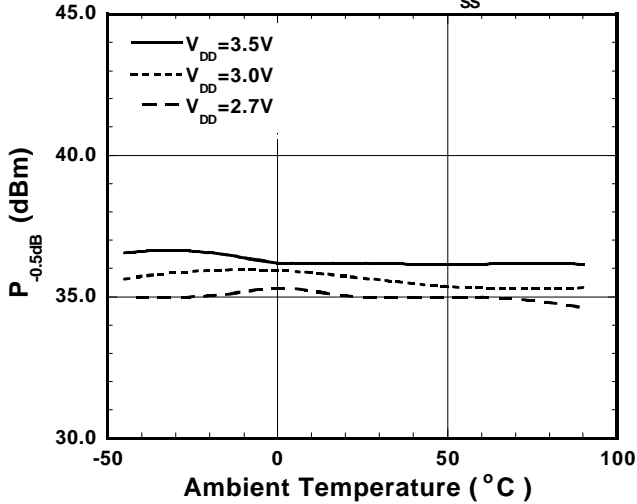
**RX Isolation vs. Ambient Temperature**

(TX-ANT1, Pin=30dBm, f=1453MHz,  $V_{SS}=-2.5V$ )



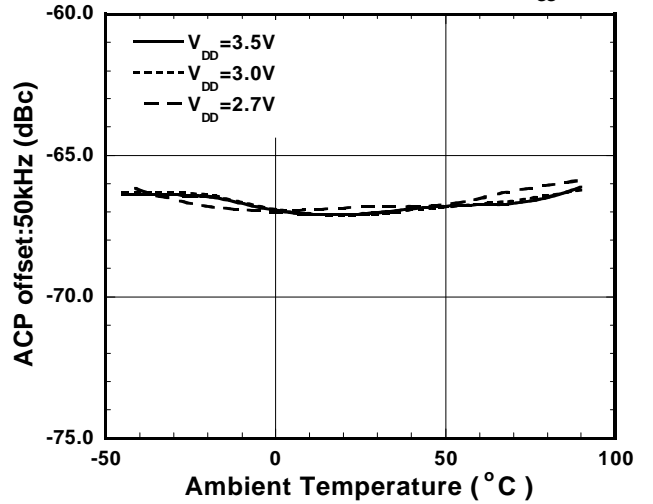
**$P_{-0.5dB}$  vs. Ambient Temperature**

(Tx-Ant1, f=1453MHz,  $V_{SS}=-2.5V$ )



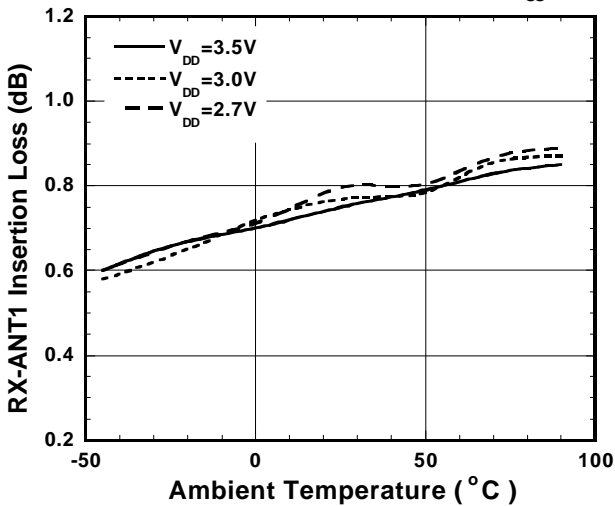
**ACP(offset:50kHz) vs. Ambient Temperature**

(TX-ANT1, Pin=30dBm, f=1453MHz,  $V_{SS}=-2.5V$ )



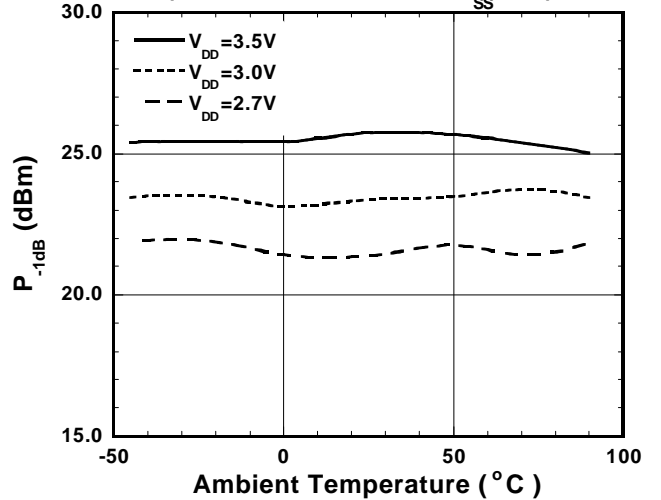
**Loss vs. Ambient Temperature**

(RX-ANT1, Pin=10dBm, f=1501MHz,  $V_{SS}=0V$ )



**$P_{-1dB}$  VS. Ambient Temperature**

(RX-ANT1, f=1501MHz,  $V_{SS}=0V$ )



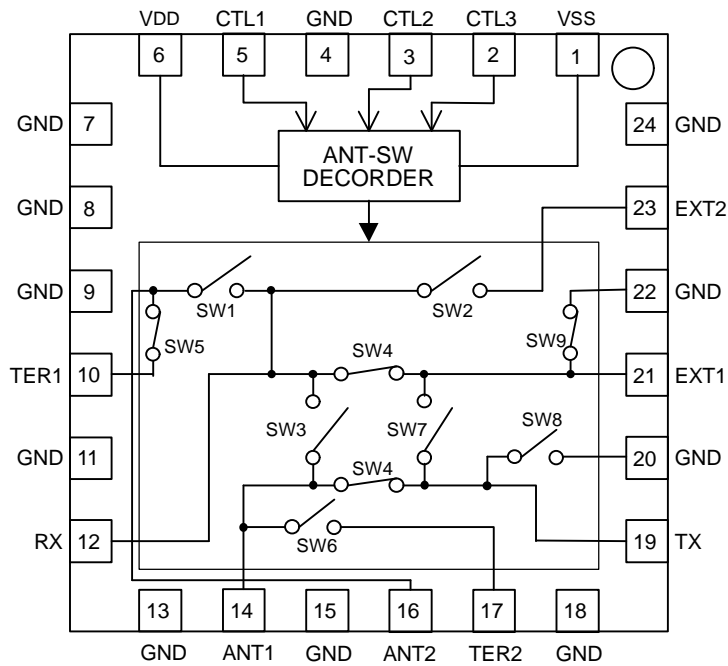
# NJG1520PE1

## TRUTH TABLE

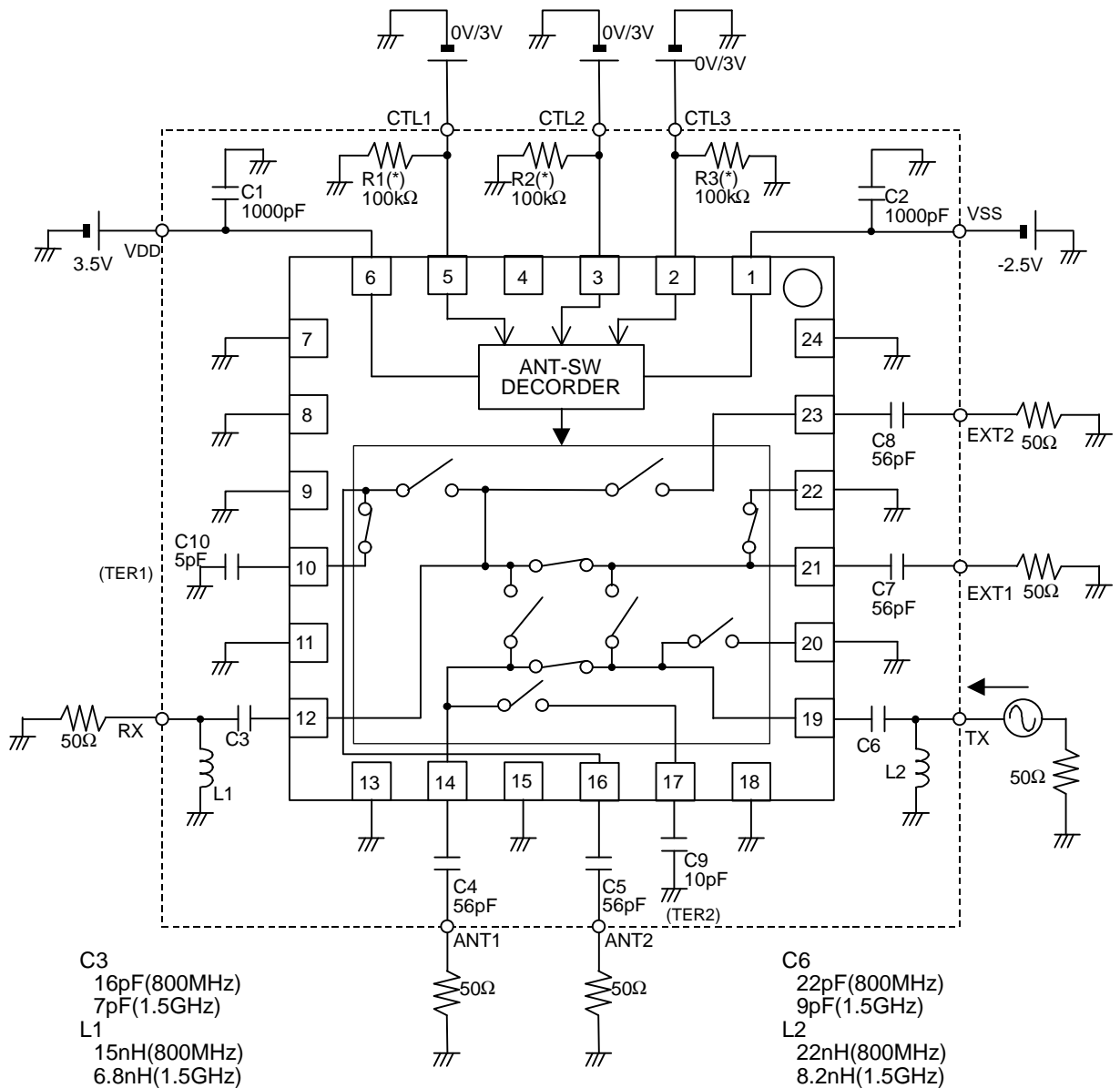
"H"=V<sub>CTL</sub> (H), "L"=V<sub>CTL</sub> (L), "X"=H or L

ROUTE	CONTROL INPUT			CONTROL OUTPUT								
	Tx/Rx	Diversity	IN/OUT	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9
	CTL1	CTL2	CTL3									
TX-ANT1	H	X	H	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON
TX-EXT1	H	X	L	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF
RX-ANT1	L	L	H	OFF	OFF	ON	OFF	ON	OFF	ON	ON	ON
RX-ANT2	L	H	H	ON	OFF	OFF	OFF	OFF	ON	ON	ON	ON
RX-EXT1	L	L	L	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF
RX-EXT2	L	H	L	OFF	ON	OFF	OFF	ON	ON	ON	ON	ON

## PIN CONFIGURATION (TOP VIEW)



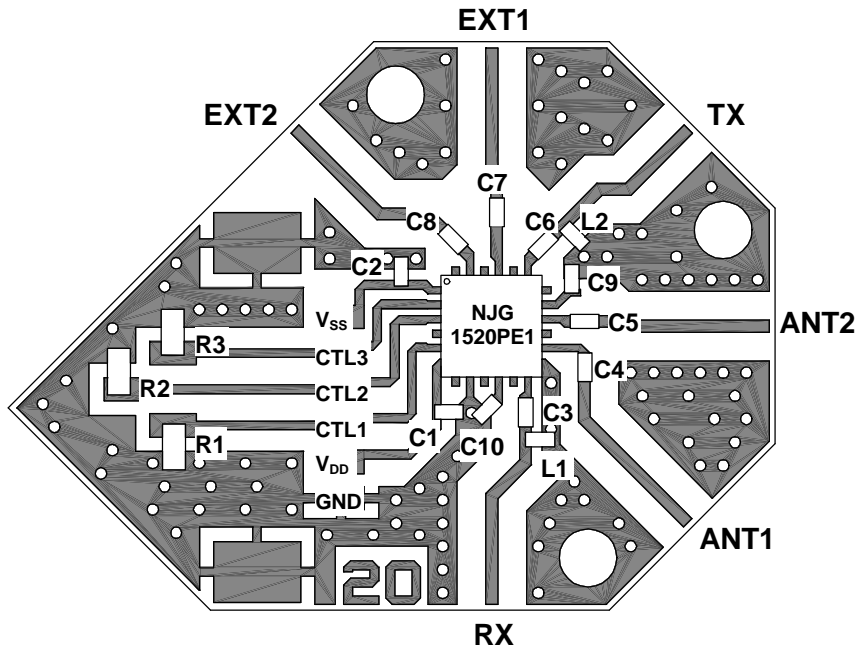
## RECOMMENDED CIRCUIT (TX-ANT1 PASSING)



(\*) If the voltage level of CTL1~CTL3 is unstable, please connect R1~R3 with GND or V<sub>DD</sub> respectively.

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## RECOMMENDED PCB DESIGN



PCB: FR-4, t= 0.2mm  
Strip width: 0.4mm

Board total Loss (Capacitor, Connector, and PCB)

Pass route	800MHz Band (dB)	1.5GHz Band (dB)
TX-ANT1	0.23	0.30
TX-EXT1		
RX-ANT1	0.22	0.30
RX-ANT2		
RX-EXT1		
RX-EXT2		

### PARTS LIST

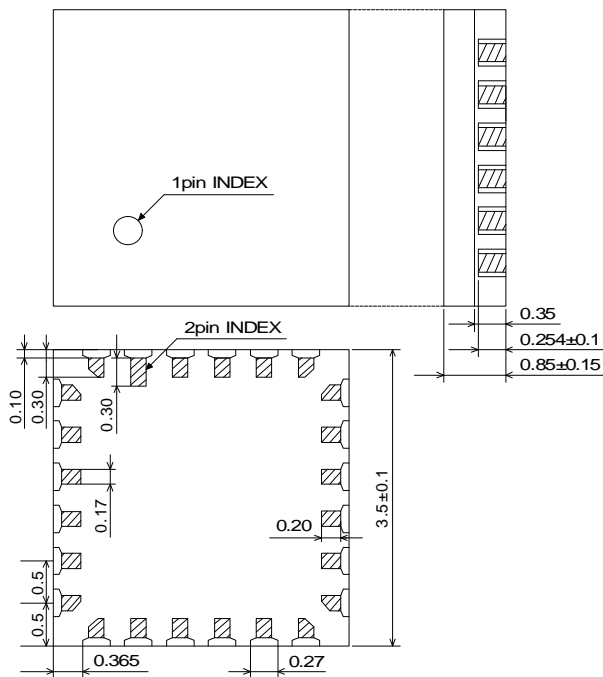
	VALUE		COMMENT
	800MHz Band	1.5GHz Band	
R1-R3	100KΩ		
C1, C2	1000pF		MURATA(GRM36)
C4, C5, C7, C8	56pF		MURATA(GRM36)
C3	16pF	7pF	MURATA(GRM36)
C6	22pF	9pF	MURATA(GRM36)
C9	10pF		MURATA(GRM36)
C10	5pF		MURATA(GRM36)
L1	15nH	6.8nH	TAIYO-YUDEN(HK1005)
L2	22nH	8.2nH	TAIYO-YUDEN(HK1005)

### PRECAUTIONS

- [1] The bypass capacitors should be connected to the V<sub>DD</sub>, V<sub>SS</sub> terminals as close as possible respectively.
- [2] For good RF performance, the ground terminals should be directly connected to the ground patterns and through-holes as close as possible by using relatively wide pattern.



## ■ PACKAGE OUTLINE (FFP24-E1)



UNITS	: mm
PCB	: Ceramic
OVER COAT	: Epoxy resin
LEAD SURFACE	: Au
WEIGHT	: 30mg

### Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

### [CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with