NCP1232

Microprocessor Monitor

The NCP1232 is a fully-integrated processor supervisor. It provides three important functions to safeguard processor functionality: precision power on/off reset control, watchdog timer and external reset override.

On power-up, the NCP1232 holds the processor in the reset state for a minimum of 250 msec after V_{CC} is within tolerance to ensure a stable system start-up.

Microprocessor functionality is monitored by the on-board watchdog circuit. The microprocessor must provide a periodic low-going signal on the $\overline{ST}$ input. Should the processor fail to supply this signal within the selected time-out period (150 msec, 600 msec or 1200 msec), an out-of-control processor is indicated and the NCP1232 issues a processor reset as a result.

The outputs of the NCP1232 are immediately driven active when the PB input is brought low by an external push-button switch or other electronic signal. When connected to a push-button switch, the NCP1232 provides contact debounce.

The NCP1232 is packaged in a space-saving 8-pin plastic SOIC package and requires no external components.

Features

- Precision Voltage Monitor
  (Adjustable +4.5 V or +4.75 V)
- Reset Pulse Width (250 msec Min)
- No External Components
- Adjustable Watchdog Timer
  (150 msec, 600 msec or 1.2 sec)
- Debounced Manual Reset Input for External Override

Applications

- Computers
- Controllers
- Intelligent Instruments
- Automotive Systems
- Critical μP Power Monitoring

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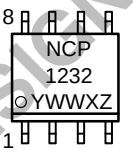
MARKING DIAGRAM

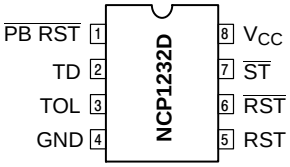
SO-8
D SUFFIX
CASE 751



YY, Y = Year
WW = Work Week
X = Assembly ID Code
Z = Subcontractor ID Code

PIN CONNECTIONS

8-Pin SOIC

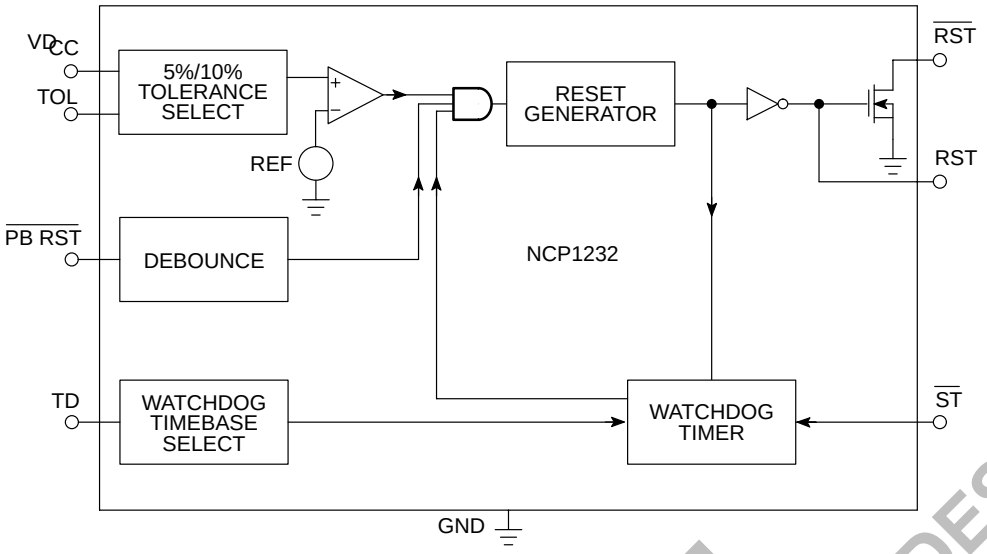


(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP1232DR2	SO-8	2500 Tape & Reel

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin No. (8-Pin SOIC)	Symbol	Description
1	PB RST	Push-button Reset Input. A debounced active-low input that ignores pulses less than 1 msec in duration and is guaranteed to recognize inputs of 20 msec or greater.
2	TD	Time Delay Set. The watchdog time-out select input (t_{TD} = 150 msec for TD = 0 V, t_{TD} = 600 msec for TD = open, t_{TD} = 1.2 sec for TD = V_{CC}.)
3	TOL	Tolerance Input. Connect to GND for 5% tolerance or to V_{CC} for 10% tolerance.
4	GND	Ground.
5	RST	Reset Output (Active High) - goes active: 1. If V_{CC} falls below the selected reset voltage threshold 2. If $\overline{\text{PB RST}}$ is forced low 3. If $\overline{\text{ST}}$ is not strobed within the minimum time-out period 4. During power-up
6	RST	Reset Output (Active Low, Open Drain) - see RST.
7	ST	Strobe Input. Input for watchdog timer.
8	V_{CC}	The +5 V Power Supply Input.

ABSOLUTE MAXIMUM RATINGS* Voltage on any pin (with respect to GND) -0.3 V to +5.8 V

Rating	Value	Unit
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range, T_{stg}	-65 to +150	°C
Lead Temperature (Soldering, 10 sec)	+300	°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; V_{CC} = +4.5 V to 5.5 V, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	-	4.5	5.0	5.5	V
$\overline{ST}$ and $\overline{PB\ RST}$ Input High Level	V_{IH}	Note 1	2.0	-	V_{CC} +0.3	V
$\overline{ST}$ and $\overline{PB\ RST}$ Input Low Level	V_{IL}	-	-0.3	-	+0.8	V
Input Leakage $\overline{ST}$, TOL	I_L	-	-1.0	-	+1.0	μA
Output Current RST	I_{OH}	V_{OH} = 2.4 V	-1.0	-12	-	mA
Current RST, $\overline{RST}$	I_{OL}	V_{OL} = 0.4 V	2.0	10	-	mA
Operating Current	I_{CC}	Note 2	-	50	200	μA
V_{CC} 5% Trip Point (Note 3)	V_{CCTP}	TOL = GND	4.50	4.62	4.74	V
V_{CC} 10% Trip Point (Note 3)	V_{CCTP}	TOL = V_{CC}	4.25	4.37	4.49	V

CAPACITANCE (Note 4) (T_A = +25°C)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance $\overline{ST}$, TOL	C_{IN}	-	-	-	5.0	pF
Output Capacitance RST, $\overline{RST}$	C_{OUT}	-	-	-	7.0	pF

AC ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; V_{CC} = +5.0 V to ±10%, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{PB\ RST}$ (Note 5)	t_{PB}	Figure 3	20	-	-	msec
$\overline{PB\ RST}$ Delay	t_{PBD}	Figure 3	1.0	4.0	20	msec
Reset Active Time	t_{RST}	-	250	610	1000	msec
$\overline{ST}$ Pulse Width	t_{ST}	Figure 4	20	-	-	nsec
$\overline{ST}$ Time-out Period	t_{TD}	Figure 4 TD Pin = 0 V TD Pin = Open TD Pin = V_{CC}	 62.5 250 500	 150 600 1200	 250 1000 2000	msec
V_{CC} Fall Time (Note 4)	t_F	Figure 5	10	-	-	μsec
V_{CC} Rise Time (Note 4)	t_R	Figure 6	0	-	-	μsec
V_{CC} Detect to RST High and $\overline{RST}$ Low	t_{RPD}	Figure 7, V_{CC} Falling	-	-	100	nsec
V_{CC} Detect to RST High and $\overline{RST}$ Open (Note 6)	t_{RPU}	Figure 8, V_{CC} Rising	250	610	1000	msec

1. $\overline{PB\ RST}$ is internally pulled up to V_{CC} with an internal impedance of typically 40 kΩ.
2. Measured with outputs open.
3. All voltages references to GND.
4. Guaranteed by design.
5. $\overline{PB\ RST}$ must be held low for a minimum of 20 msec to guarantee a reset.
6. t_R = 5 μsec.

Power Monitor

The NCP1232 detects out-of-tolerance power supply conditions and warns a processor-based system of an impending power failure. When V_{CC} is detected as below the preset level defined by TOL, the V_{CC} comparator outputs the signals RST and $\overline{RST}$. If TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. If TOL is connected to V_{CC}, the RST and $\overline{RST}$ become active as V_{CC} falls below 4.5 volts. Because the processing is stopped at the last possible moment of valid V_{CC}, the RST and $\overline{RST}$ are excellent control signals for a μP. The reset outputs will remain in their active states until V_{CC} has been continuously in-tolerance for a minimum of 250 msec allowing the power supply and μP to stabilize before $\overline{RST}$ is released.

Push-button Reset Input

The debounced manual reset input ($\overline{PB\ RST}$) manually forces the reset outputs into their active states. Once $\overline{PB\ RST}$ has been low for a time, t_{PBD}, the push-button delay time, the reset outputs go active. The reset outputs remain in their active states for a minimum of 250 msec after $\overline{PB\ RST}$ rises above V_{IH} (Figure 3).

A mechanical push-button or active logic signal can drive the $\overline{PB\ RST}$ input. The debounced input ignores input pulses less than 1 msec and is guaranteed to recognize pulses of 20 msec or greater. No external pull-up resistor is required because the $\overline{PB\ RST}$ input has an internal pull-up to V_{CC} of approximately 100 μA.

Watchdog Timer

When the $\overline{ST}$ input is not stimulated for a preset time period, the watchdog timer function forces RST and $\overline{RST}$ signals to the active state. The preset time period is determined by the $\overline{TD}$ inputs to be 150 msec with TD connected to ground, 600 msec with TD open, or 1200 msec with TD connected to V_{CC}, typical. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the ST input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 msec minimum (Figure 2).

The software routine that strobes $\overline{ST}$ is critical. The code must be in a section of software that is executed regularly so the time between toggles is less than the watchdog time-out period. One common technique controls the μP I/O line from two sections of the program. The software might set the I/O line high while operating in the foreground mode and set it low while in the background or interrupt mode. If both modes do not execute correctly, the watchdog timer issues reset pulses.

Supply Monitor Noise Sensitivity

The NCP1232 is optimized for fast response to negative-going changes in V_{DD}. Systems with an inordinate amount of electrical noise on V_{DD} (such as systems using relays), may require a 0.01 μF or 0.1 μF bypass capacitor to reduce detection sensitivity. This capacitor should be installed as close to the NCP1232 as possible to keep the capacitor lead length short.

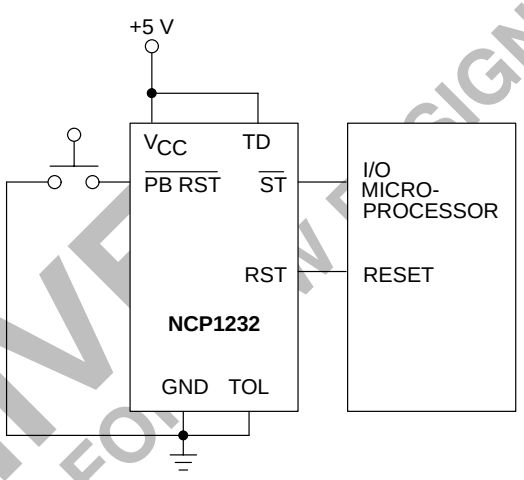


Figure 1. Push-button Reset

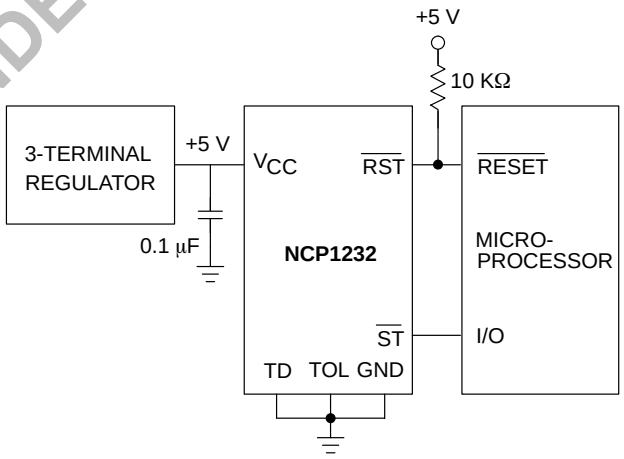


Figure 2. Watchdog Timer

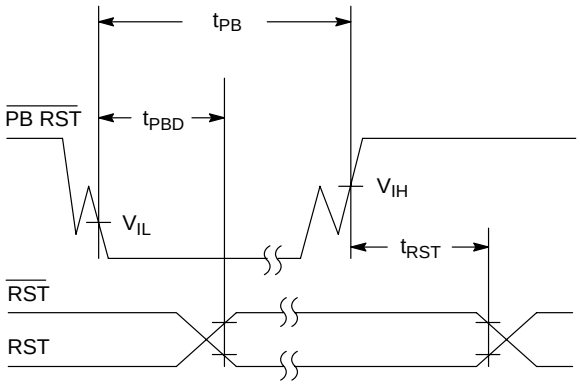


Figure 3. Push-button Reset. The debounced $\overline{PB\ RST}$ input ignores input pulses less than 1 msec and is guaranteed to recognized pulses of 20 msec or greater

PUSH-BUTT ON RESET

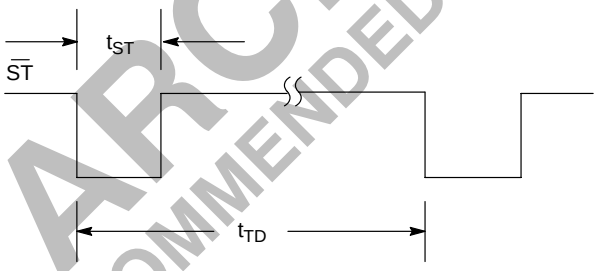


Figure 4. Strobe Input

NOTE: t_{TD} is the maximum elapsed time between $\overline{ST}$ high-to-low transistions ($\overline{ST}$ is activated by falling edges only) which will keep the watchdog timer from forcing the reset outputs active for a time of t_{RST}. t_{TD} is a function of the voltage at the TD pin, as tabulated below.

CONDITION	t_{TD} MIN	t_{TD} TYP	t_{TD} MAX
TD PIN = 0 V 62.5 msec	150 msec	250 msec	
TD PIN = OPEN	250 msec	600 msec	1000 msec
TD PIN = V_{CC} 500 msec	1200 msec	2000 msec	

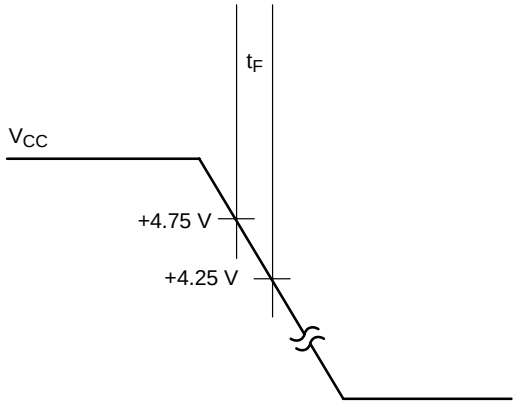


Figure 5. Power-Down Slew Rate

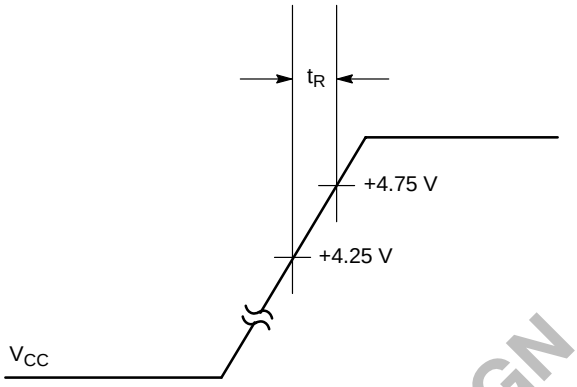


Figure 6. Power-Down Slew Rate

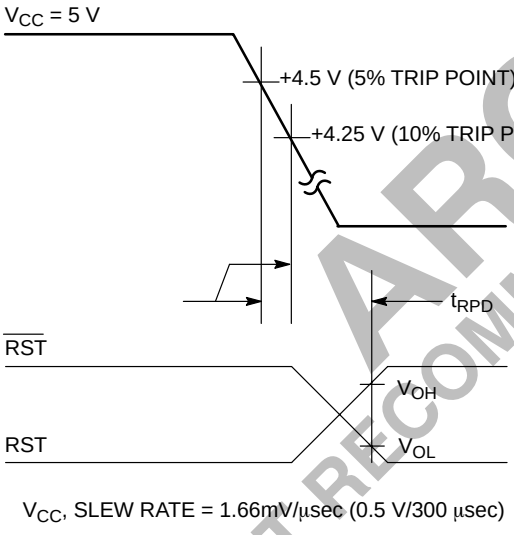


Figure 7. V_{CC} Detect Reset Output Delay (Power-Down)

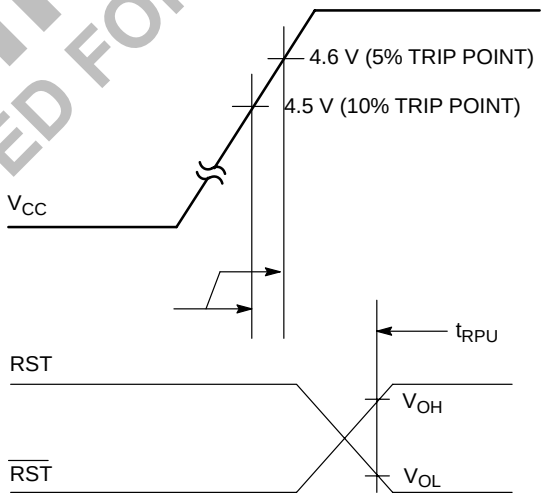
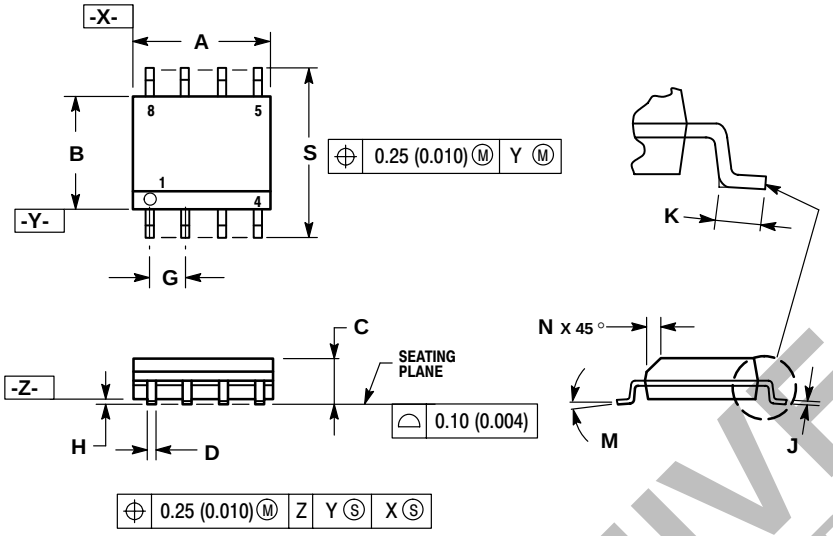


Figure 8. V_{CC} Detect Reset Output Delay (Power-Up)

PACKAGE DIMENSIONS

SO-8
D SUFFIX
CASE 751-07
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
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