# NCP1000, NCP1001, NCP1002

# Integrated Off-Line Switching Regulator

The NCP1000 through NCP1002 series of integrated switching regulators, combine a fixed frequency PWM controller with an integrated high voltage power switch circuit. This chip allows for simple design and minimal parts count for very low cost applications which utilize an ac input. This chip is designed to power a single ended topology, typically a discontinuous mode flyback, with secondary side sensing.

The internal high voltage switch circuit and startup circuit can function in continuous operation over a wide range of inputs, from 85 Vac to 265 Vac, and thus can be used in any existing power system in the world. Though inexpensive, these devices include a number of features such as undervoltage lockout, over−temperature protection, bandgap reference and leading edge blanking that make them an excellent value.

### Features

- Highly Integrated Solution
- Operates Over Universal Input Voltage Range (85 Vac to 265 Vac)
- On−board 700 V Power Switch Circuit
- Minimal External Parts Required
- Input Undervoltage Lockout with Hysteresis
- Very Low Standby Current
- No Minimum Load Requirement
- Opto Fail−Safe Shutdown Circuit
- Pb−Free Packages are Available*

### Typical Applications

- Cell Phone Chargers
- Wall Adapters
- On−board AC−DC Converters

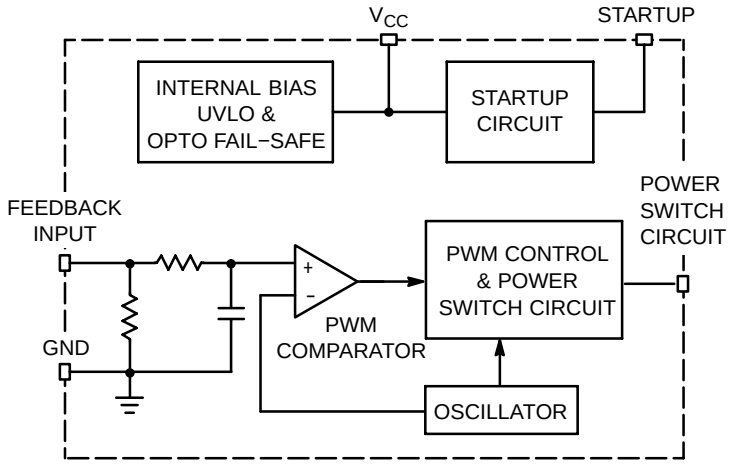


**Figure 1. Simplified Block Diagram**

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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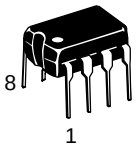
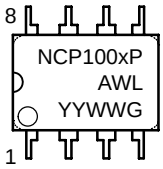



**PDIP−8**
**P SUFFIX**
**CASE 626**

Pin: 1. $V_{CC}$
2. Feedback Input
3, 6−8 Ground
4. Startup
5. Power Switch Circuit

**MARKING DIAGRAM**




x = Device Number 0, 1, or 2
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

**ORDERING INFORMATION***

| Device | Package | Shipping | Ipk Typ (A) | Ron Max (Ω) |
|---|---|---|---|---|
| NCP1000P | PDIP−8 | 50 Units/Rail | 0.5 | 18 |
| NCP1000PG | PDIP−8 (Pb−Free) | 50 Units/Rail | 0.5 | 18 |
| NCP1001P | PDIP−8 | 50 Units/Rail | 1.0 | 9 |
| NCP1001PG | PDIP−8 (Pb−Free) | 50 Units/Rail | 1.0 | 9 |
| NCP1002P | PDIP−8 | 50 Units/Rail | 1.5 | 6 |
| NCP1002PG | PDIP−8 (Pb−Free) | 50 Units/Rail | 1.5 | 6 |

*Consult factory for additional optocoupler fail−safe latching, frequency, and current limit options.

**FUNCTIONAL PIN DESCRIPTION**

| Pin | Function | Description |
|---|---|---|
| 1 | $V_{CC}$ | Positive input supply voltage. This pin is connected to an external capacitor for energy storage. The startup circuit sources current out of this pin to initially charge the capacitor. When the voltage reaches the upper threshold limit of the undervoltage lockout circuit, the startup circuit will turn off, and the power supply will begin operation. Power is then supplied to the chip via this pin, by virtue of the auxiliary winding. |
| 2 | Feedback Input | The error signal from the optocoupler is fed into this input. It is loaded with a 2.7 kΩ resistor which converts the opto current into a voltage. There is a 7.0 kHz, single pole, low pass filter between this pin and the error amp input. A 10 volt clamp is also connected to this pin to protect the device from ESD damage or overvoltage conditions. |
| 3, 6, 7, 8 | Ground | Ground reference pin for the circuit. These pins are part of the integrated circuit leadframe and are an integral part of the heat flow path on the PDIP−8 package. |
| 4 | Startup | This pin is connected to the bulk DC input voltage supply. It feeds an internal current source that initially charges up the $V_{CC}$ capacitor on power up. |
| 5 | Power Switch Circuit | The internal power switch circuit is connected between this pin and ground. This pin connects directly to one end of the transformer primary winding. |

**MAXIMUM RATINGS** (Notes 1 and 2)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Switch Circuit (Pin 5)<br>Drain Voltage Range<br>Drain Current Peak During Transformer Saturation | <br>$V_{DS}$<br>$I_{DS(pk)}$ | <br>−0.3 to 700<br>2.0 $I_{lim}$ Max | <br>V<br>A |
| Power Supply Voltage Range (Pin 1) | $V_{clp}$ | −0.3 to 10 | V |
| Feedback Input (Pin 2)<br>Voltage Range<br>Current | <br>$V_{I(fb)}$<br>$I_{fb}$ | <br>−0.3 to 10<br>100 | <br>V<br>mA |
| Thermal Resistance<br>P Suffix, Plastic Package Case 626<br>Junction−to−Lead<br>Junction−to−Air, 2.0 Oz. Printed Circuit Copper Clad<br>0.36 Sq. Inch<br>1.0 Sq. Inch | <br><br>$R_{\theta JL}$<br>$R_{\theta JA}$ | <br><br>5.0<br><br>45<br>35 | °C/W |
| Operating Junction Temperature | $T_J$ | −40 to 125 | °C |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1−3: Human Body Model 2000 V per MIL−STD−883, Method 3015.
   Machine Model Method 200 V.
   Pins 4 and 5 are the HV startup and the drain of the LDMOS device, rated only to the max rating of the part , or 700 V.
2. This device contains Latchup protection and exceeds ±200 mA per JEDEC Standard JESD78.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 8.6 volts, pin 2 grounded, $T_J$ = 25°C for typical values. For min/max values, $T_J$ is the operating junction temperature that applies.)

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | |
| Frequency ($I_{fb}$ = 1.1 mA) (Note 4) (Figure 7) | $f_{OSC}$ | | | | kHz |
| $T_J$ = 25°C | | 90 | 100 | 110 | |
| $T_J$ = 0°C to 125°C | | 85 | – | 115 | |
| $T_J$ = −40°C to 125°C | | 75 | – | 115 | |
| **PWM COMPARATOR** | | | | | |
| Feedback Input PWM Gain ($T_J$ = 25°C) ($I_{fb}$ = 1.20 mA to 1.30 mA) (Figure 2) | $A_v$ | −110 | – 136 | −170 | %/mA |
| Gain Temperature Coefficient ($T_J$ = −40°C to $T_J$ = 125°C) (Note 4) | $\Delta A_v$ | – | 0.2 | – | (%/mA)/°C |
| PWM Duty Cycle (Pin 2) | | | | | |
| Maximum ($I_{fb}$ = 0.8 mA) | $D_{(max)}$ | 68 | 72 | 74 | % |
| Zero Duty Cycle Current | $I_{fb}$ | 1.8 | – | – | mA |
| PWM Ramp | | | | | V |
| Peak | $V_{rpk}$ | – | 4.1 | – | |
| Valley | $V_{rvly}$ | – | 2.7 | – | |
| **STARTUP CONTROL AND $V_{CC}$ LIMITER** | | | | | |
| Undervoltage Lockout (Figure 8) | | | | | V |
| $V_{CC}$ Clamp Voltage ($I_{CC}$ = 4.0 mA) | $V_{clp}$ | 8.3 | 8.55 | 8.9 | |
| Startup Threshold ($V_{clp}$ Increasing) | $V_{clp(on)}$ | 8.2 | 8.5 | 8.8 | |
| Minimum Operating Voltage After Turn−On | $V_{clp(min)}$ | 7.2 | 7.5 | 8.0 | |
| Hysteresis | $V_H$ | – | 1.0 | – | |
| Startup Circuit, Pin 1 Output Current (Pin 4 = 50 V) | $I_{start}$ | | | | mA |
| $V_{CC}$ = 0 V | | 2.0 | 3.4 | 4.2 | |
| $V_{CC}$ = 8.0 V | | 1.5 | 2.6 | 4.2 | |
| Minimum Startup Voltage ($V_{CC}$ = $V_{clp(on)}$ −0.2 V, $I_{start}$ = 0.5 mA) | $V_{start}$ | – | 14.7 | 20 | V |
| Auto Restart ($C_{Pin\ 1}$ = 47 μF, Pin 4 = 50 V) (Note 5) | | | | | |
| Duty Cycle | $D_{rst}$ | 4.0 | 5.0 | 6.0 | % |
| Frequency | $f_{rst}$ | – | 1.2 | – | Hz |
| Startup Circuit Breakdown Voltage (I = 25 μA) (Note 5) | $V_{BR(st)}$ | 700 | – | – | V |
| Startup Circuit Leakage Current (Pin 4 = 700 $V_{DC}$) | $I_{leak}$ | | | | μA |
| $T_J$ = 25°C | | – | 20 | 40 | |
| $T_J$ = −40°C to 125°C | | – | 30 | 75 | |

3. Maximum package power dissipation limits must be observed.
4. Tested junction temperature range for this device series: $T_{low}$ = −40°C, $T_{high}$ = +125°C
5. Guaranteed by design only.

## ELECTRICAL CHARACTERISTICS

| Characteristics | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **POWER SWITCH CIRCUIT** | | | | | |
| Power Switch Circuit On−State Resistance | $R_{(on)}$ | | | | Ω |
| NCP1000 ($I_D$ = 50 mA) | | | | | |
| $T_J$ = 25°C | | − | 13 | 18 | |
| $T_J$ = 125°C (Note 8) | | − | 24 | 36 | |
| NCP1001 ($I_D$ = 100 mA) | | | | | |
| $T_J$ = 25°C | | − | 7.0 | 9.0 | |
| $T_J$ = 125°C (Note 8) | | − | 14 | 18 | |
| NCP1002 ($I_D$ = 150 mA) | | | | | |
| $T_J$ = 25°C | | − | 4.0 | 6.0 | |
| $T_J$ = 125°C (Note 8) | | − | 8.0 | 12 | |
| Power Switch Circuit Breakdown Voltage ($I_{D(off)}$ = 100 μA, $T_J$ = 25°C) | $V_{(BR)}$ | 700 | − | − | V |
| Power Switch Circuit Off−State Leakage Current ($V_{DS}$ = 650 V) | $I_{(off)}$ | | | | μA |
| $T_J$ = 25°C | | − | 0.25 | 1.0 | |
| $T_J$ = −40°C to 125°C | | − | − | 50 | |
| Switching Characteristics ($V_{DS}$ = 50 V, $R_L$ set for $I_D$ = 0.7 $I_{lim}$) | | | | | ns |
| Turn−on Time (90% to 10%) | $t_{on}$ | − | 50 | − | |
| Turn−off Time (10% to 90%) | $t_{off}$ | − | 50 | − | |
| **CURRENT LIMIT AND THERMAL PROTECTION** | | | | | |
| Current Limit Threshold ($T_J$ = 25°C) (Note 9) | $I_{lim}$ | | | | A |
| NCP1000 | | 0.42 | 0.48 | 0.54 | |
| NCP1001 | | 0.84 | 0.96 | 1.08 | |
| NCP1002 | | 1.26 | 1.43 | 1.6 | |
| Current Limit, Peak Switch Current | $I_{pk}$ | | | | A |
| NCP1000 (di/dt = 100 mA/μs) | | − | 0.500 | − | |
| NCP1001 (di/dt = 200 mA/μs) | | − | 1.000 | − | |
| NCP1002 (di/dt = 300 mA/μs) | | − | 1.500 | − | |
| Opto Fail−safe Protection (Figure 12) | $I_{Ofail}$ | | | | mA |
| $T_J$ = 25°C | | − | 18 | 25 | |
| $T_J$ = 0°C to 125°C | | 10 | − | 35 | |
| Propagation Delay, Current Limit Threshold to Power Switch Circuit Output (Leading Edge Blanking plus Current Limit Delay) | $t_{PLH}$ | − | 220 | − | ns |
| Thermal Protection (Note 6, 8) | | | | | °C |
| Shutdown (Junction Temperature Increasing) | $t_{sd}$ | 125 | 140 | − | |
| Hysteresis (Junction Temperature Decreasing) | $t_H$ | − | 30 | − | |
| **TOTAL DEVICE** (Pin 1) | | | | | |
| Power Supply Current After UVLO Turn−On | | | | | mA |
| Power Switch Circuit Enabled | $I_{CC1}$ | | | | |
| NCP1000 | | − | 1.2 | 1.6 | |
| NCP1001 | | − | 1.4 | 1.8 | |
| NCP1002 | | − | 1.6 | 2.0 | |
| Power Switch Circuit Disabled | $I_{CC2}$ | 0.6 | 1.0 | 1.25 | |

6. Maximum package power dissipation limits must be observed.
7. Tested junction temperature range for this device series:
   $T_{low}$ = −40°C $T_{high}$ = +125°C
8. Guaranteed by design only.
9. Actual peak switch current is increased due to the propagation delay time and the di/dt (see Figure 16).

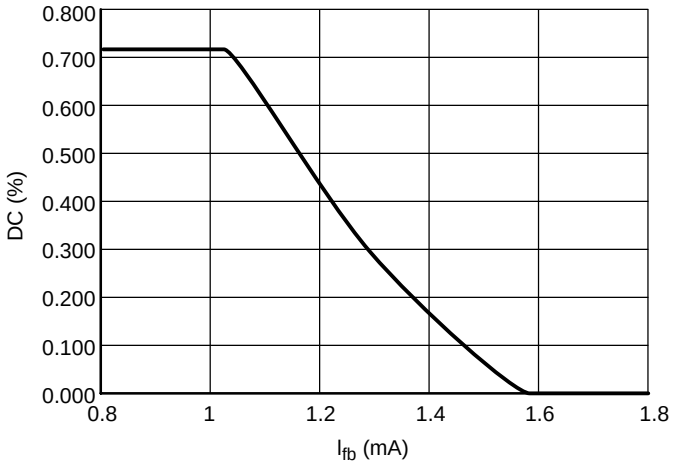



**Figure 2. Duty Cycle vs. FB Input Current**

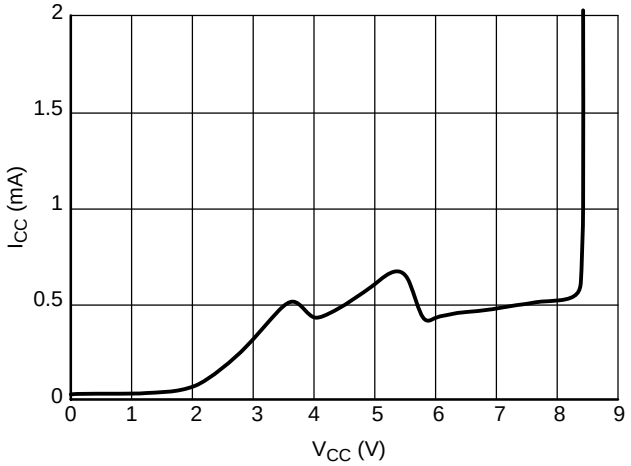



**Figure 3. $I_{CC}$ vs. $V_{CC}$**

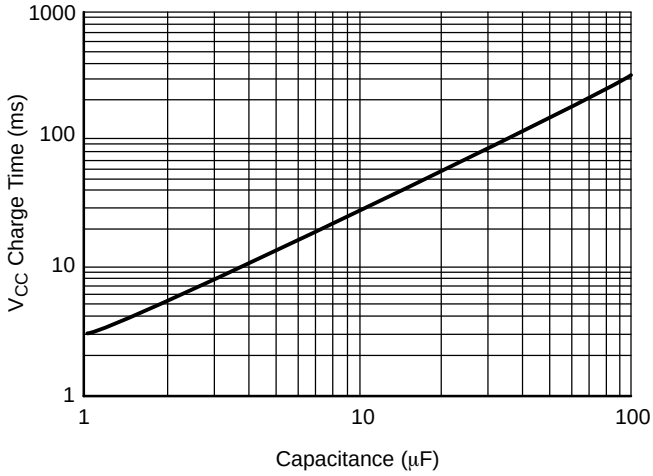



**Figure 4. Charge Time vs. $V_{CC}$ Capacitance**

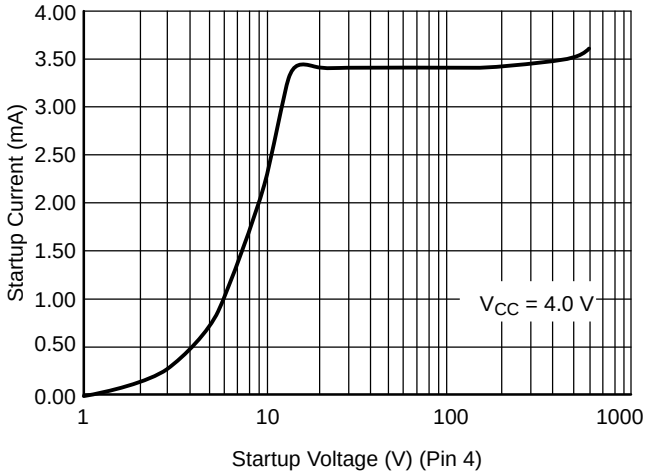



**Figure 5. Startup Current vs. Startup Voltage**

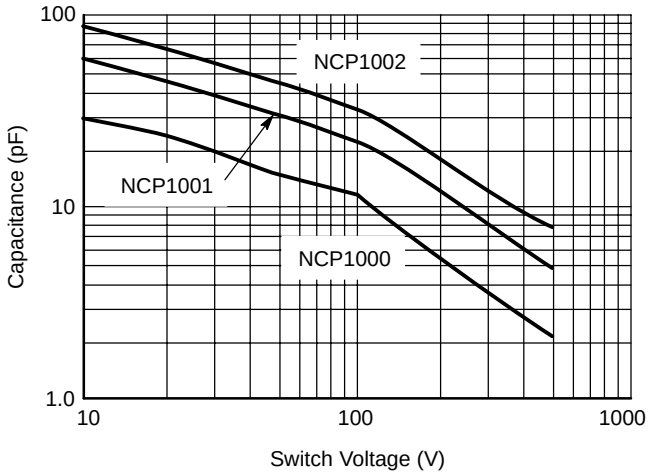



**Figure 6. Power Switch Circuit Capacitance vs. Voltage**

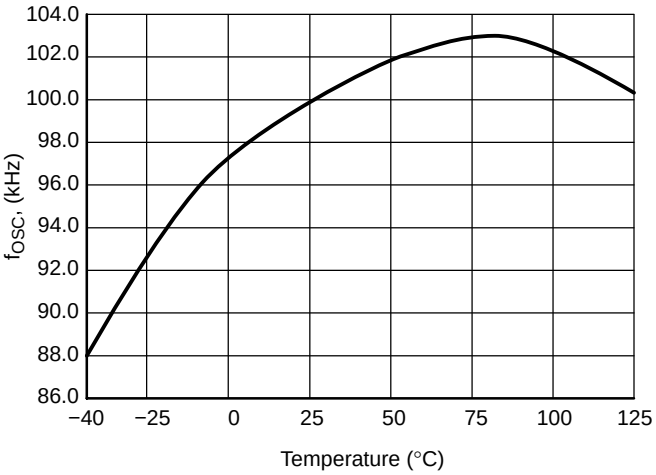



**Figure 7. Oscillator Frequency vs. Temperature**

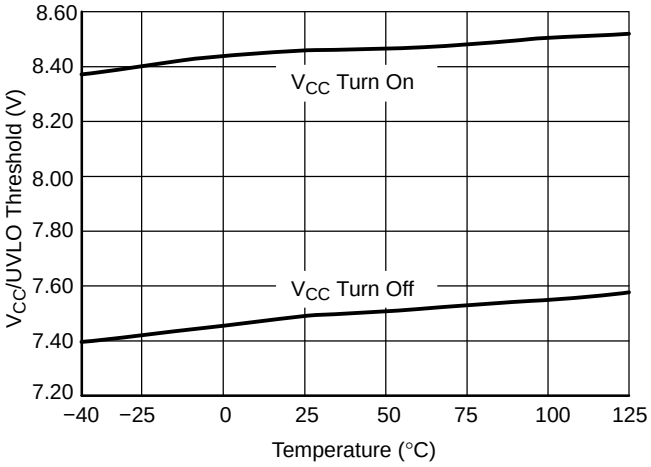



**Figure 8. $V_{CC}$/UVLO Threshold vs. Temperature**

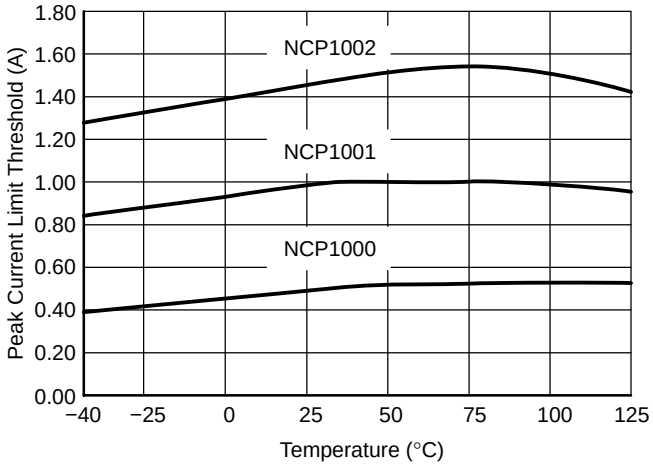



**Figure 9. Peak Current Limit Threshold vs. Temperature**

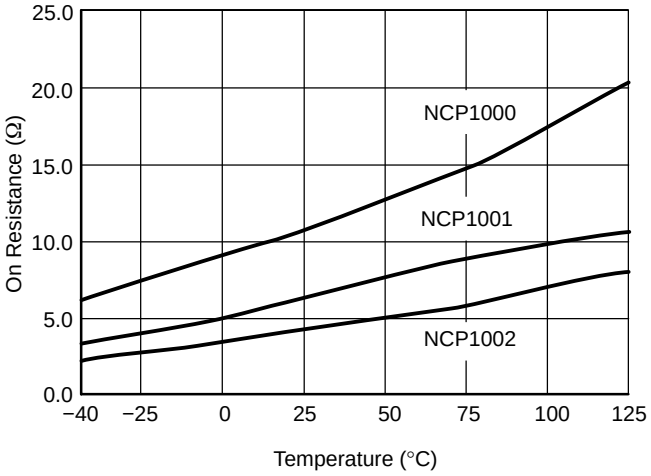



**Figure 10. Power Switch Circuit On Resistance vs. Temperature**

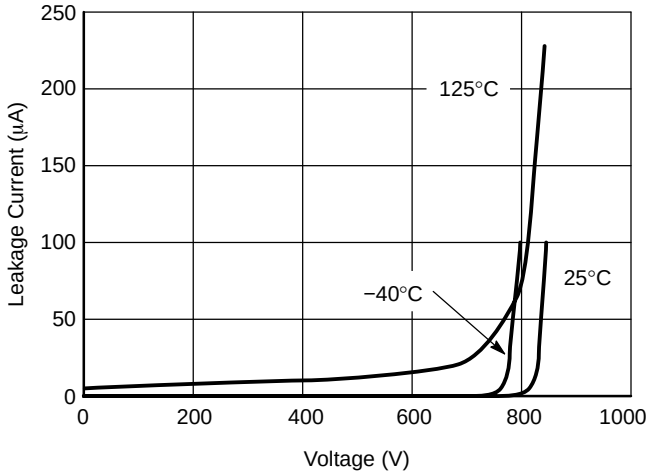



**Figure 11. Power Switch Circuit Leakage Current vs. Pin 5 Voltage**

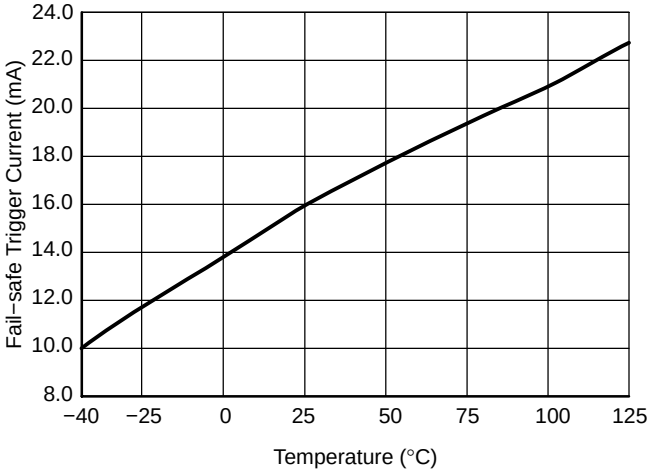



**Figure 12. Opto Fail−safe Trigger Current vs. Temperature**

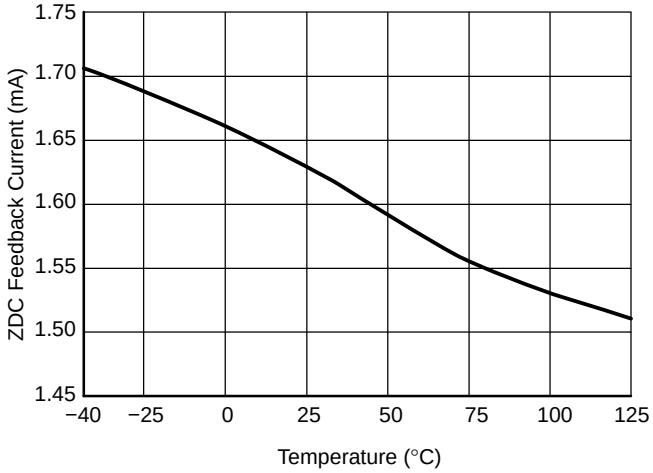



**Figure 13. Zero Duty Cycle Feedback Current vs. Temperature**

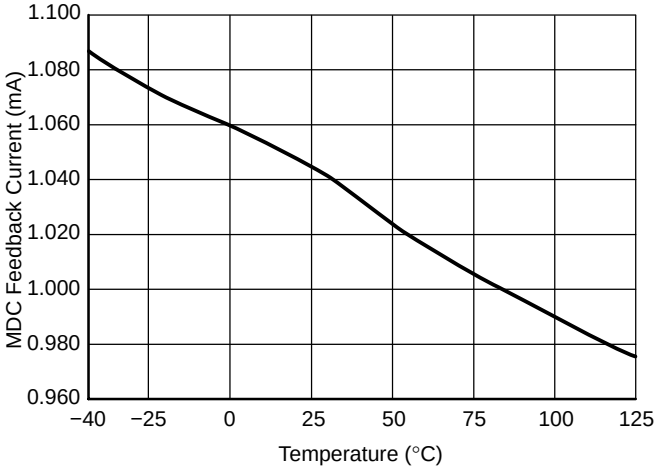



**Figure 14. Maximum Duty Cycle Feedback Current vs. Temperature**

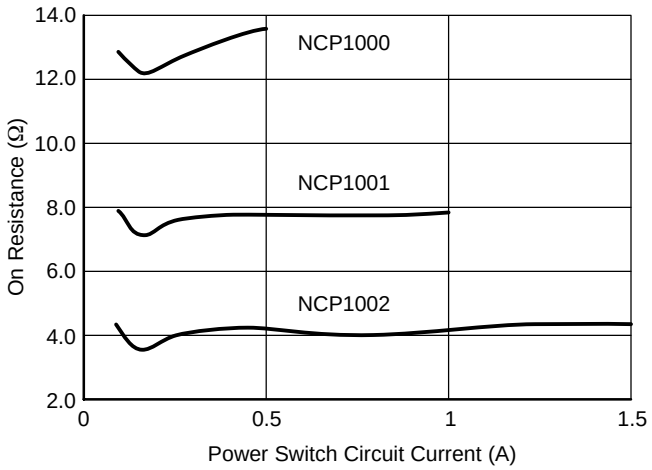



**Figure 15. On Resistance vs. Current**

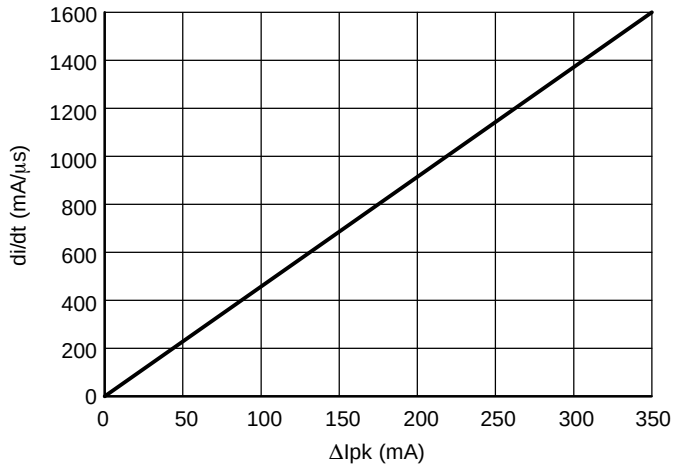



**Figure 16. Power Switch Circuit di/dt vs. ΔIpk**

## OPERATING DESCRIPTION

### Introduction

The NCP1000 thru NCP1002 represent a new higher level of integration by providing on a single monolithic chip all of the active power, control, logic, and protection circuitry required to implement a high voltage flyback or forward converter. This device series is designed for direct operation from a rectified 240 Vac line source and requires minimal external components for a complete cost sensitive converter solution. Potential markets include office automation, industrial, residential, personal computer, and consumer. A description of each of the functional blocks is given below, and the representative block diagram is shown in Figure 17.

### Oscillator

The Oscillator block consists of two comparators that alternately gate on and off a trimmed current source and current sink which are used to respectively charge and discharge an on−chip timing capacitor between two voltage levels. This configuration generates a precise linear sawtooth ramp signal that is used to pulse width modulate the MOSFET of the Power Switch circuit. During the charge of the timing capacitor, the Oscillator duty cycle output holds one input of the Driver low. This action keeps the MOSFET of the Power Switch Circuit off, thus limiting the maximum duty cycle. The Oscillator frequency is internally programmed for 100 kHz operation with a controlled charge to discharge current ratio that yields a maximum Power Switch Circuit duty cycle of 72%. The Oscillator temperature characteristics are shown in Figure 7.

### PWM Comparator and Latch

The pulse width modulator (PWM) consists of a comparator with the Oscillator ramp output applied to the inverting input. The Oscillator clock output applies a set pulse to the PWM Latch when the timing capacitor reaches its peak voltage, initiating Power Switch Circuit conduction. As the timing capacitor discharges, the ramp voltage decreases to a level that is less than the Error Amplifier output, causing the PWM Comparator to reset the latch and terminate Power Switch Circuit conduction for the duration of the ramp−down period. This method of having the Oscillator set and the PWM Comparator reset the Latch prevents the possibility of multiple output pulses during a given Oscillator clock cycle. This circuit configuration is commonly referred to as double pulse suppression logic. A timing diagram is shown in Figure 18 that illustrates the behavior of the pulse width modulator.

No load operation. The pulse width modulator is designed to operate between 73% and 0% duty cycle. The ability to operate down to zero duty cycle allows for no load operation without the burden of preloads. This feature is consistent with the Blue Angle requirements, as it minimizes power consumption while in the standby operation mode. For operation at no load, the output may skip cycles. This is a common occurrence for this type of control circuit. The converter will switch for several cycles, and due to delays in the output filter and feedback loop, the duty cycle will not be reduced until the output has exceeded it's regulation limit. The unit will then shut down for several cycles until the voltage is below the regulation limit, and then it will switch again. During the time that switching cycles are not present the output voltage will decay according to it's RC time constant, which is based on the output capacitance and internal loading from the regulation circuitry. During this interval, the voltage on the $V_{CC}$ supply will also decay. If it decays below the lower hysteretic turn off threshold, the unit will shut down and recycle. This mode of operation is not normally desirable. In order to avoid it, **the time constant for the $V_{CC}$ cap and load should be equal to, or greater than the time constant of the output.** If no load operation is not required, a relatively small value ($< 10$ μF) for the $V_{CC}$ capacitor is acceptable.

### Feedback Input

The feedback input, pin 2, accepts the DC error signal that feeds the non−inverting input to the PWM. Pin 2 has a nominal 2.7 kΩ internal resistor to ground, which converts the optocoupler current into a voltage. Its' signal is filtered by a 7.0 kHz low pass filter which reduces high frequency noise to the input of the PWM comparator.

Typically, the photo transistor of the optocoupler is connected between $V_{CC}$ (pin 1) and the Feedback input (pin 2). The photo transistor is effectively a current source which is driven by the LED, which is connected to the output regulation circuit of the power supply. An external capacitor may be connected from pin 2 to ground for additional noise filtering if necessary.

When the feedback input is below the lower threshold of the ramp signal, the output of the power converter will be operating at full duty cycle. The input current vs. duty cycle transfer function is shown in Figure 2. As the voltage increases, the duty cycle will vary linearly with the change in voltage at the feedback input, between the upper and lower extremes of the ramp waveform 2.7 V to 4.1 V. Above the upper extreme point of the ramp, the duty cycle will be zero and no power will be transmitted to the output.

The circuit should be designed such that when the output is low, the optocoupler will be off, leaving the voltage at pin 2 at ground (full duty cycle). As the output voltage increases, the optocoupler will begin to conduct, such that the voltage at pin 2 increases until the proper duty cycle is reached to maintain regulation.

Pin 2 is protected from ESD transients by a 10 V Zener diode to ground.

### Current Limit Comparator and Power Switch Circuit

The NCP1000 series uses cycle−by−cycle current limiting as a means of protecting the output switch transistor from overstress. Current limiting is implemented by monitoring the instantaneous output switch current during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the Oscillator ramp−down period.

The Power Switch Circuit is constructed using a SENSEFET™ allowing a virtually lossless method of monitoring the drain current. A small number of the power MOSFET cells are used for current sensing by connecting their individual sources to a single ground referenced sense resistor, $R_{pk}$. The current limit comparator detects if the voltage across $R_{pk}$ exceeds the reference level that is present at the noninverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch Circuit. Figure 9 shows that this detection method yields a relatively constant current limit threshold over temperature. The high voltage Power Switch Circuit is integrated with the control logic circuitry and is designed to directly drive the converter transformer. The Power Switch Circuit is capable of switching 700 V with an associated drain current that ranges from 0.5 A to 1.5 A. Proper drain voltage snubbing during converter startup and overload is mandatory for reliable device operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path to prevent a premature reset of the PWM Latch. A potential premature reset signal is generated each time the Power Switch Circuit is driven into conduction and appears as a narrow voltage spike across current sense resistor $R_{pk}$. The spike is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior that masks the current signal until the Power Switch Circuit turn−on transition is completed.

The current limit propagation delay time is typically 220 ns. This time is measured from when an overcurrent appears at the Power Switch Circuit drain, to the beginning of turn−off. Care must be taken during transformer saturation so that the maximum device current limit rating is not exceeded. To determine the peak Power Switch Circuit current at turn off, the effect of the propagation delay must be taken into account. To do this, use the appropriate Current Limit Threshold value from the electrical tables, and then add the ΔIpk based on the di/dt from Figure 16. The di/dt of the circuit can be calculated by the following formula:

$$di/dt\ (A/\mu s) = V/L$$

where:

V is the rectified, filtered input voltage (volts)

L is the primary inductance of the flyback transformer (Henries)

### High Voltage Startup

The NCP1000−1002 contain an internal startup circuit that eliminates the need for external startup components. In addition, this circuit increases the efficiency of the supply as it uses no power when in the normal mode of operation, but instead uses the power supplied by the auxiliary winding.

Rectified, filtered ac line voltage is connected to pin 4. An internal JFET allows current to flow from the startup pin, to the $V_{CC}$ pin at a current of approximately 3.0 mA. Figure 5 shows the startup current out of pin 1 which charges the capacitor(s) connected to this pin.

The start circuit will be enhanced (conducting) when the voltage at Pin 1 ($V_{CC}$) is less than 7.5 V. It will remain enhanced until the $V_{CC}$ voltage reaches 8.5 V. At this point the Power Switch Circuit will be disabled, and the unit will generate voltage via the auxiliary winding to maintain proper operation of the device. Figure 4 shows the charge time for turn−on vs. $V_{CC}$ capacitance when the unit is initially energized.

If the $V_{CC}$ voltage drops below 7.5 V (e.g. current limit mode), the start circuit will again begin conducting, and will charge up the $V_{CC}$ cap until the 8.5 V limit is reached.

### $V_{CC}$ Limiter and Undervoltage Lockout

The undervoltage lockout (UVLO) is designed to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. It inhibits operation of the major functions of the device by disabling the Internal Bias circuitry, and assures that the Power Switch Circuit remains in its “off’’ state as the bias voltage is initially brought up from zero volts. When the NCP100x is in the “off’’ state, the High Voltage Startup circuit is operational. The UVLO is a hysteretic switch and will hold the device in its “off’’ state any time that the $V_{CC}$ voltage is less than 7.5 V. As the $V_{CC}$ increases past 7.5 V, the NCP100x will remain off until the upper threshold of 8.6 V is reached. At this time the power converter is enabled and will commence operation. The UVLO will allow the unit to continue to operate as long as the $V_{CC}$ voltage exceeds 7.5 V. The temperature characteristics of the UVLO circuit are shown in Figure 8.

If the converter output is overloaded or shorted, the device will enter the auto restart mode. This happens when the auxiliary winding of the power transformer does not have sufficient voltage to support the $V_{CC}$ requirements of the chip. Once the chip is operational, if the $V_{CC}$ voltage falls below 7.5 V the unit will shut down, and the High Voltage Startup circuit will be enabled. This will charge the $V_{CC}$ cap up to 8.5 V, which will clock the divide by eight counter. The divide by eight counter holds the Power Switch Circuit off. This causes the $V_{CC}$ cap to discharge. It will continue to discharge and recharge for eight consecutive cycles. After the eighth cycle, the unit will turn on again. If the fault remains, the unit will again cycle through the auto restart mode; if the fault has cleared the unit will begin normal operation. The auto restart mode greatly reduces the power dissipation of the power devices in the circuit and improves

reliability in overload conditions. Figure 20 shows the timing waveforms in auto restart mode.

The $V_{CC}$ pin receives its startup power from the high voltage startup circuit. Once the undervoltage lockout trip point is exceeded, the high voltage startup circuit turns off, and the $V_{CC}$ pin receives its power from the auxiliary winding of the power transformer. Once the converter is enabled, the $V_{CC}$ voltage will be clamped by the 8.6 V limiter. Since the voltage limiter will regulate the $V_{CC}$ voltage at 8.6 V, it must shunt all excess current based on the input impedance to this pin. A resistor is required between the auxiliary winding filter capacitor and the $V_{CC}$ pin to limit the current.

### Optocoupler Fail−safe Circuit

The NCP100x has the ability to sense an open optocoupler and protect the load in the event of a failure. This circuit operates by sensing the current in the $V_{CC}$ limiter, and detecting a high current which is an indication of an open optocoupler.

The $V_{CC}$ pin receives the output of a current source which is created by the voltage drop between the auxiliary winding and the $V_{CC}$ limiter across the shunt resistor. The Vcc limiter will clamp the $V_{CC}$ voltage to approximately 8.6 V. Any current that is available at this pin, that is not needed for either the chip bias current, or the opto current is shunted through this limiter.

The opto fail−safe circuit operates on the premise that under an open opto condition, the opto current will all be shunted through the $V_{CC}$ limiter, and the output voltage (and therefore the auxiliary winding voltage) will increase. The increase in auxiliary winding voltage will cause an amplified increase in the current into the $V_{CC}$ pin. To detect an open opto condition, the current in the limiter is measured and if it exceeds 10 milliamps, the chip will shut down and go into burst mode operation. After a shutdown signal, the optocoupler fail−safe circuit will enable the divide−by−eight counter and attempt to restart the unit after every eight $V_{CC}$ cycles.

For this circuit to operate properly, the shunt resistor must be chosen prudently. There is a range of values for $R_S$ that will determine the operation of this circuit. On one extreme, a large value of $R_S$ will minimize the bias current, which will have the effect of maximizing efficiency, while reducing the response to an open optocoupler. The other extreme is the minimum value of $R_S$, which will maximize the bias current into the chip and minimize the voltage overshoot in the event of an open optocoupler.

For minimum bias current:

$$Rs_{max} = \frac{(V_{AUX\,min} - 8.8\ volts)}{I_{CC1max}}$$

where:

$V_{AUXmin}$ is the minimum expected DC voltage from the auxiliary winding.

Typically, this voltage will vary between $\pm 5\%$ to $\pm 10\%$ from it's nominal value.

$I_{CC1max}$ is the maximum rated bias current for the device used. This value can found in the tables on the data sheet.

For the best optocoupler fail−safe response:

$$Rs_{min} = \frac{(V_{AUX\,max} - 7.2\ volts)}{1.0mA + I_{trip}}$$

where:

$V_{AUXmax}$ is the maximum expected DC voltage from the auxiliary winding.

$I_{trip}$ is the minimum trip current for the optocoupler fail−safe. This information can be found in the tables under ***Current Limit and Thermal Protection***, as well as in Figure 12.

The value of $R_S$ that is used in the circuit must be between the two extreme values calculated. Setting it closer to $R_{Smin}$ will optimize the optocoupler fail−safe feature, while setting it closer to the $R_{Smax}$ value will minimize the bias current

### Thermal Shutdown and Package

The internal Thermal Shutdown block protects the device in the event that the maximum junction temperature is exceeded. When activated, typically at 140°C, one input of the Driver is held low to disable the Power Switch Circuit. Thermal shutdown activation is non−latching and the Power Switch Circuit is allowed resume operation when the junction temperature falls below 110°C. The thermal shutdown feature is provided to prevent catastrophic device failures from accidental overheating. It is not intended to be used as a substitute for proper heatsinking.

The die in the 8−pin dual−in−line package is mounted on a special heat tab copper alloy lead frame. The tab consists of pins 3, 6, 7, 8 is specifically designed to improve the thermal conduction from the die to the printed circuit board. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance.

### Applications

**Do not attempt to construct a converter circuit on a wire−wrap or plug−in prototype board.** In order to ensure proper device operation and stability, it is important to minimize the lead length and the associated inductance of the ground pin. This pin must connect as directly as possible to the printed circuit ground plane and should not be bent or offset by the board layout. The Power Switch Circuit pin can be offset if additional layout creepage distance is required. Due to the potentially high rate of change in switch current, a capacitor (if used), at pin 2, should have traces as short as possible, from pin 2 and ground. This will significantly reduce the level of switching noise that can be imposed upon the feedback control signal.

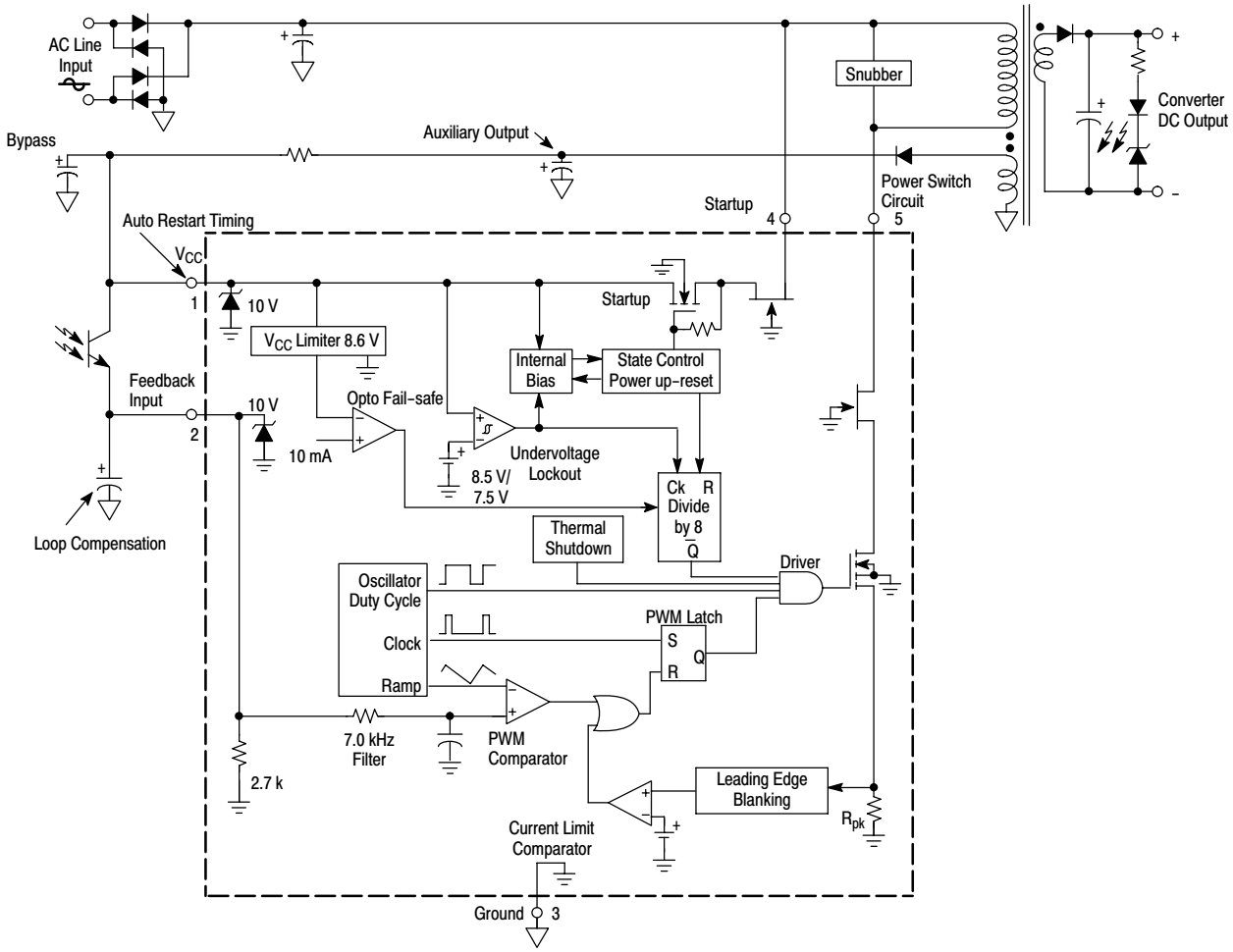



**Figure 17. Representative Block Diagram**

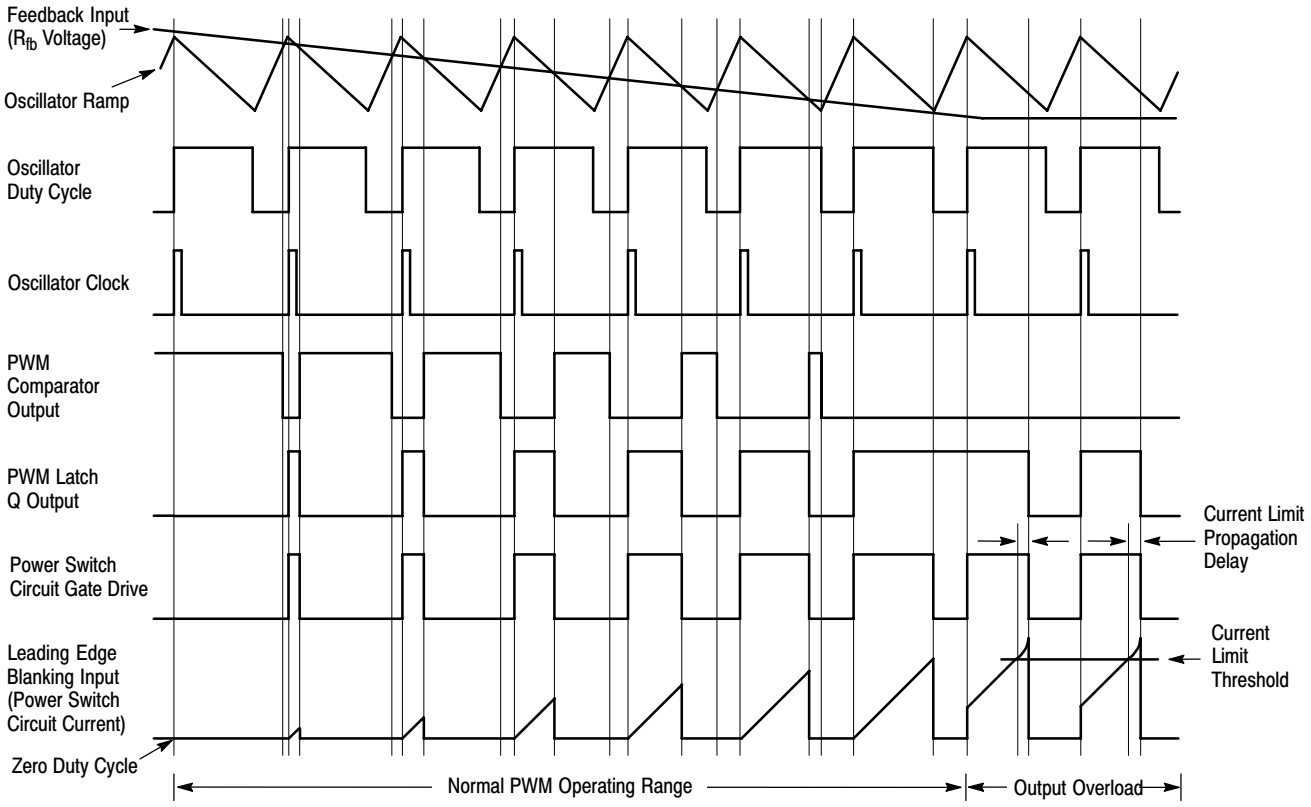



**Figure 18. Pulse Width Modulation Timing Diagram**

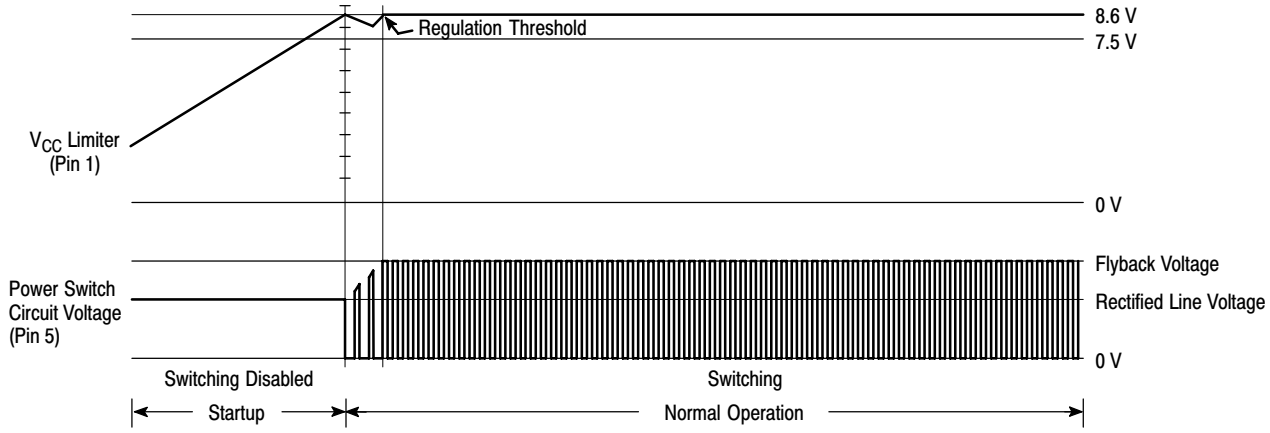



**Figure 19. Startup and Normal Operation Timing Diagram**

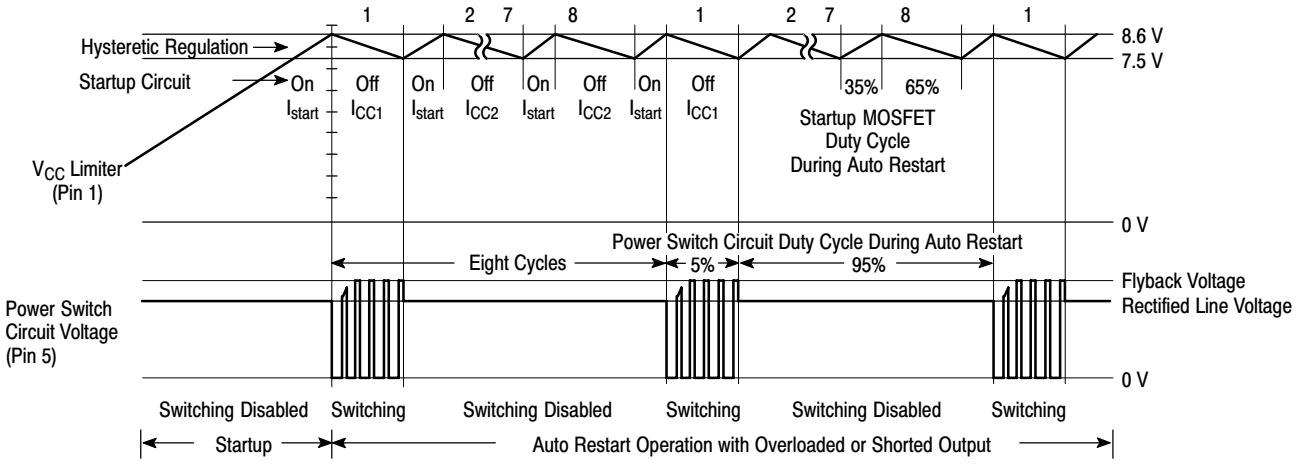



**Figure 20. Auto Restart Operation Timing Diagram**

## APPLICATIONS INFORMATION

### APPLICATION #1: Offline Converter Provides 5.0 V, 1.0 A Output for Small Electronic Equipment

ON Semiconductor's NCP1000 series of offline converters offers a low cost, high efficiency power source for low power, electronic equipment. It serves the same function as small, line frequency transformers, but with the added benefits of line and load regulation, transient suppression, reduction in weight, and operation across the universal input voltage range.

This kit provides a 5.0 V, 1.0 A output, which is derived from an input source of 85 to 265 Vac, and 50 Hz to 60 Hz. This range of input voltages will allow this circuit to function virtually anywhere in the world without modification. The output is regulated and current limited, and EMI filters are included on both the input and output.

**Converter Test Data**

| Parameter | Conditions | Data |
|---|---|---|
| Line Regulation | 85 v ≤ Vin ≤ 265 v | ΔVo = 6.0 mV |
| Load Regulation | 0 A ≤ Io ≤ 1.0 A | ΔVo = 8.0 mV |
| Combined Line/ Load Regulation | 85 v ≤ Vin ≤ 265 v<br>.09 A ≤ Io ≤ 1.0 A | ΔVo = 10 mV |
| Output Ripple | Io = 1.0 A | 100 $mV_{pp}$ |
| Input Power | $V_{in}$ = 115 v, Io = 1.0 A<br>$V_{in}$ = 220 v, Io = 1.0 A | 7.75 watts<br>7.88 watts |
| Power Factor | $V_{in}$ = 115 v, Io = 1.0 A<br>$V_{in}$ = 220 v, Io = 1.0 A | −.57<br>−.49 |
| Efficiency | $V_{in}$ = 115 v, Io = 1.0 A<br>$V_{in}$ = 220 v, Io = 1.0 A | η = 66%<br>η = 64% |

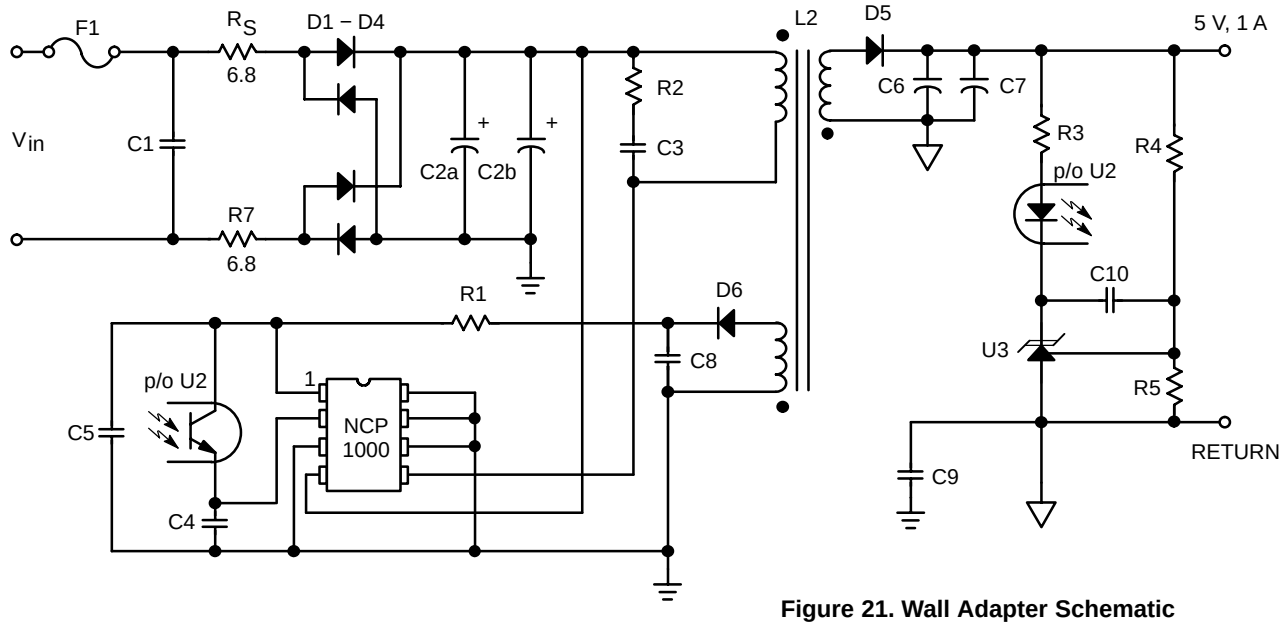
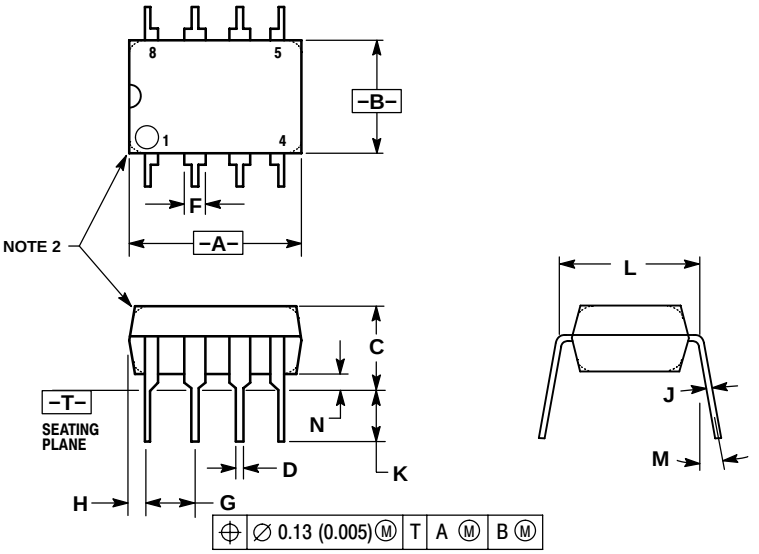



**Figure 21. Wall Adapter Schematic**

For additional information on this application, please order application note AND8019/D from the Literature Distribution Center or download from our website at http://onsemi.com.

## PACKAGE DIMENSIONS

**PDIP−8**
**P SUFFIX**
CASE 626−05
ISSUE L




NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.40 | 10.16 | 0.370 | 0.400 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.94 | 4.45 | 0.155 | 0.175 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.76 | 1.27 | 0.030 | 0.050 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | --- | 10° | --- | 10° |
| N | 0.76 | 1.01 | 0.030 | 0.040 |

The products described herein (NCP1000, 1001, 1002), may be covered by one or more of the following U.S. patents: 4,553,084; 5,418,410; 5,477,175; 5,760,639; 5,859,768. There may be other patents pending.



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