MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX839

Digitally Controlled Analog I/O Processor

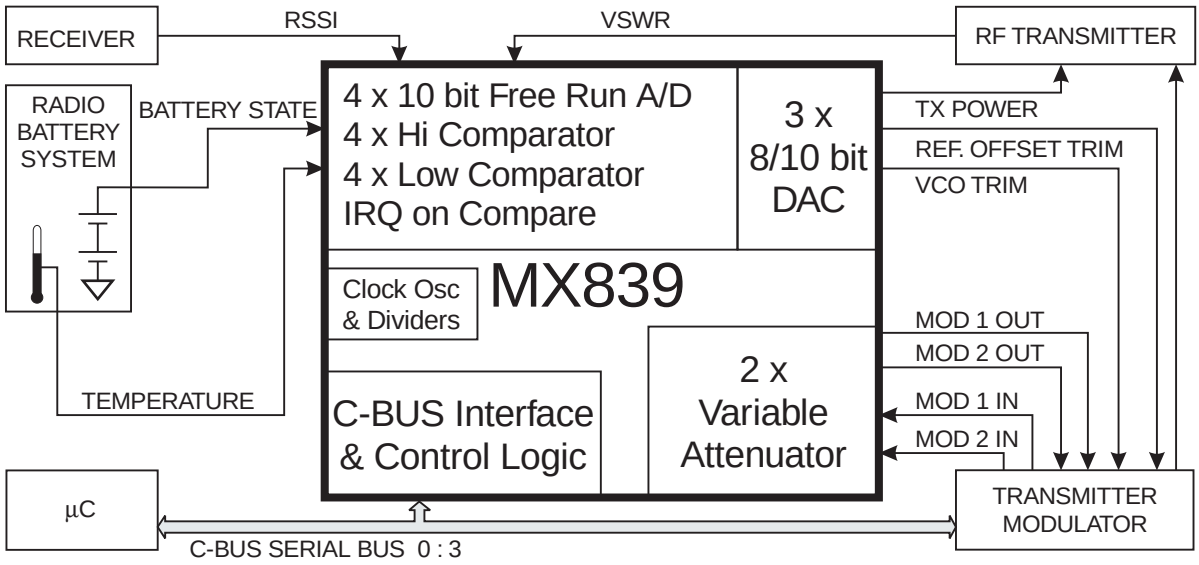
PRELIMINARY INFORMATION

Features

- **4 input intelligent 10 bit A/D monitoring subsystem**
  - **4 High and 4 Low Comparators**
  - **External IRQ Generator**
  - **Free Running Operation**
- **Three 8/10 bit DACs**
- **Two Variable Attenuators**
- **Selectable A/D Clock Frequencies**
- **Full Control via 4-wire Serial Interface**
- **Low Power 3.0 Operation**

Applications

- **PCS, Cellular, LMR, Wireless Transceivers, and General Purpose**
- **Monitor and Control:**
  - **RSSI, Battery State, Temperature, VSWR, and Error Voltages**
- **Digital Trim and Calibration:**
  - **VCOs, TCXO, Power Output, Bias, Current, IF Gain, Deviation, Modulation Depth, and Baseband Gain**



The MX839 is a low power CMOS µC peripheral device which provides digitally controlled calibration, trimming, and monitoring functions for PCS, cellular, LMR, wireless transceivers, and general purpose applications.

Featuring a four input intelligent 10 bit A/D monitoring subsystem, an interrupt generator, three 8/10 bit DACs, and two variable attenuator functions, the MX839 automatically monitors, produces, and trims up to nine analog signals via a simple four wire serial control bus. The free running A/D intelligent monitoring subsystem includes independent high and low limit comparators for each of four analog input signals which can be configured to generate external µC interrupts.

The MX839's high level of integration reduces end product parts count, component size, and software complexity. MX839 digital trimming functions also reduce manufacturing costs by eliminating manual trimming operations.

Featuring an operating range of 3.0V to 5.5V the MX839 is available in 24-pin SSOP (MX839DS), 24-pin SOIC (MX839DW), and 24-pin PDIP (MX839P) packages.

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1 Block Diagram

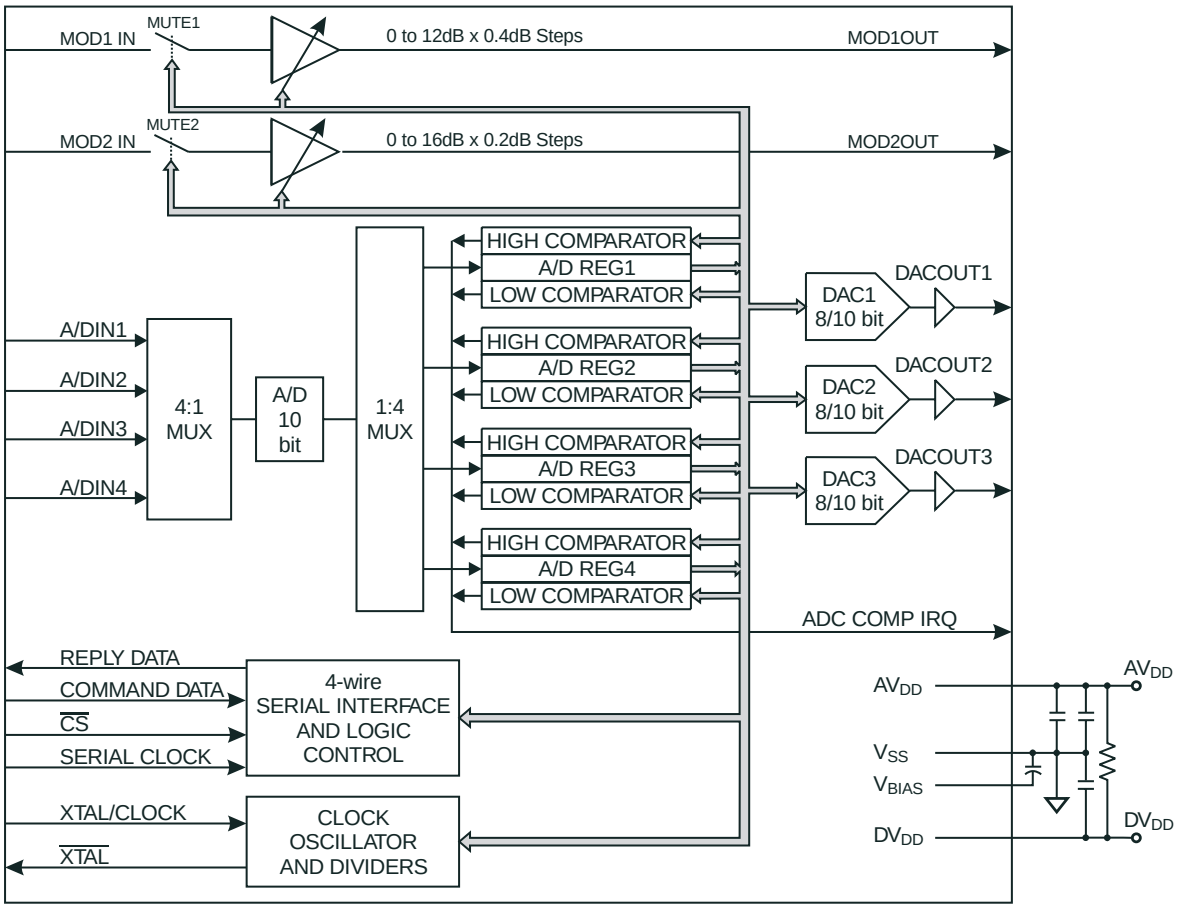

Figure 1: Block Diagram

2 Signal List

Pin No.	Name	Type	Description
1	$\overline{XTAL}$	output	The output of the on-chip oscillator inverter.
2	XTAL/CLOCK	input	The input to the on-chip oscillator inverter, for external Xtal circuit or clock.
3	SERIAL CLOCK	input	The 'C-BUS' serial clock input. This clock, produced by the µC, is used for transfer timing of commands and data to and from the device. See Figure 5.
4	COMMAND DATA	input	The 'C-BUS' serial data input from the µC. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the SERIAL CLOCK. See Figure 5.
5	REPLY DATA	output	The 'C-BUS' serial data output to the µC. The transmission of REPLY DATA bytes is synchronized to the SERIAL CLOCK under the control of the $\overline{CS}$ input. This tri-state output is held at high impedance when not sending data to the µC. See Figure 5.
6	$\overline{CS}$	input	The 'C-BUS' data loading control function. This input is provided by the µC. Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See Figure 5.
7	$\overline{IRQ}$	output	This output indicates an interrupt condition to the µC by going to a logic '0'. This is a 'wire-ORable' output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic '0' when active and a high-impedance when inactive. An external pullup resistor is required. The conditions that cause interrupts are indicated in the IRQ FLAG register and are effective if not disabled.
8	A/DIN1	input	Analog to digital converter input 1 (A/D1)
9	A/DIN2	input	Analog to digital converter input 2 (A/D2)
10	A/DIN3	input	Analog to digital converter input 3 (A/D3)
11	A/DIN4	input	Analog to digital converter input 4 (A/D4)
12	V_{SS}	power	Negative supply (ground) for both analog and digital supplies.
13	V_{BIAS}	output	An analog bias line for the internal circuitry, held at $AV_{DD}/2$. This pin must be bypassed by a capacitor mounted close to the device pins.
14	N/C		No internal connection. Do not make any connection to this pin.
15	DACOUT1	output	Digital to analog converter No. 1 output (DAC1)
16	DACOUT2	output	Digital to analog converter No. 2 output (DAC2)
17	DACOUT3	output	Digital to analog converter No. 3 output (DAC3)
18	N/C		No internal connection. Do not make any connection to this pin.
19	AV_{DD}	power	Positive analog supply. Analog levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.
20	MOD1 IN	input	Input to MOD1 variable attenuator.
21	MOD2 IN	input	Input to MOD2 variable attenuator.
22	MOD1	output	Output of MOD1 variable attenuator.
23	MOD2	output	Output of MOD2 variable attenuator.
24	DV_{DD}	power	Positive digital supply. Digital levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

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3 External Components

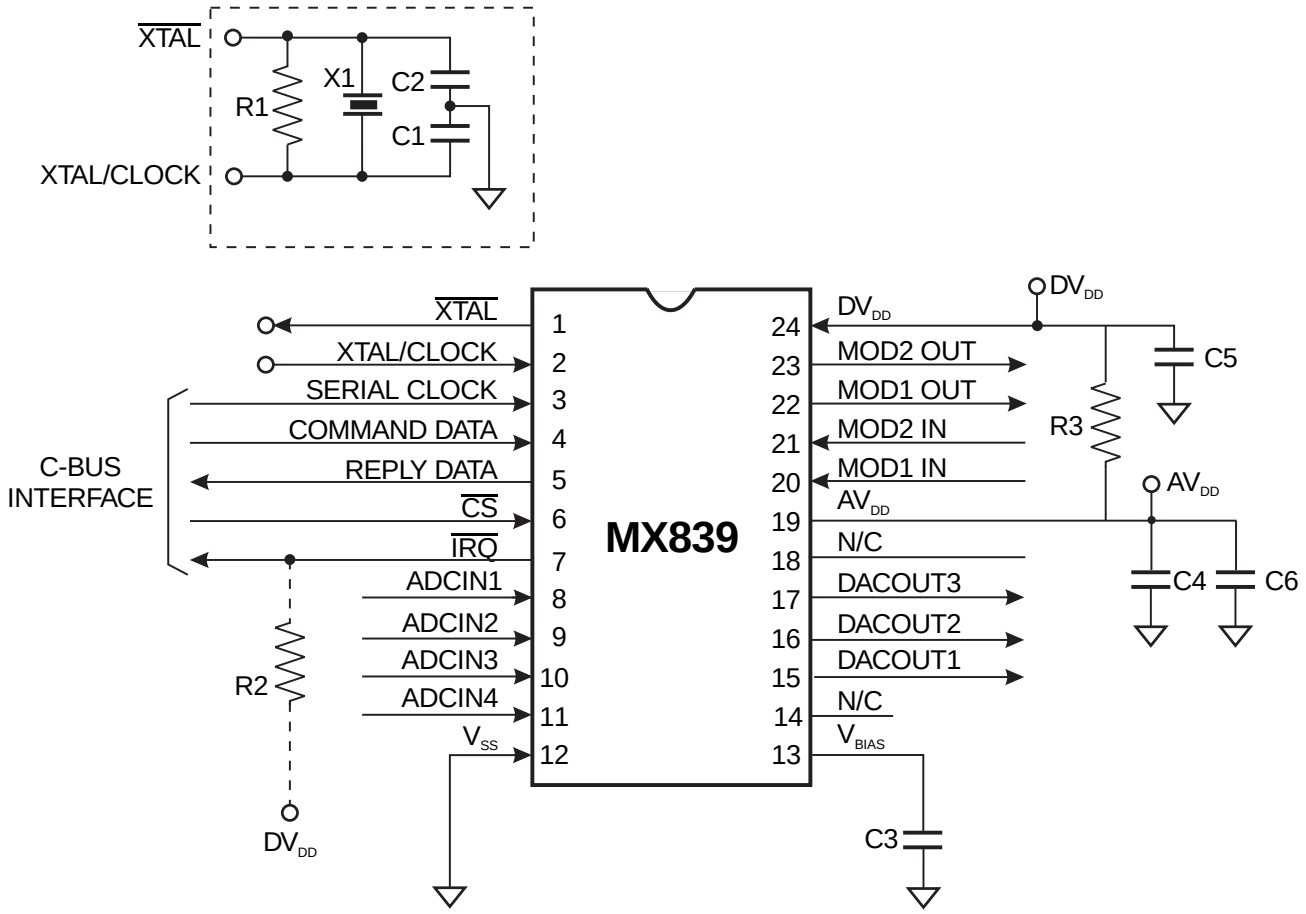

Figure 2: Recommended External Components

R1		1MΩ	±5%
R2		22kΩ	±10%
R3	Note 1	10Ω	±10%
C1		22pF	±20%
C2		22pF	±20%
C3		0.1µF	±20%

C4	Note 1	0.1µF	±20%
C5		0.1µF	±20%
C6	Note 1	10.0µF	±20%
X1	Note 2, 3		±100ppm

Table 1: Recommended External Components

Notes:

1. These values should be determined in regard to the amount of supply filtering required for D/A outputs.
2. If an external clock is to be used, then it should be connected to Pin 2 and the components C1, C2, R1, and X1 omitted. The ADC clock frequency is derived from the crystal or external clock by means of internal programmable dividers. See Section 6 for details of crystal or external clock frequency range.
3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

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4 General Description

The device comprises four groups of related functions: variable attenuators, digital to analog converters, a multiplexed analog to digital converter with multiplexer, clock generator and four 8-bit magnitude comparators with variable reference levels. These functions are all controlled by the 'C-BUS' serial interface and are described below:

4.1 Variable Attenuators

The two variable attenuators have a range of 0 to -12dB and 0 to -6dB respectively and may be controlled independently.

4.2 Digital to Analog Converters

Three DACs are provided with default resolutions of 8 bits, which are defined at the initial chip reset. In this mode the 'C-BUS' data is transferred in a single byte. An option is provided to define any one or more of the DAC resolutions to be 10 bits, then the DAC requires the transfer of two 'C-BUS' data bytes.

The upper and lower DAC reference voltages are defined internally as AV_{DD} and V_{SS} respectively. The output voltage is expressed as:

$$V_{OUT} = AV_{DD} \times (DATA / 2^n) \quad [Volts]$$

Where, n is the DAC resolution (8 or 10 bits) and DATA is the decimal value of the input code. For example: n = 8 and binary code = 11111111 therefore DATA = 255

$$V_{OUT} = AV_{DD} \times (255 / 256) \quad [Volts]$$

Any one of the three DAC input latches might be loaded by sending an address/command byte followed by one or two data bytes to the 'C-BUS' interface. The data is then latched and the static voltage is updated at the appropriate output.

When a DAC is disabled, its output is defined as open-circuit.

4.3 Analog to Digital Converter and A/D Clock Generator

A single successive approximation A/D is provided with four multiplexed inputs. After a general reset command $01, the A/D converter subsystem is disabled. To start conversions the Clock Control ($D0) and A/D control ($D7) registers must be written (refer to Tables 2,6, and 8). Please note that A/D channel 1 must be active for any other channel to work. Also note that A/D control register bit 5 ($\overline{READ}$) should be set low prior to issuing a 'READ A/D DATA x' command to disable conversions so the data being read does not change during the read which could otherwise result in erroneous data being read. To re-enable conversions the A/D control register bit 5 ($\overline{READ}$) bit must be set back high.

The internal A/D clock frequency (f_{A/D_CLK}) is generated with a programmable clock generator. Users have flexible control of this clock signal via the Clock Control Register ($D0), DIVIDER set per Table 6, and the choice of an external system clock signal or a dedicated crystal. f_{A/D_CLK} should be chosen not to exceed 1MHz.

Since the typical application is for monitoring slowly changing control voltages, a Sample and Hold circuit is not included at the input of the A/D. Thus, for the analog to digital conversion to be accurate, the input signal should not change significantly during the conversion time. For 'n-bit' accuracy (with a maximum error of 1LSB) the maximum signal 'linear rate of change,' 'S,' is defined by:

$$S = \frac{AV_{DD} \quad f_{A/D\_CLK}}{2^n \quad 1000 \quad (n+2)} \qquad [mV/\mu S]$$

where: n is the number of bits of accuracy with a maximum error of 1 LSB

where: $f_{A/D\_CLK} = \frac{f_{XTAL}}{DIVIDER}$, DIVIDER is selected per Table 6.

For Example: The most significant bits (n) of accuracy.

For (n = 6) bit accuracy with AV_{DD}=5V and f_{A/D_CLK} = 1MHz

S = 9.77 [mV/μS]

For (n = 8) bit accuracy with AV_{DD}=5V and f_{A/D_CLK} = 1MHz

S = 1.95 [mV/μS]

For (n = 10) bit accuracy with AV_{DD}=3.3V and f_{A/D_CLK} = 1MHz

S = 0.27 [mV/μS]

The input signal should therefore be band limited to ensure the maximum signal 'linear rate of change' is not exceeded for the desired accuracy.

After enabling conversions the user must allow time for all enabled channels to be digitized before reading the results via the 'C-BUS'. The minimum required time to wait is:

$$T_{CONV\_MAX} = \frac{(10 + 2) \quad \text{'Number of Enabled Inputs'}}{f_{A/D\_CLK}} \qquad \text{[Seconds]}$$

Upon disabling conversions the data for the most recent conversion completed for each channel will be available via the 'C-BUS' commands 'READ A/D DATA x' (addresses $DC, $DD, $DE, $DF) for input channels 1 through 4 respectively.

Do not forget to re-enable conversions by setting A/D control register bit 5, the $\overline{\text{READ}}$ bit, back high after reading the desired A/D results. Note that the Magnitude Comparators (see section 4.4) can be configured to monitor the A/D channel data in order to minimize the software burden of continuously reading the A/D channel data. It is not recommended to issue 'READ A/D DATA x' commands without first setting A/D control register bit 5, the $\overline{\text{READ}}$ bit, low.

An Example C-BUS transaction to do a conversion and read of A/D Channel 1:

HEX ADDRESS/ COMMAND	WRITE DATA BYTE 1	READ DATA BYTE 1	READ DATA BYTE 2	COMMENT
$01	N/A	N/A	N/A	Reset Device
$D0	$03	N/A	N/A	Set f_{A/D_CLK} DIVIDER = 4
$D7	$70	N/A	N/A	Enable conversion on A/D Channel 1
$D7	$50	N/A	N/A	Disable conversions after waiting T_{CONV_MAX}
$DC	N/A	xxxxxxxx	000000xx	Read A/D Channel 1 Data
$D7	$70	N/A	N/A	Re-enable conversion on A/D Channel 1

4.4 Magnitude Comparators and Interrupt Request

High and low digital comparator reference levels are provided for the four digital magnitude comparators via the 'C-BUS' interface. The digital input to the comparators is provided by the most significant 8 data bits of each A/D channel

When the sampled data falls outside the high or low digital comparator reference levels the status register is updated and the $\overline{\text{IRQ}}$ pin is pulled low. When a reference level is set to '0', its IRQ is disabled.

4.5 Software Description

4.5.1 Address/Commands

Instructions and Data are transferred via the 'C-BUS' in accordance with the timing information provided in Figure 5.

Instruction and data transactions to and from the FX839 consist of an Address/Command byte followed by either:

(i) a control or DAC data write (1 or 2 bytes) or,

(ii) a status or A/D data read (1 or 2 bytes)

4.5.2 Write Only Register (8-Bit and 16-Bit)

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	CLOCK						DIVIDER		
$D0	CONTROL	0	0	0	0	0	BIT 2	BIT 1	BIT 0
	VARIABLE			MOD1	MOD1				
$D2	ATTENUATOR (1)	0	0	ENABLE	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	VARIABLE			MOD2	MOD2				
	ATTENUATOR (2)	0	0	ENABLE	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DAC	NBIT	NBIT	NBIT		DAC1	DAC2	DAC3	
$D3	CONTROL	DAC1	DAC2	DAC3	0	ENABLE	ENABLE	ENABLE	0
	DAC1 DATA								
$D4	(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1								
	(2)	0	0	0	0	0	0	BIT 9	BIT 8
	DAC2 DATA								
$D5	(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1								
	(2)	0	0	0	0	0	0	BIT 9	BIT 8
	DAC3 DATA								
$D6	(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1								
	(2)	0	0	0	0	0	0	BIT 9	BIT 8
	A/D				A/DIN1	A/DIN2	A/DIN3	A/DIN4	
$D7	CONTROL	0	1	$\overline{\text{READ}}$	ACTIVE	ACTIVE	ACTIVE	ACTIVE	0
	MAG COMP ONE	MAGNITUDE COMPARATOR UPPER LEVEL							
$D8	LEVELS (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP ONE	MAGNITUDE COMPARATOR LOWER LEVEL							
	LEVELS (2)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP TWO	MAGNITUDE COMPARATOR UPPER LEVEL							
$D9	LEVELS (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP TWO	MAGNITUDE COMPARATOR LOWER LEVEL							
	LEVELS (2)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP THREE	MAGNITUDE COMPARATOR UPPER LEVEL							
$DA	LEVELS (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP THREE	MAGNITUDE COMPARATOR LOWER LEVEL							
	LEVELS (2)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP FOUR	MAGNITUDE COMPARATOR UPPER LEVEL							
$DB	LEVELS (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP FOUR	MAGNITUDE COMPARATOR LOWER LEVEL							
	LEVELS (2)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Table 2: Write Only Register (8-Bit and 16-Bit)

Note

1. A second byte is expected by the 'C-BUS' interface only when the 'NBIT DAC*n*' bit of the 'DAC Control Register' is set high. Otherwise, the data transfer is a single byte (Bit 7 to Bit 0).

4.6 Read Only Registers (8-Bit and 16-Bit)

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$D1	IRQ FLAGS	HIRQF 4	LIRQF 4	HIRQF 3	LIRQF 3	HIRQF 2	LIRQF 2	HIRQF 1	LIRQF 1
$DC	A/D DATA1 (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	(2)	0	0	0	0	0	0	BIT 9	BIT 8
$DD	A/D DATA2 (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	(2)	0	0	0	0	0	0	BIT 9	BIT 8
$DE	A/D DATA3 (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	(2)	0	0	0	0	0	0	BIT 9	BIT 8
$DF	A/D DATA4 (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	(2)	0	0	0	0	0	0	BIT 9	BIT 8

Table 3: Read Only Registers (8-Bit and 16-Bit)

4.7 Write Only Register Description

4.7.1 RESET Register (Hex Address $01)

The reset command has no data attached to it. It sets the device registers into the specific states listed below:

REGISTER NAME		BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
CLOCK CONTROL		0	0	0	0	0	0	0	0
DAC CONTROL		0	0	0	0	0	0	0	0
DAC1 DATA*1*		0	0	0	0	0	0	0	0
DAC2 DATA*1*		0	0	0	0	0	0	0	0
DAC3 DATA*1*		0	0	0	0	0	0	0	0
A/D CONTROL		0	0	0	0	0	0	0	0
VARIABLE ATTENUATOR	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0
MAG COMP ONE LEVELS	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0
MAG COMP TWO LEVELS	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0
MAG COMP THREE LEVELS	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0
MAG COMP FOUR LEVELS	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0

Table 4: RESET Register (Hex Address $01)

Note

1. Default resolution is defined as 8-Bits.

4.7.2 CLOCK CONTROL Register (Hex Address $D0)

This register controls the A/D clock divide ratio:

Bits 7 to 3	Reserved for future use. These bits should be set to '0'.
DIVIDER (Bit 2 - Bit 0)	The Xtal input clock divide ratio, which sets the A/D sample clock frequency, is defined in the following table.

Table 5: CLOCK CONTROL Register (Hex Address $D0)

Bit 2	Bit 1	Bit 0	Function
0	0	0	Powersave
0	0	1	÷1
0	1	0	÷2
0	1	1	÷4
1	0	0	÷8
1	0	1	÷16
1	1	0	÷32
1	1	1	÷64

Table 6: DIVIDER (Bit 2 - Bit 0)

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4.7.3 VARIABLE ATTENUATOR Register (Hex address $D2)

This is a 16-bit register. Byte (1) is sent first. Bits 0 - 5 of the first byte in this register are used to enable and set the attenuation of the Modulator 1 amplifier. Bits 0 - 5 of the second byte in this register are used to enable and set the attenuation of the Modulator 2 amplifier. See Table 7.

5	4	3	2	1	0	Mod. 1 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	12.0dB
1	0	0	0	1	0	11.6dB
1	0	0	0	1	1	11.2dB
1	0	0	1	0	0	10.8dB
1	0	0	1	0	1	10.4dB
1	0	0	1	1	0	10.0dB
1	0	0	1	1	1	9.6dB
1	0	1	0	0	0	9.2dB
1	0	1	0	0	1	8.8dB
1	0	1	0	1	0	8.4dB
1	0	1	0	1	1	8.0dB
1	0	1	1	0	0	7.6dB
1	0	1	1	0	1	7.2dB
1	0	1	1	1	0	6.8dB
1	0	1	1	1	1	6.4dB
1	1	0	0	0	0	6.0dB
1	1	0	0	0	1	5.6dB
1	1	0	0	1	0	5.2dB
1	1	0	0	1	1	4.8dB
1	1	0	1	0	0	4.4dB
1	1	0	1	0	1	4.0dB
1	1	0	1	1	0	3.6dB
1	1	0	1	1	1	3.2dB
1	1	1	0	0	0	2.8dB
1	1	1	0	0	1	2.4dB
1	1	1	0	1	0	2.0dB
1	1	1	0	1	1	1.6dB
1	1	1	1	0	0	1.2dB
1	1	1	1	0	1	0.8dB
1	1	1	1	1	0	0.4dB
1	1	1	1	1	1	0dB

5	4	3	2	1	0	Mod. 2 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	6.0dB
1	0	0	0	1	0	5.8dB
1	0	0	0	1	1	5.6dB
1	0	0	1	0	0	5.4dB
1	0	0	1	0	1	5.2dB
1	0	0	1	1	0	5.0dB
1	0	0	1	1	1	4.8dB
1	0	1	0	0	0	4.6dB
1	0	1	0	0	1	4.4dB
1	0	1	0	1	0	4.2dB
1	0	1	0	1	1	4.0dB
1	0	1	1	0	0	3.8dB
1	0	1	1	0	1	3.6dB
1	0	1	1	1	0	3.4dB
1	0	1	1	1	1	3.2dB
1	1	0	0	0	0	3.0dB
1	1	0	0	0	1	2.8dB
1	1	0	0	1	0	2.6dB
1	1	0	0	1	1	2.4dB
1	1	0	1	0	0	2.2dB
1	1	0	1	0	1	2.0dB
1	1	0	1	1	0	1.8dB
1	1	0	1	1	1	1.6dB
1	1	1	0	0	0	1.4dB
1	1	1	0	0	1	1.2dB
1	1	1	0	1	0	1.0dB
1	1	1	0	1	1	0.8dB
1	1	1	1	0	0	0.6dB
1	1	1	1	0	1	0.4dB
1	1	1	1	1	0	0.2dB
1	1	1	1	1	1	0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte)	When this bit is '1' the MOD1 attenuator is enabled. When this bit is '0' the MOD1 attenuator is disabled (i.e. powersaved).
MOD2 ENABLE (Bit 5, second byte)	When this bit is '1' the MOD2 attenuator is enabled. When this bit is '0' the MOD2 attenuator is disabled (i.e. powersaved).
(Bits 7 and 6, first and second bytes)	Reserved for future use. These should be set to '0'.

Table 7: VARIABLE ATTENUATOR Register (Hex address $D2)

4.7.4 DAC CONTROL Register (Hex address $D3)

This register controls the resolution and the number of enabled DAC outputs:

NBIT DAC1 (Bit 7) **NBIT DAC2 (Bit 6)** **NBIT DAC3 (Bit 5)**	These bits define the input resolutions for each of the four DACs. When 'NBIT DAC*n*' is '0' the resolution of DAC*n* is 8-Bits. When 'NBIT DAC*n* is '1' the resolution of DAC*n* is 10-Bits.
(Bit 4)	Reserved for future use. This bit should be set to '0'.
DAC1 ENABLE (Bit 3) **DAC2 ENABLE (Bit 2)** **DAC3 ENABLE (Bit 1)**	These bits allow any one or more of the three DACs to be powered up. When '0' the DAC*n* is powered down and the output is high impedance. When '1' the DAC is powered on and the output voltage is defined by the DAC Data Registers.
(Bit 0)	Reserved for future use. This bit should be set to '0'.

4.7.5 DAC1 DATA Register (Hex Address $D4)

4.7.6 DAC2 DATA Register (Hex Address $D5)

4.7.7 DAC3 DATA Register (Hex Address $D6)

The data in these three registers sets the analog voltage at the output of DAC1, DAC2 and DAC3. This data will consist of one or two bytes depending on the defined input resolution that is set by bits 7, 6 and 5 of the DAC Control Register. When operating with 10-bit resolution Bit 7 to Bit 2 of the DAC*n* DATA Register second data byte must be set to "0".

4.7.8 A/D CONTROL Register (Hex Address $D7)

This register sets which channels are active and enables conversion mode or read mode.

(Bit 7)	Reserved for future use. This bit should be set to '0'.
(Bit 6)	Reserved for future use. This bit should be set to '1'.
$\overline{\text{READ}}$ (Bit 5)	When this bit is set to '1' all active channels are continuously sampled and the latest converted data stored for each channel. When this bit is set to '0' all conversions are stopped so that they may be read.
A/D1 ACTIVE (Bit 4) **A/D2 ACTIVE (Bit 3)** **A/D3 ACTIVE (Bit 2)** **A/D4 ACTIVE (Bit 1)**	These bits allow any one or more of the four A/D input channels to be enabled. When '0' the A/DIN*n* input voltage is not converted. When '1' the A/DIN*n* input is defined as active and the input voltage is converted. A/D1 must be active for any other channel to be active.
(Bit 0)	Reserved for future use. This bit should be set to '0'.

Table 8: A/D CONTROL Register (Hex Address $D7)

4.7.9 MAG COMP ONE LEVELS (Hex Address $D8)

4.7.10 MAG COMP TWO LEVELS (Hex Address $D9)

4.7.11 MAG COMP THREE LEVELS (Hex Address $DA)

4.7.12 MAG COMP FOUR LEVELS (Hex Address $DB)

Each address controls the relevant numbered A/D magnitude comparator.

The first byte, transmitted with the most significant bit first, sets the magnitude comparator upper reference level and the second byte sets the magnitude comparator lower reference level.

When a reference level's value is set to '0' its IRQ is disabled.

In general, if a reference level's value is R (unsigned decimal value of data byte)

$$V_{REF} = AV_{DD} \times \frac{R}{256} \quad [\text{Volts}]$$

4.8 Read Only Register Description

4.8.1 IRQ FLAGS Register (Hex Address $D1)

HIRQF1 (Bit 1) **HIRQF2 (Bit 3)** **HIRQF3 (Bit 5)** **HIRQF4 (Bit 7)**	These bits are set if the relevant digital magnitude comparator input exceeds its upper reference level. These bits are reset to '0' immediately after reading the IRQ FLAGS register. When any of these bits are set, an interrupt will be generated if the relevant reference level is not zero.
LIRQF1 (Bit 0) **LIRQF2 (Bit 2)** **LIRQF3 (Bit 4)** **LIRQF4 (Bit 6)**	These bits are set if the relevant digital magnitude comparator input falls below its lower reference level. These bits are reset to '0' immediately after reading the IRQ FLAGS register. When any of these bits are set, an interrupt will be generated if the relevant reference level is not zero.

Table 9: IRQ FLAGS Register (Hex Address $D1)

4.8.2 A/D DATA1 Register (Hex Address $DC)

4.8.3 A/D DATA2 Register (Hex Address $DD)

4.8.4 A/D DATA3 Register (Hex Address $DE)

4.8.5 A/D DATA4 Register (Hex Address $DF)

This data will consist of two bytes each. Bit 7 to Bit 2 of the second data byte will be set to '0'. Bits 0-7 of the first byte are the lease significant 8 bits while Bits 0-1 of the second byte are the most significant 2 bits of the 10 bit conversion.

The analog input (V_{IN}) is converted to a 10-bit digital word (w) according to:

$$w = \frac{V_{IN}}{AV_{DD}} \times 1024$$

The bits of word (w) are returned in 2 bytes as follows:

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Return Byte 1	w_7	w_6	w_5	w_4	w_3	w_2	w_1	w_0
Return Byte 2	0	0	0	0	0	0	w_9	w_8

5 Application

5.1 C-Bus Clock

Although this is specified as a 500kHz clock for compatibility with other C-BUS devices, the MX839 C-BUS will operate over a much wider range. Users should ensure that the C-BUS clock is at least 4 times slower than the crystal or external clock on Pin 2 of the MX839.

6 Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS}) (either AV_{DD} or DV_{DD})		-0.3	7.0	V
Voltage on any pin to V_{SS}		-0.3	V_{DD} + 0.3	V
Current				
AV_{DD}		-30	30	mA
DV_{DD}		-30	30	mA
V_{SS}		-30	30	mA
Any other pin		-20	20	mA
AV_{DD} - DV_{DD}	Note 1, 2	-100	100	mV
DW / P Package				
Total Allowable Power Dissipation at T_{AMB} = 25°C			800	mW
Derating above 25°C			13	mW/°C above 25°C
Storage Temperature		-55	125	°C
Operating Temperature		-40	85	°C
DS Package				
Total Allowable Power Dissipation at T_{AMB} = 25°C			550	mW
Derating above 25°C			9	mW/°C above 25°C
Storage Temperature		-55	125	°C
Operating Temperature		-40	85	°C

Note:

1. It is recommended that AV_{DD} be connected to DV_{DD} through a filter.
2. It is also recommended that AV_{DD} and DV_{DD} Voltages be tightly AC coupled to V_{SS} with a capacitor.

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS}) (either AV_{DD} or DV_{DD})	3.0	5.5	V
Operating Temperature	-40	85	°C
Xtal Frequency	0.5	6.0	MHz

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6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
AV_{DD}= DV_{DD} = V_{DD} = 3.3V to 5.0V, T_{AMB} = 25°C

		Notes	Min.	Typ.	Max.	Units
DC Parameters						
Supply Voltage			3.0	5.0	5.5	V
Supply Difference (AV_{DD} - DV_{DD})			-100		100	mV
I_{DD}						
V_{DD} = 5V						
powersaved				250	400	µA
not powersaved				4.5	7.0	mA
V_{DD} = 3.3V						
powersaved				150	250	µA
not powersaved				2.5	4.0	mA
'C-BUS' Interface						
Input Logic '1'			70%			DV_{DD}
Input Logic '0'					30%	DV_{DD}
Input Leakage Current (Logic '1' and '0')			-1.0		1.0	µA
Input Capacitance					7.5	pF
Output Logic '1' (I_{OH} = 120µA)			90%			DV_{DD}
Output Logic '0' (I_{OL} = 360µA)					10%	DV_{DD}
DACs and Output Buffers (Guaranteed monotonic)						
Un-loaded Performance						
Resolution				8 or 10		Bits
Internal DAC Settling Time (to 0.5 lsb)					10.0	µs
Integral non-linearity	Figure 4	7				
8 Bit mode					3.0	LSBs
10 Bit mode					5.0	LSBs
Differential non-linearity	Figure 3	6				
8 Bit mode					1.0	LSBs
10 Bit mode					1.0	LSBs
Buffer Slew Rate (with 20pF load)					TBD	V/µs
Buffer Output Resistance					200	Ω
Zero Error (For 0000_{HEX} code input)			-20	0	20	mV
RMS Output Noise Voltage		1		10		µV
Loaded Performance		2				
Output voltage with 5kΩ resistive load to ground						
Digital code = $3FF_{HEX}$		3	4.79			V
Digital code = 200_{HEX}, 10 Bit		3		2.495		V
Digital code = 80_{HEX}, 8 Bit		3		2.495		V
Output voltage with 5kΩ resistive load to V_{DD}						
Digital code = 000_{HEX}		3			200	mV
Minimum Resistive Load		4	1.0			kΩ

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	Notes	Min.	Typ.	Max.	Units
A/Ds and Multiplexed Inputs (Guaranteed monotonic)					
Resolution			10		Bits
Input signal 'linear rate of change' For 1 Bit error V_{DD} = 3.3V, and f_{A/D_CLK} = 1MHz				0.27	mV/µs
Conversion Time f_{A/D_CLK} = 1MHz			12		µs
Integral non-linearity Figure 4	7			2.0	LSBs
Differential non-linearity Figure 3	6			1.0	
Zero error		-20		20	mV
A/D Clock Frequency (f_{A/D_CLK})			1.0	TBD	MHz
Input Capacitance			TBD		pF
Variable Attenuators					
Nominal Adjustment Range					
MOD1 Attenuator		0		12.0	dB
MOD2 Attenuator		0		6.0	dB
Attenuation Accuracy		-1.0		1.0	dB
Step Size					
MOD1		0.2	0.4	0.6	dB
MOD2		0.1	0.2	0.3	dB
Output Impedance	5		600		Ω
Bandwidth (-3dB)			100		kHz
Input Impedance			15		kΩ
Magnitude Comparators and Interrupt Request					
Resolution			8		Bits
Output Logic '0' at $\overline{IRQ}$ (I_{OL}= 360µA and pull-up resistor R2 = 22kΩ ± 10% to DV_{DD})				10%	DV_{DD}
'Off' State Leakage Current at $\overline{IRQ}$ $V_{OUT} = DV_{DD}$				10	µA
Xtal/Clock Input					
Frequency Range	8	0.5		6.0	MHz
'High' pulse width		40			ns
'Low' pulse width		40			ns
Input Impedance (at 100Hz)			10		MΩ
Gain (input = $1mV_{RMS}$ at 100Hz)			20		dB

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Operating Characteristics Notes:

1. Measured over a 0 to 30kHz Band.
2. The extremes of the DAC output range (when resistively loaded) is affected by the output impedance of the DAC buffer. Under these conditions, the output impedance can approach 200Ω. However; when the output is operating well within the supply; the output impedance will be significantly lower, thereby improving the loaded performance.
3. R_{LOAD} = 5kΩ AV_{DD} = 5.0V.
4. Loads less than 1kΩ will produce output distortion.
5. Small signal impedance, at AV_{DD} = 5V and T_{AMB} = 25°C.
6. Differential non-linearity is defined as the difference in width between adjacent code midpoints and the width of an ideal LSB, divided by the width of an ideal LSB. See Figure 3.
7. Integral non-linearity is defined as the width difference between an actual code midpoint and the line of best fit through all code midpoints, divided by the width of an ideal LSB. See Figure 4.
8. 6MHz operation at V_{DD} = 5.0V only. The 'C-BUS' clock must be at lest 4 times slower than the XTAL/CLOCK frequency.

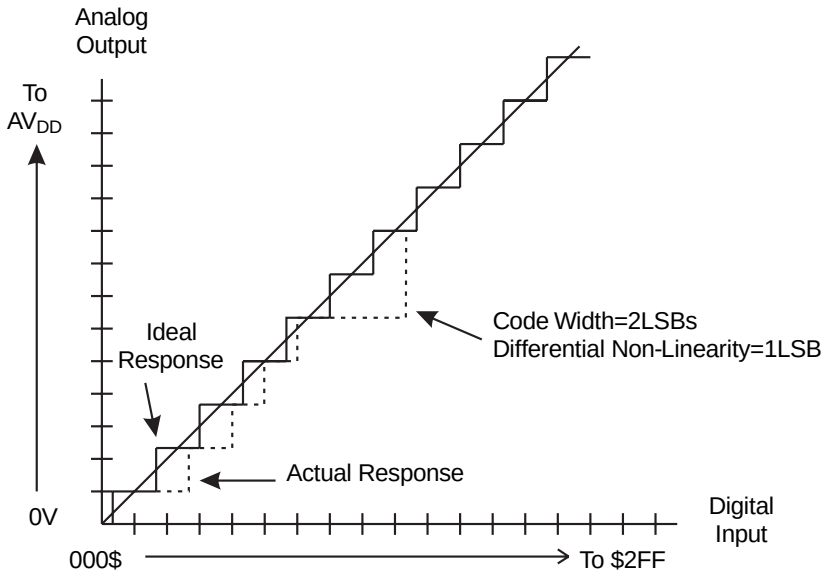


Figure 3: Differential Non-Linearity of a D/A Converter

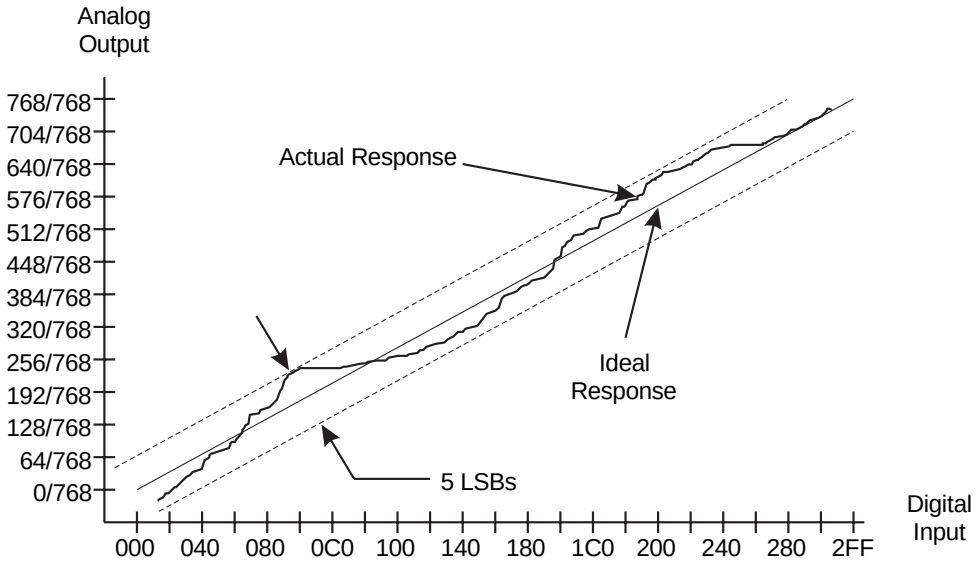


Figure 4: Integral Non-Linearity of a D/A Converter

6.1.4 Timing

For the following conditions unless otherwise specified:

DV_{DD} = 3.3V to 5.0V, T_{AMB} = 25°C

	Parameter	Min.	Typ.	Max.	Units
t_{CSE}	"CS-Enable to Clock-High"	2.0			µs
t_{CSH}	Last "Clock-High to CS-High"	4.0			µs
t_{HIZ}	"CS-High to Reply Output 3-state"			2.0	µs
t_{CSOFF}	"CS-High" Time between transactions	2.0			µs
t_{NXT}	"Inter-Byte" Time	4.0			µs
t_{CK}	"Clock-Cycle" time	2.0			µs

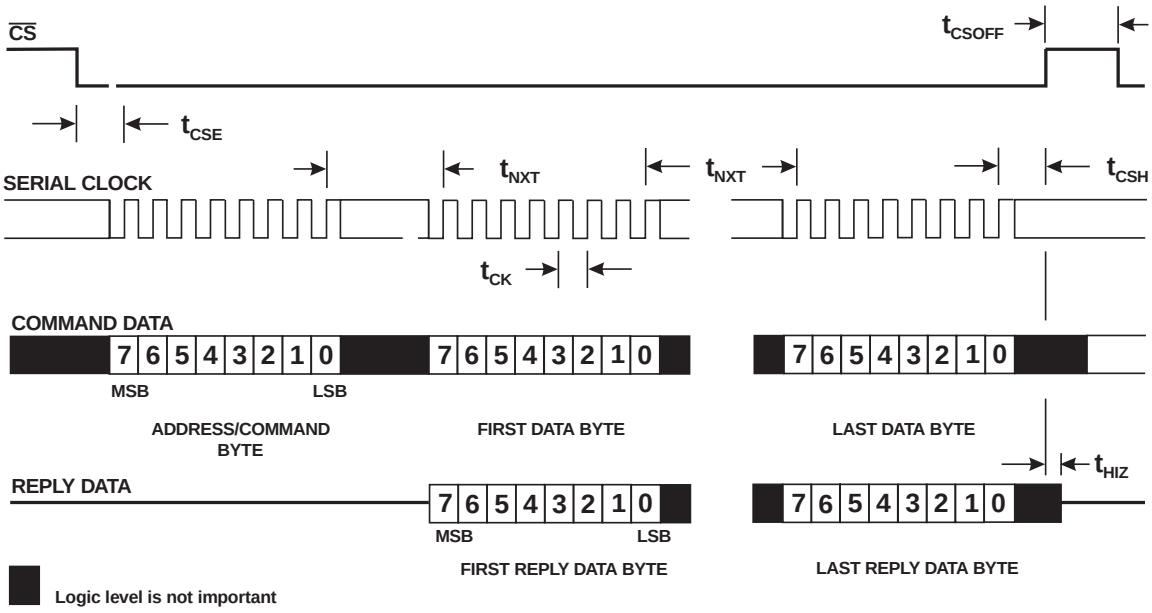
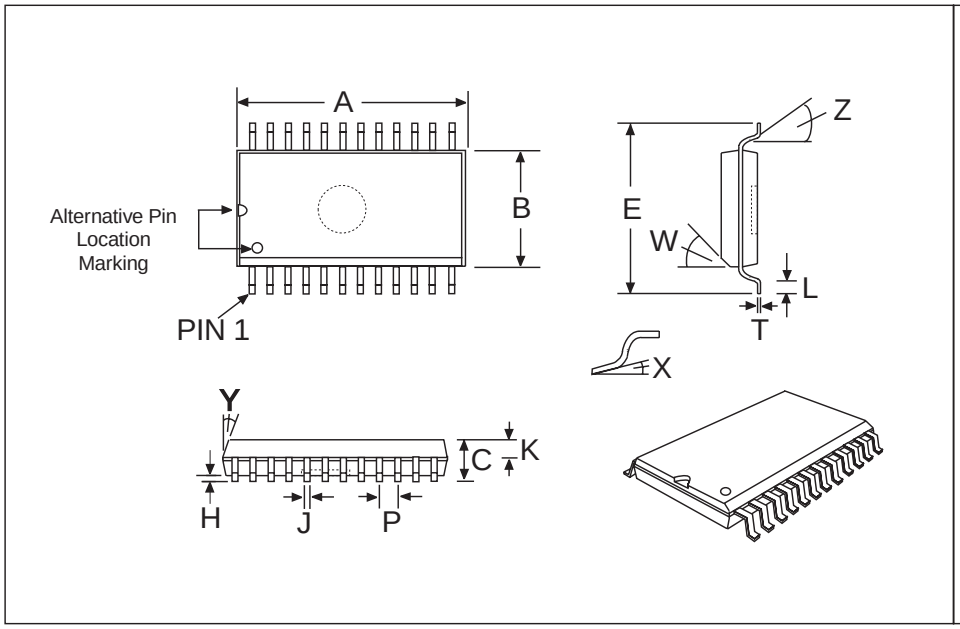


Figure 5: 'C-BUS' Timing

Timing Notes:

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µC serial interface formats 'C-BUS' compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

6.2 Packaging

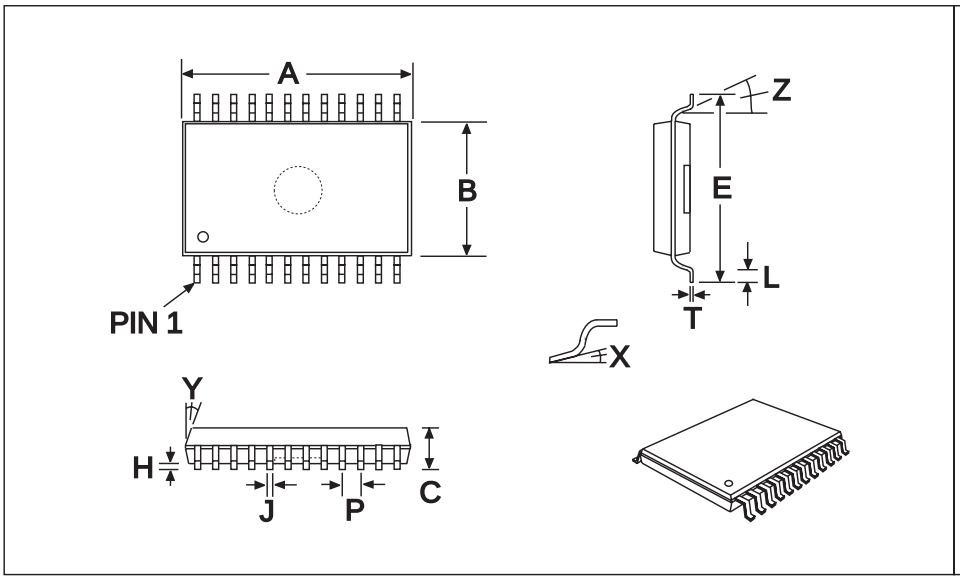


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin SOIC Mechanical Outline: *Order as part no. MX839DW*

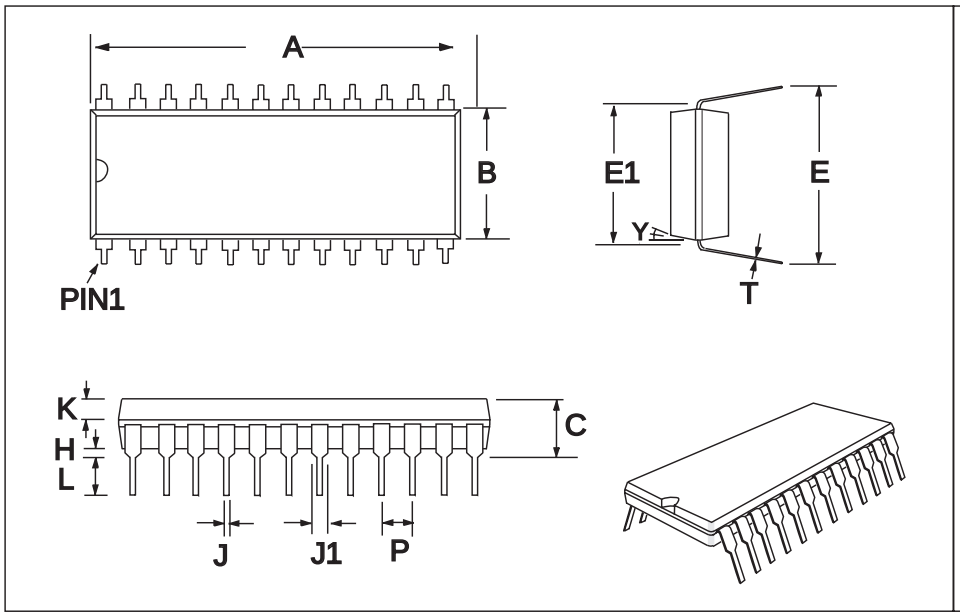


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 24-pin SSOP Mechanical Outline: *Order as part no. MX839DS*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin PDIP Mechanical Outline: *Order as part no. MX839P*