OKI Semiconductor

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MSM7581

ITU-T G.721 4ch ADPCM TRANSCODER

GENERAL DESCRIPTION

The MSM7581 is an ADPCM transcoder which is used by the new digital cordless system. It converts 64 kbps voice PCM serial data to 32 kbps ITU-T G.721 ADPCM serial data, and vice versa.

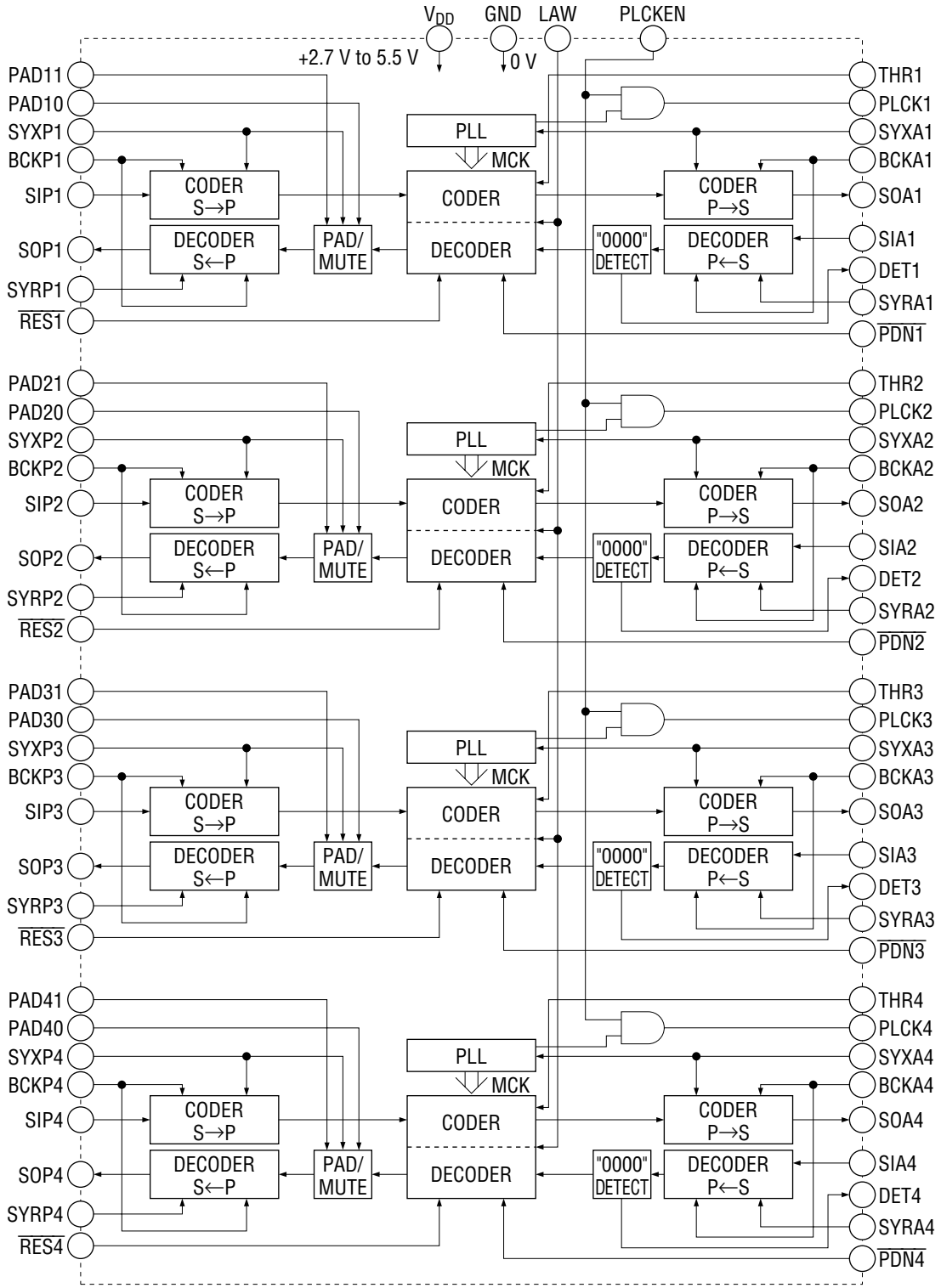
This device is consists of four systems with full-duplex voice data channels and a data-through mode.

The MSM7581 provides cost effective solutions for digital cordless office telephone systems which are incorporated into PABXs, and for the public base stations which are connected to the Central Office through digital PSTNs.

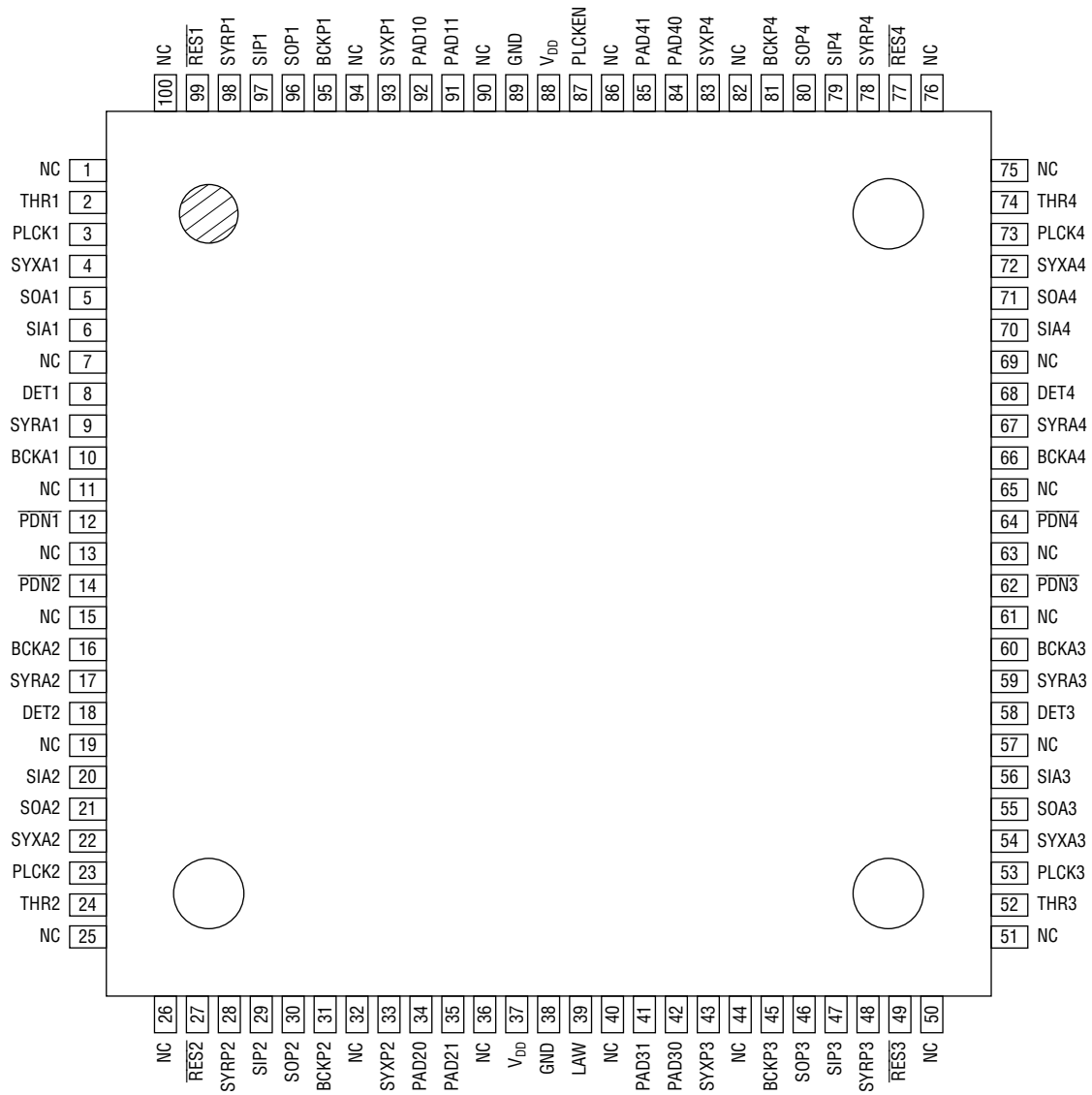
FEATURES

- Conforms to ITU-T G.721
- Built-in Full-duplex Transcoder with Four Data Channels
- PCM companding Law: A-law/μ-law selectable
- Serial PCM Data Transmission Speed: 64 kbps to 2048 kbps
- Serial ADPCM Data Transmission Speed: 32 kbps to 2048 kbps
- Hardware Reset – ITU-T G.721 Optional Reset – for each channel
- Power Down Control for each channel
- Decoder (ADPCM → PCM) Mute Mode and PAD Mode for each channel
- ADPCM Data-through Mode
- Capable of time slot conversion
- Special ADPCM Input Data Code (”0000”) Detector for each channel
- Master Clock Signal : Not necessary
- Power supply voltage/Consumption current :
  +2.7 V to +5.5 V, 2 mA/channel (max)
- Package :
  100-pin plastic TQFP (TQFP100-P-1414-0.50-K) (Product name : MSM7581TS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No connect pin

100-Pin Plastic TQFP

PIN AND FUNCTIONAL DESCRIPTIONS

GND

Ground, 0 V.

SIP1, SOP1

PCM serial data input (SIP1) and output (SOP1) for Channel 1.
SOP1 is an open-drain output, which goes into a high impedance state after a continuous 8-bit serial data output.

SIP2, SOP2

PCM serial data input (SIP2) and output (SOP2) for Channel 2.
SOP2 is an open-drain output, which goes into a high impedance state after a continuous 8-bit serial data output.

SIP3, SOP3

PCM serial data input (SIP3) and output (SOP3) for Channel 3.
SOP3 is an open-drain output, which goes into a high impedance state after a continuous 8-bit serial data output.

SIP4, SOP4

PCM serial data input (SIP4) and output (SOP4) Channel 4.
SOP4 is an open-drain output, which goes into a high impedance state after a continuous 8-bit serial data output.

PAD10 - PAD40, PAD11 - PAD41

PAD mode control.
The PCM output can be attenuated by 12 dB or 6 dB and set to an out-of-service pattern (idle pattern) by controlling these pins. Set these pins to digital "0" level during normal operation.The control sequences are as follows:

PAD11 - PAD41	PAD10 - PAD40	
0	0	Normal
0	1	6 dB Loss
1	0	12 dB Loss
1	1	Out-of-service Pattern

THR1, THR2, THR3, THR4

Control pins for the data-through modes.
THR (1 - 4) are for Channel (1 - 4), respectively. The data-through mode is selected when digital "1" is applied to THR (1 - 4). In this mode, 8-bit serial input data applied to SIA (1 - 4) (ADPCM data input) is passed to the PCM serial data output pins, SOP (1 - 4), without any data modification. SOP (1 - 4) go to the high impedance state after the output of 8-bit data has been applied to SIA (1 - 4).
Conversely 8-bit serial input data applied to SIP (1 - 4) (PCM data input) is passed to ADPCM serial data output pins, SOA (1 - 4), without any data modification.
SOA (1 - 4) go to the high impedance state after the output of 8-bit serial data has been applied to SIP (1 - 4).
ADPCM and PCM data interfaces have the mutually independent signal input pins for synchronizing signals. The time slots for data input and output can be exchanged between them. Some timing at which data may be deleted or duplicated as described in "Note on Usage" should not be used.

SYXP1 - 4, SYRP1 - 4

Synchronous signal input pins to define PCM data input and output timing for Channel 1 (SIP1, SOP1), Channel 2 (SIP2, SOP2), Channnel 3 (SIP3, SOP3), and Channel 4 (SIP4, SOP4).
The synchronous signals SYXA1 and SYRAI (Channel 1), SYXA2 and SYRA2 (Channel 2), SYXA3 and SYRA3 (Channel 3), and SYXA4 and SYRA4 (Channel 4), which define ADPCM data input and output timing are provided.
PCM and ADPCM data interfaces can be used at a mutually independent timing except some timing.
Note: When PCM and ADPCM data interfaces are used at a mutually independent timing, the timing described in "Note on Usage" should not be used.
SYXP signals must be input for PAD signal input processing.

BCKP1 - 4

Bit clock input.
These signals define the PCM data transmission speed at the PCM data input/output terminals. BCKP (1 - 4) are used for Channel (1 - 4). Since BCKA (1 - 4) defines the data rate of the ADPCM data interface, the PCM and ADPCM data can be input or output at different speeds.

LAW

PCM data companding law selection.
Digital "1" and "0" correspond to A-law and μ-law, respectively.

$\overline{\text{PDN1}}$, $\overline{\text{PDN2}}$, $\overline{\text{PDN3}}$, $\overline{\text{PDN4}}$

Power down mode selection.
$\overline{\text{PDN1 - 4}}$ can be independently set to power down mode. When digital "0" is applied, these pins are in the power-down mode.

SIA1, SOA1

ADPCM serial data input (SIA1) and output (SOA1) pins for Channel 1.
SOA1 is an open-drain pin and enters to the high impedance state after outputting a continuous 4-bit serial data stream. When the data-through mode is selected, SOA1 enters to the high impedance state after outputting an 8-bit serial data stream.

SIA2, SOA2

ADPCM serial data input (SIA2) and output (SOA2) pins for Channel 2.
These pins function the same as SIA1 and SOA1.

SIA3, SOA3

ADPCM serial data input (SIA3) and output (SOA3) pins for Channel 3.
These pins function the same as SIA1 and SOA1.

SIA4, SOA4

ADPCM serial data input (SIA4) and output (SOA4) pins for Channel 4.
These pins function the same as SIA1 and SOA1.

SYXA1 - 4 , SYRA1 - 4

SYXA1, SYXA2, SYXA3, and SYXA4 are synchronous signal input pins to define ADPCM data input and output timings for Channel 1 (SIA1, SOA1), Channel 2 (SIA2, SOA2), Channel 3 (SIA3, SOA3), and Channel 4 (SIA4, SOA4), respectively.
Therefore, PCM data interfaces can be used at a mutually independent timing except some timing.
Since master clocks are generated by the internal PLL using SYXA1 to SYXA4, a synchronous signal should be input to these pins.
Note: When PCM and ADPCM data interfaces are used at a mutually independent timing, the timing described in "Note on Usage" should not be used.

DET1, DET2, DET3, DET4

Special ADPCM input data pattern detect pins.
When detecting a 4-bit continuous "0" pattern at the ADPCM input pins Channel 1 (SIA1), Channel 2 (SIA2), Channel 3 (SIA3), and Channel 4 (SIA4), DET (1 - 4) goes from a digital "0" to a digital "1" state.
A digital "1" is output at the rising edge of the clock. The fourth data bit (LSB) is clocked into the register by the bit clock (BCKA 1 - 4) and held there until the rising edge in the next time frame.
When detecting the special data pattern in the next time frame, the digital "1" on the pins DET (1 - 4) is remains.

$\overline{RES1}$, $\overline{RES2}$, $\overline{RES3}$, $\overline{RES4}$

Algorithm reset signal input pins for each Channel (1 - 4) .
When digital “0” is applied, the entire transcoder goes to the initial state.
This reset is defined by ITU-T G.721 and is an optional reset.
The reset width (during "L") should be 125 µs or more.

BCKA1 - 4

Bit clock input pins used to define the data transmission speed at the ADPCM interface.
Using these pins, the ADPCM data interface can be defined at a speed other than the PCM data interface.

V_{DD}

Power supply.
The device must operate between +2.7 V and +5.5 V.

PLCKEN

Input pin which enables the output of an 8 kHz clock from the PLLs.
This pin generates the internal master clocks. The 8 kHz clocks from the internal PLLs synchronized with external signals applied to SYXA 1 - 4 are output to PLCK 1 - 4.
Set this pin at digital "0" during normal operation since it is used as the control pin for testing the IC.

PLCK1 - 4

Output pins of the 8 kHz clock from PLLs.
When PLCKEN = "1", the 8 kHz clock pulses synchronized with external signals are applied to SYXA1 - 4 outputs. When PLCKEN = "0", "0" level is output to these pins.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	0 to 7	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	2.7	—	5.5	V
Operating Temperature	Ta	—	–30	+25	+80	°C
Digital Input High Voltage	V_{IH}	All digital input pins	0.45 × V_{DD}	—	V_{DD}	V
Digital Input Low Voltage	V_{IL}		0	—	0.16 × V_{DD}	V
Bit Clock Frequency	F_{BCLKA}	BCKA1 - 4	32	—	2048	kHz
	F_{BCLKP}	BCKP1 - 4	64	—	2048	kHz
Synchronous signal Frequency	F_{SYNC}	SYXP1 - 4, SYRP1 - 4 SYXA1 - 4, SYRA1 - 4	—	8.0	—	kHz
Clock Duty Ratio	D_C	BCKA1 - 4, BCKP1 - 4	30	50	70	%
Digital Input Rise Time	t_{Ir}	All Digital Input Pins	—	—	50	ns
Digital Input Fall Time	t_{If}		—	—	50	ns
Synchronous signal Timing CODER	t_{XS}	BCKP1 - 4 to SYXP1 - 4	100	—	—	ns
	t_{SX}	SYXA1 - 4 to BCKA1 - 4	100	—	—	ns
Synchronous signal Timing DECODER	t_{RS}	BCKA1 - 4 to SYRA1 - 4	100	—	—	ns
	t_{SR}	SYRP1 - 4 to BCKP1 - 4	100	—	—	ns
Synchronous signal Width	t_{WS}	SYXP1 - 4, SYRP1 - 4 SYXA1 - 4, SYRA1 - 4	1 BCLK	—	100	µs
Data Set-up Time	t_{DS}	—	100	—	—	ns
Data Hold Time	t_{DH}	—	100	—	—	ns
Digital Output Load	R_{DL}	SOP1 - 4, SOA1 - 4 (Pull-up Resistor)	500	—	—	Ω
	C_{DL}	SOP1 - 4, SOA1 - 4 DET1 - 4, PLCK1 - 4	—	—	100	pF

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 V to 5.5 V, Ta = –30°C to +80°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Power On Mode: 4 Channels	—	5	8	mA
	I_{DD2}	Power Down Mode: 4 Channels	—	10	50	µA
Digital Input High Voltage	V_{IH}	All Digital Input Pins	$0.45 \times V_{DD}$	—	V_{DD}	V
Digital Input Low Voltage	V_{IL}	All Digital Input Pins	0.0	—	$0.16 \times V_{DD}$	V
Input Leakage Current	I_{IH}	$V_I = V_{DD}$	—	—	2.0	µA
	I_{IL}	V_I = 0 V	—	—	0.5	µA
Digital Output High Voltage	V_{OH}	DET1 - 4, PLCK1 - 4 : I_{OH} = –0.4 mA	$0.5 \times V_{DD}$	—	V_{DD}	V
Digital Output Low Voltage	V_{OL1}	SOA1 - 4, SOP1 - 4, Pull-up ≥ 500 Ω	0.0	0.2	0.4	V
	V_{OL2}	DET1 - 4, PLCK1 - 4 : I_{OL} = 2 mA	0.0	0.2	0.4	V
Output Leakage Current	I_{OL}	SOP1 - 4, SOA1 - 4	—	—	10	µA
Input Capacitance	C_{IN}	All Digital Input Pins	—	5	—	pF

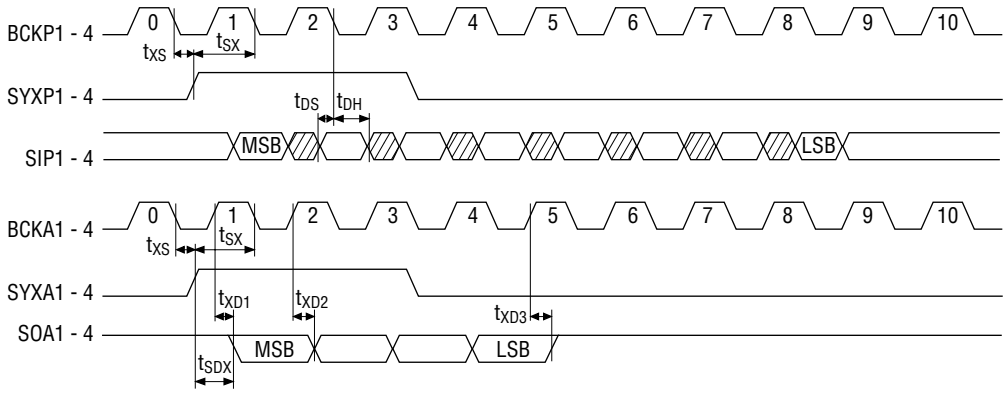
AC Characteristics

(V_{DD} = 2.7 V to 5.5 V, Ta = –30°C to +80°C)

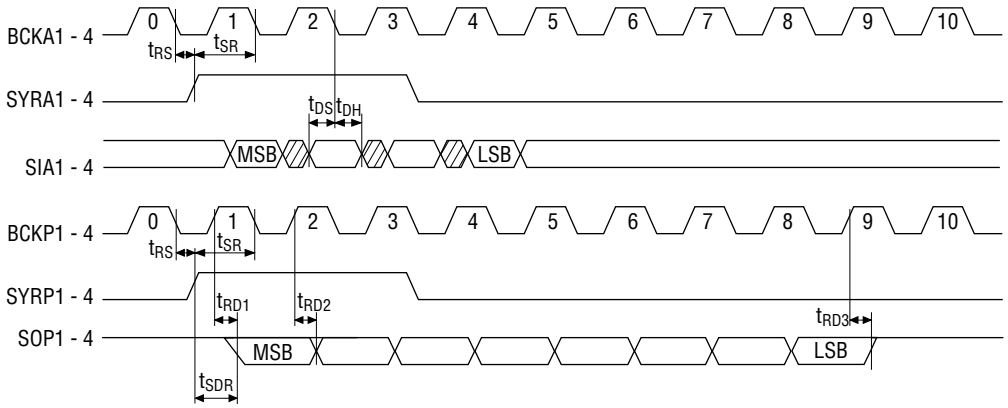
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital Output Delay Time	t_{SDX}	1 LSTTL + 100 pF Pull-up: 500 Ω	0	—	200	ns
	t_{SDR}		0	—	200	ns
	t_{XD1}, t_{RD1}		0	—	200	ns
	t_{XD2}, t_{RD2}		0	—	200	ns
	t_{XD3}, t_{RD3}		0	—	200	ns
	t_{DD1}		0	—	200	ns
	t_{DD2}		0	—	200	ns

TIMING DIAGRAM

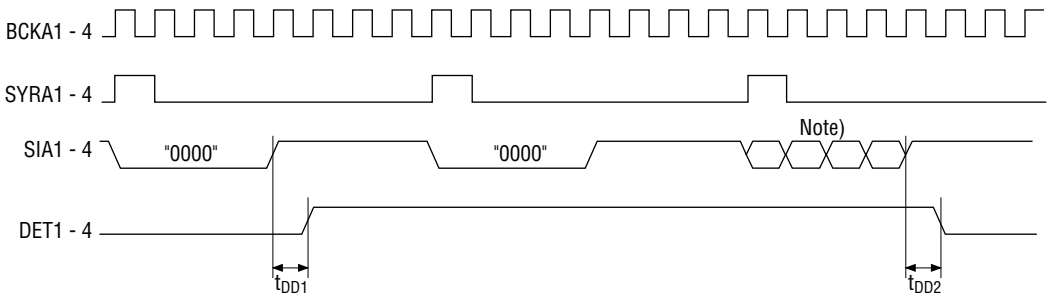
CODER



DECODER

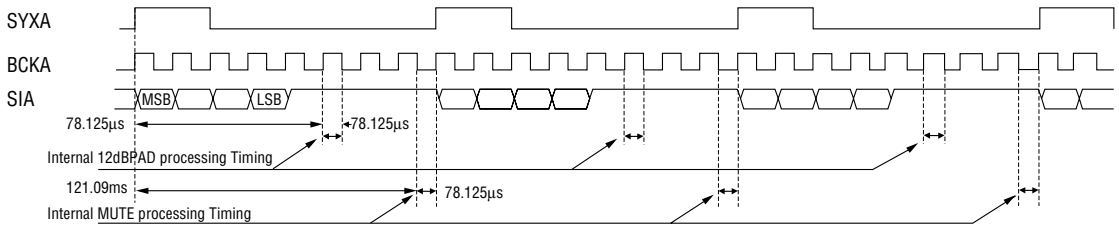


DET ("0000" detection) Output Timing

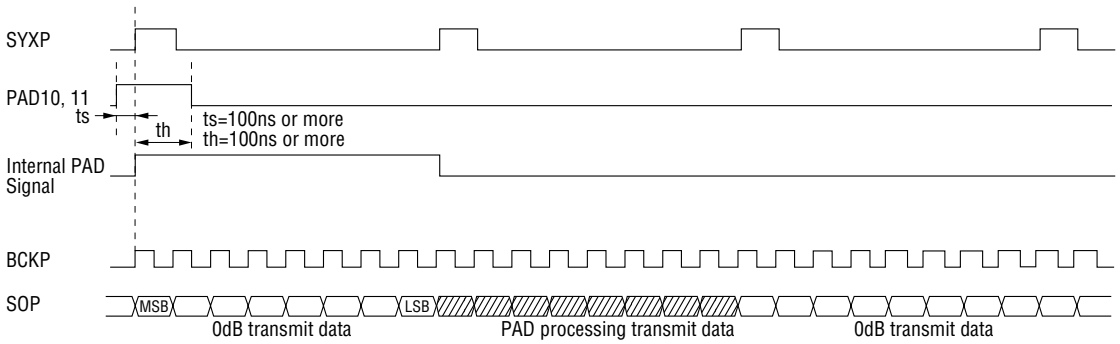


Note: 4 bit data pattern except "0000"

PAD Processing Timing



PAD10 to PAD40, PAD11 to PAD41 Timings

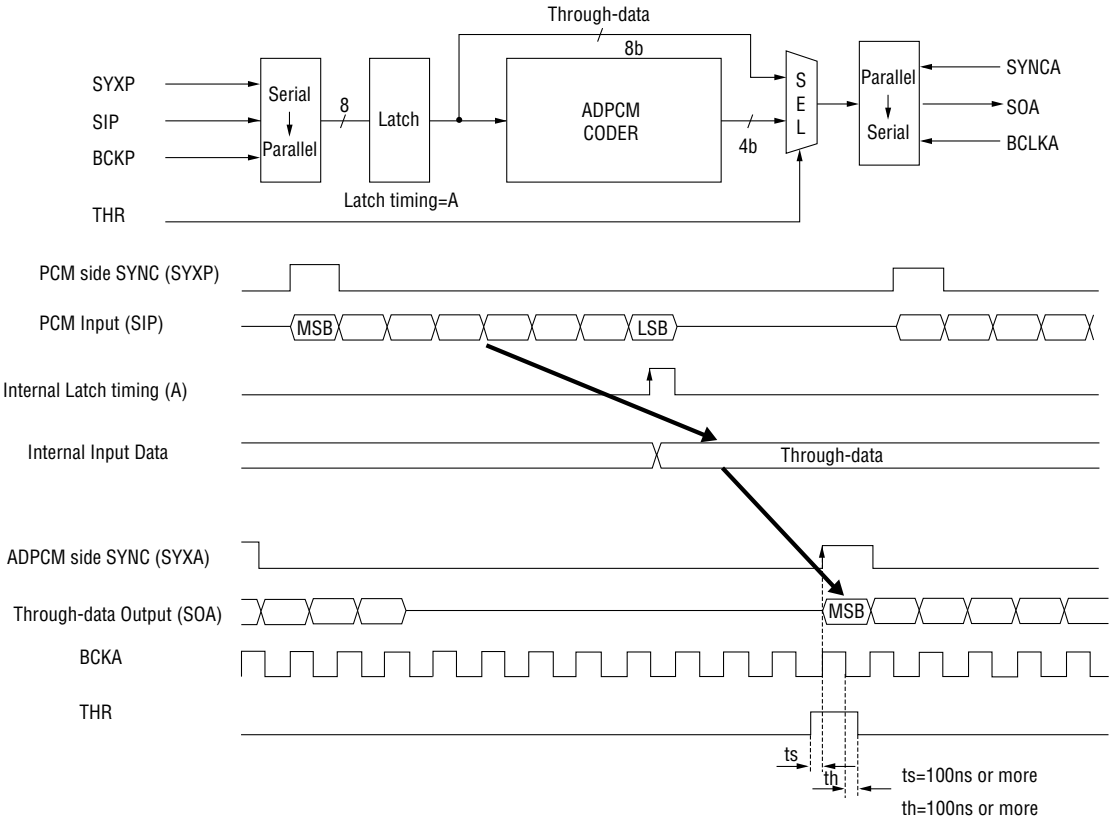


As mentioned above, PAD and MUTE processings are performed according to the rising edge of SYXA. Even if BLOCK is not 128 kHz, these processings are performed in the absolute time counted from the rising edge of SYXA.
The PAD pin must be controlled so as to cover these processings.
The PAD signal is input in the device at the rising edge of SYXP. Therefore, the PAD signal should be input at ts and th for the rise of SYXP.

THR Processing Timing

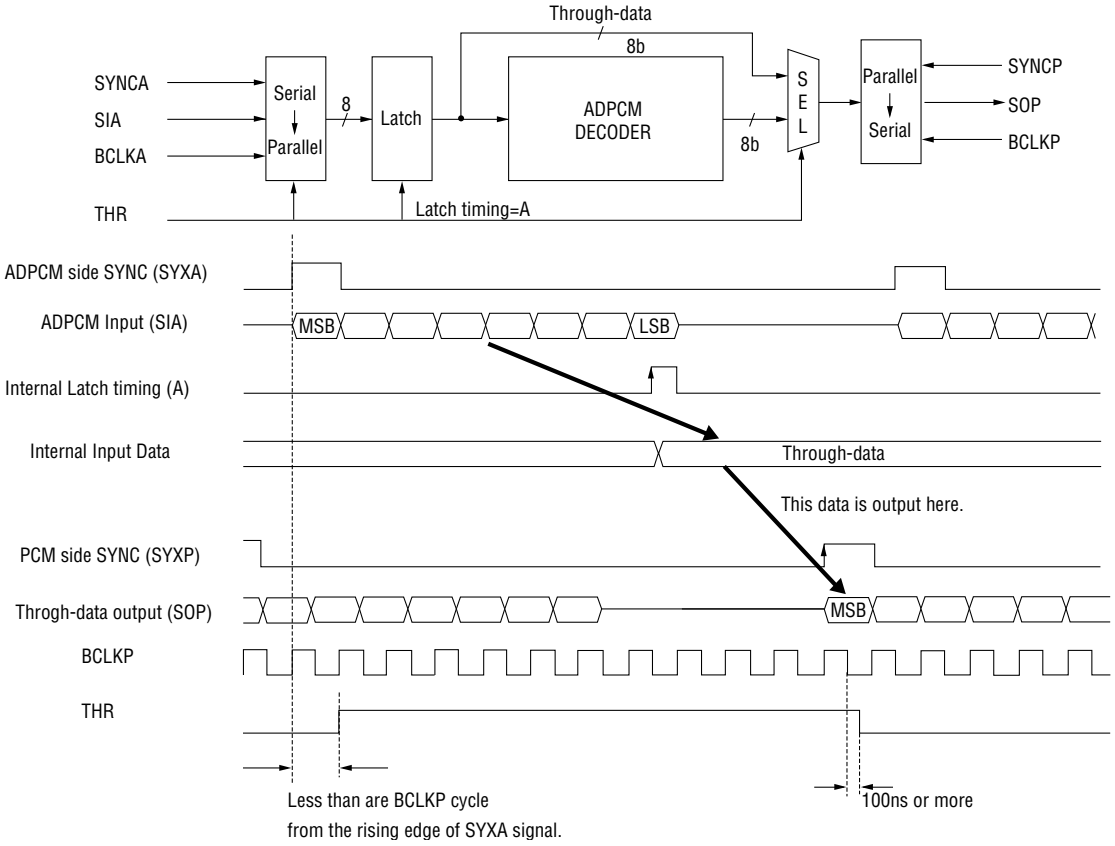
Timing Block Diagrams, when CODER and DECODER output data, are shown in the following figures.
The parallel to serial conversion of the output unit employs a load format and the load point is at the rising edge of a synchronous signal.
Therefore, input THR signal with respect to SYXA for CODER with timing of satisfying ts and th conditions shown in the figure.
For DECODER, THR signal should be input even of through-data is input.
The input timing should satisfy the conditions shown in the following figures.

CODER

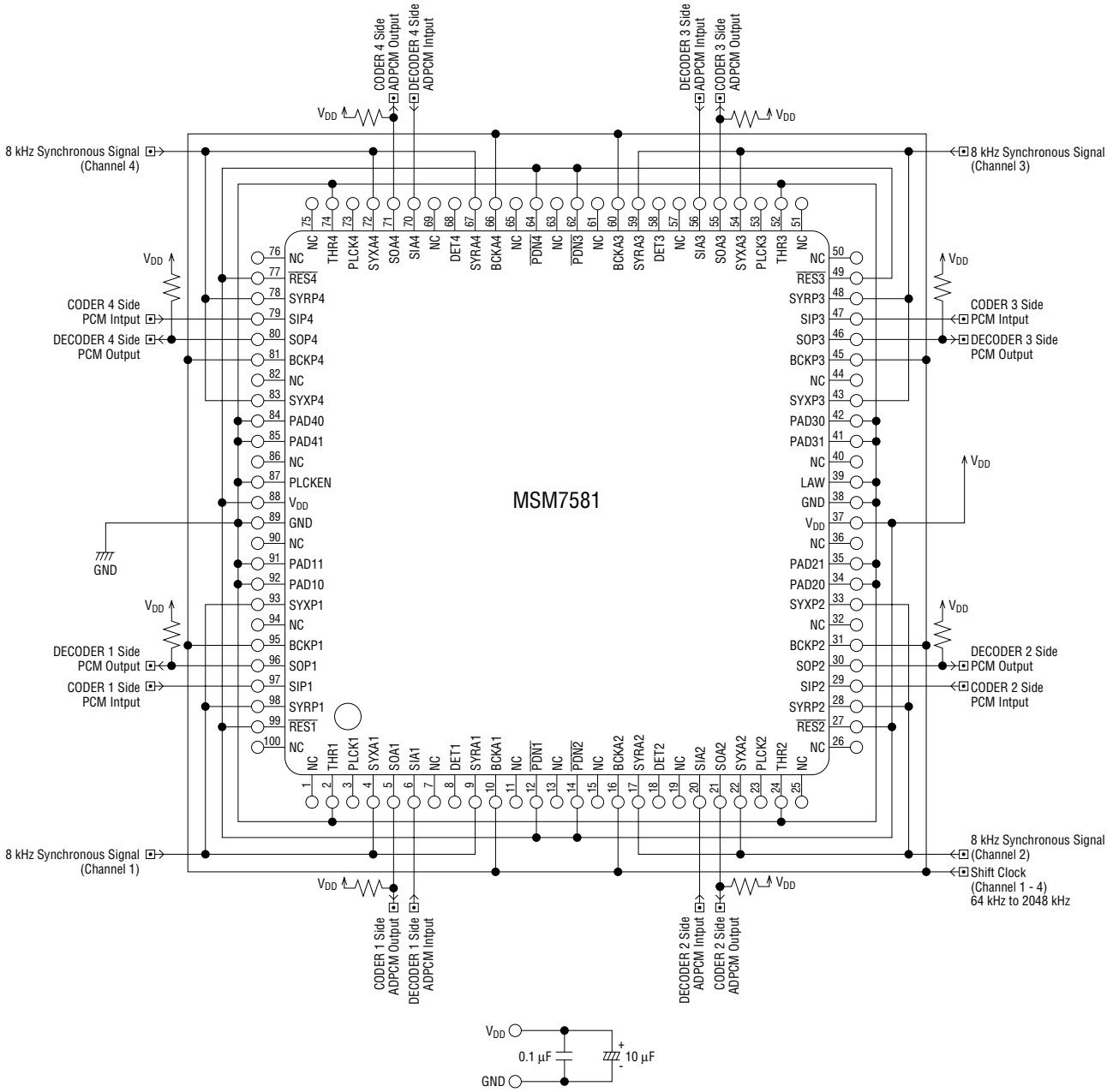


Note: That data-ship may occur when the rising edge (data load point) of SYXA and input of the internal latch timing overlap each other.

DECODER

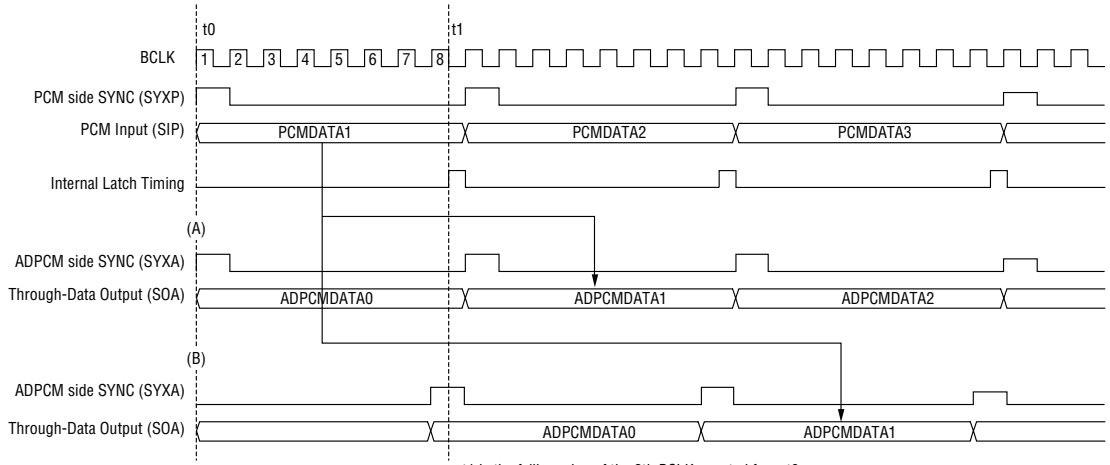

Through-data
8b
SYNCA
SIA
BCLKA
Serial
Parallel
8
Latch
ADPCM
DECODER
8b
S
E
L
Parallel
Serial
SYNCP
SOP
BCLKP
THR
Latch timing=A
ADPCM side SYNC (SYXA)
ADPCM Input (SIA)
MSB
LSB
Internal Latch timing (A)
Internal Input Data
Through-data
This data is output here.
PCM side SYNC (SYXP)
Throgh-data output (SOP)
MSB
BCLKP
THR
Less than are BCLKP cycle
from the rising edge of SYXA signal.
100ns or more

APPLICATION CIRCUIT



NOTES ON USAGE

(1) Through Mode (CODER Side)

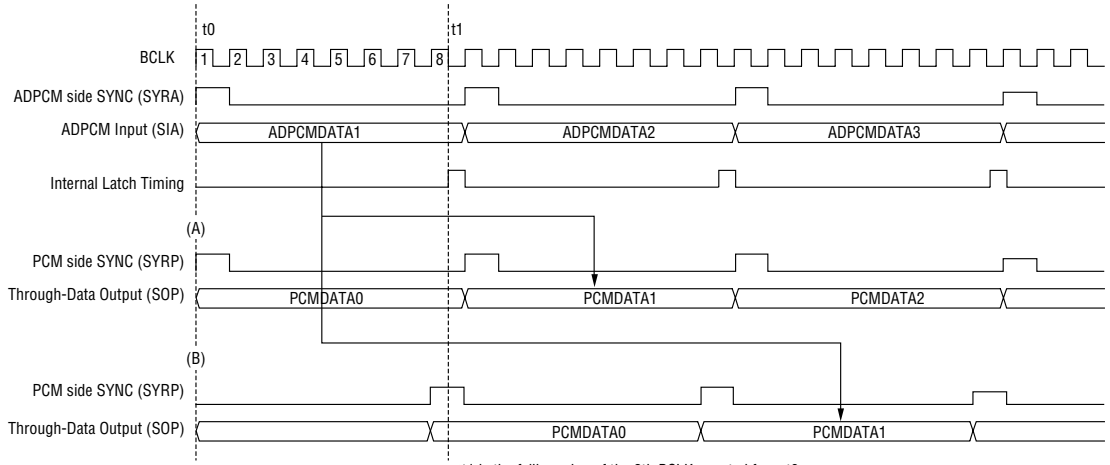


*t1 is the falling edge of the 8th BCLK counted from t0.

(A) When SYXA rises after t1, PCMDATA1 is output to ADPCMDATA1.
(B) When SYXA rises before t1, PCMDATA1 is output to ADPCMDATA1.

If SYXA rises near the t1 and jitter occurs, data slip may occur. Therefore SYXA should not rise in the range of ±500ns from t1.
The data slip means that data is deleted or the same data is output twice.

(2) Through Mode (DECODER Side)



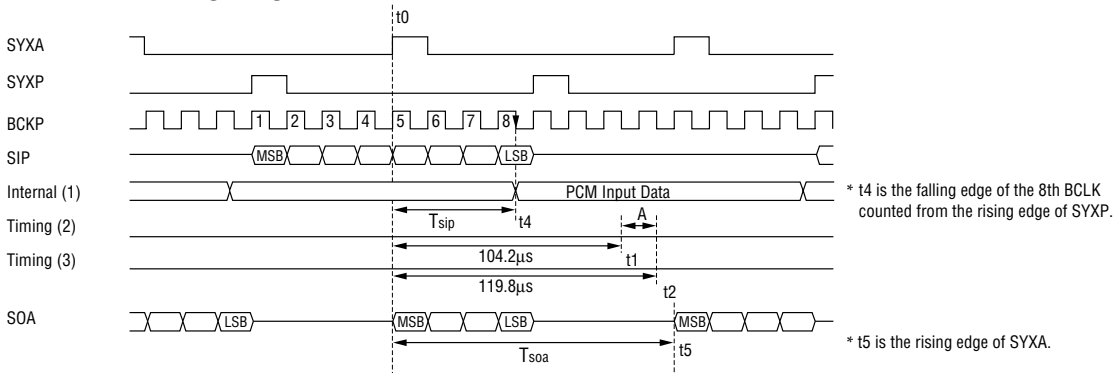
*t1 is the falling edge of the 8th BCLK counted from t0.

(A) When SYRP rises after t1, ADPCMDATA1 is output to PCMDATA1.
(B) When SYRP rises before t1, ADPCMDATA1 is output to PCMDATA1.

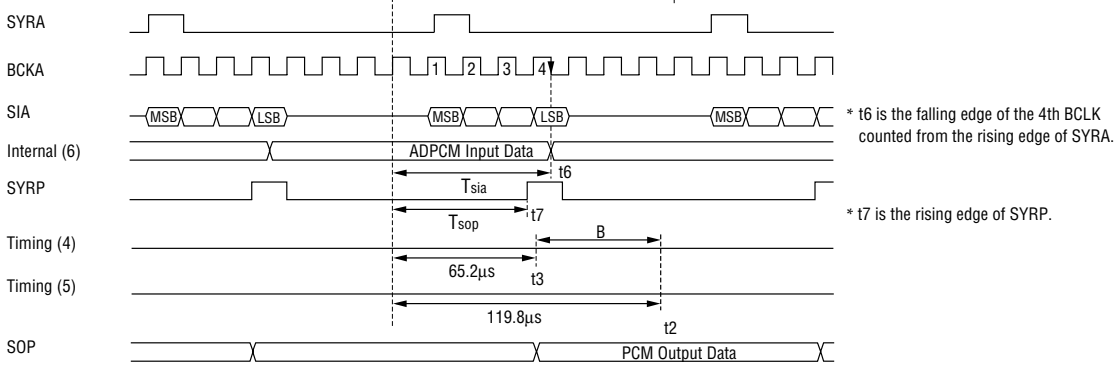
If SYRP rises near the t1 and jitter occurs, data slip may occur. Therefore SYRP should not rise in the range of ±500ns from t1.
The data slip means that data is deleted or the same data is output twice.

(3) PCM→ADPCM, ADPCM→PCM during Transcode

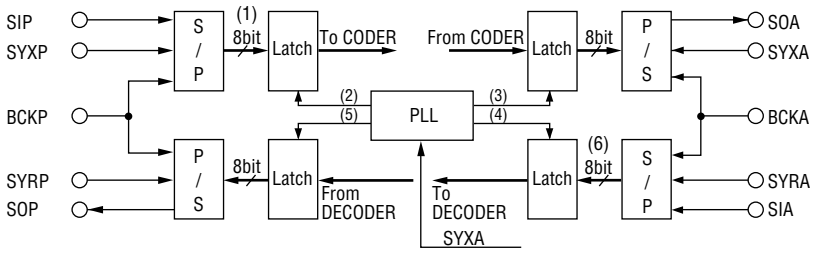
(a) CODER Timing Diagram



(b) DECODER Timing Diagram



(c) Internal Circuit Configuration

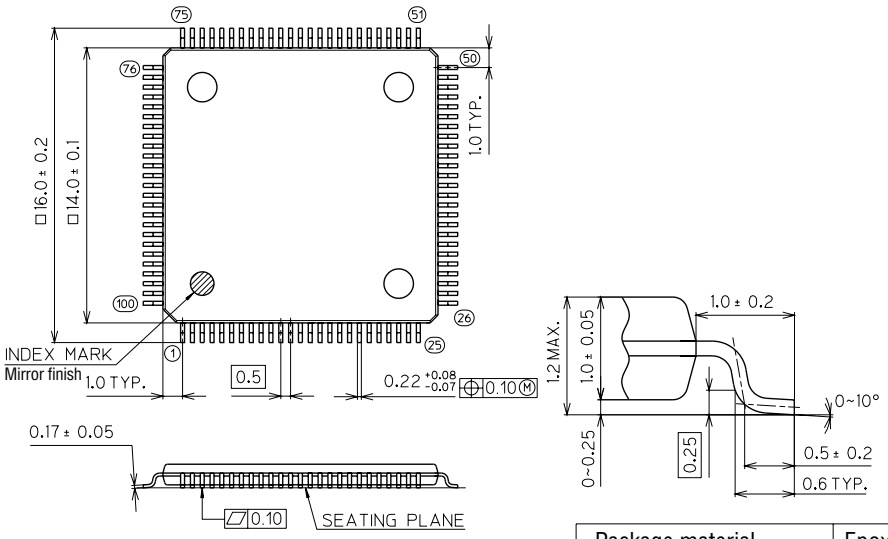


In this device, internal operating signals are generated according to the ADPCM side SYNC (SYXA) signal.
The timings are shouwn in the figures (a) and (b);
The arithmetic operation of CODER is performed at "A" in the figure (a).
The arithmetic operation of DECODER is performed at "B" in the figure (b).
Therefore, when the conversion delay time Tsip of the CODER is less than t1, ADPCM is output at the timing of Tsoa.
When Tsip is more than t1, ADPCM is output at the timing of Tsoa + 125µs.
For DECODER, when Tsia<t3 and Tsop<t2, the conversion delay time is Tsop-Tsia.
As mentioned above, a data ship may occur at Tsip=t1 in CODER, and at Tsia=t3 and Tsop=t2 in DECODER.
Therefore, the timings of SYNC signals of both PCM and ADPCM sides should not be set up in the range about ±500nsec of Tsip=t1, Tsia=t3 and Tsop=t2.
For normal operation, SYNC clocks for ADPCM and PCM sides should be continuous at 8 kHz and synchronized with each other even if their phases are different.

PACKAGE DIMENSIONS

(Unit : mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.55 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).