

MSM7533H/7533V/7534**2ch Single Rail CODEC****GENERAL DESCRIPTION**

The MSM7533 and MSM7534 are two-channel CODEC CMOS ICs for voice signals ranging from 300 to 3400 Hz. These devices contain filters for A/D and D/A conversion.

Designed especially for a single-power supply and low-power applications, these devices contain two-channel AD/DA converters in a single chip and achieve a reduced footprint and a reduced number of external components.

The MSM7533 and MSM7534 are best suited for an analog interface to an echo canceller DSP used in digital telephone terminals, digital PABXs, and hands free terminals.

FEATURES

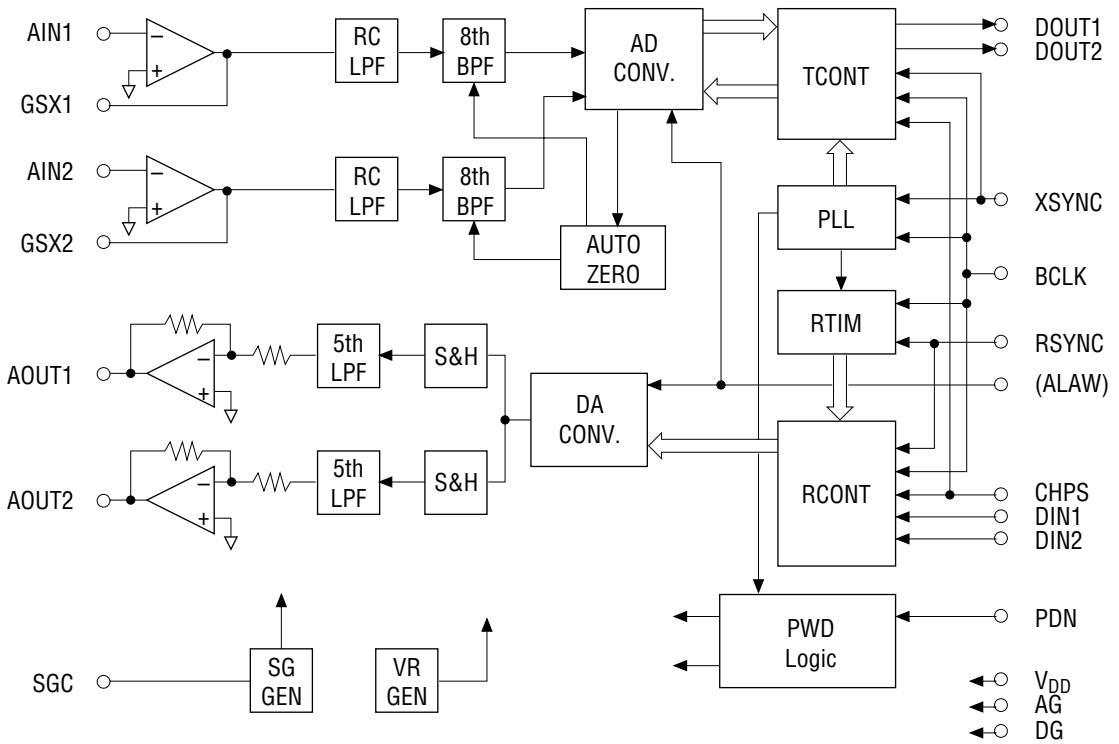
- Single power supply: +5 V
- Power consumption

| | | | |
|------------------|--------------|-------------|-----------------------|
| Operating mode: | 35 mW Typ. | 74 mW Max. | $V_{DD} = 5\text{ V}$ |
| Power save mode: | 7 mW Typ. | 16 mW Max. | $V_{DD} = 5\text{ V}$ |
| Power down mode: | 0.05 mW Typ. | 0.3 mW Max. | $V_{DD} = 5\text{ V}$ |
- ITU-T Companding law

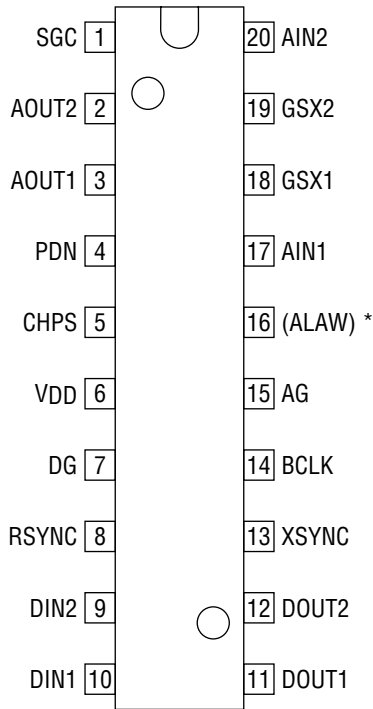
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|-----------|-----------------------------|
| MSM7533H: | μ -law |
| MSM7534: | A-law |
| MSM7533V: | μ /A-law pin selectable |
- Built-in PLL eliminates a master clock
- The PCM interface can be switched between 2 channel serial/parallel
- Transmission clock: 64/128/256/512/1024/2048 kHz
96/192/384/768/1536/1544/200 kHz
(During 2 channel serial mode, the 64 and 96 kHz clocks are disabled)
- Adjustable transmit gain
- Built-in reference voltage supply
- Analog output can directly drive a 600 Ω line transformer
- Package options:

| | |
|---|-------------------------------|
| 20-pin plastic skinny DIP (DIP20-P-300-2.54-S1) | (Product name : MSM7533HRS) |
| | (Product name : MSM7533VRS) |
| | (Product name : MSM7534RS) |
| 24-pin plastic SOP (SOP24-P-430-1.27-K) | (Product name : MSM7533HGS-K) |
| | (Product name : MSM7533VGS-K) |
| | (Product name : MSM7534GS-K) |

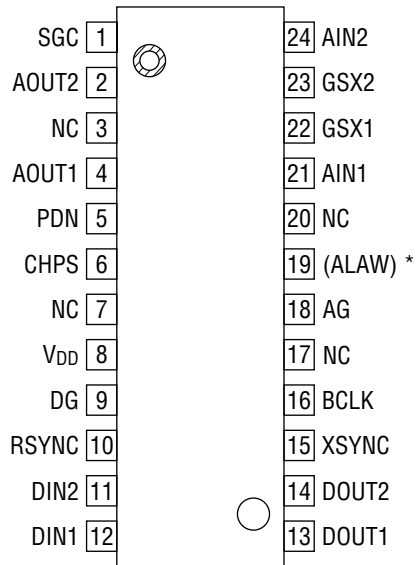
BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



20-Pin Plastic Skinny DIP



NC : No connect pin

24-Pin Plastic SOP

* The ALAW pin is only applied to the MSM7533VRS/MSM7533VGS-K.

PIN AND FUNCTIONAL DESCRIPTIONS

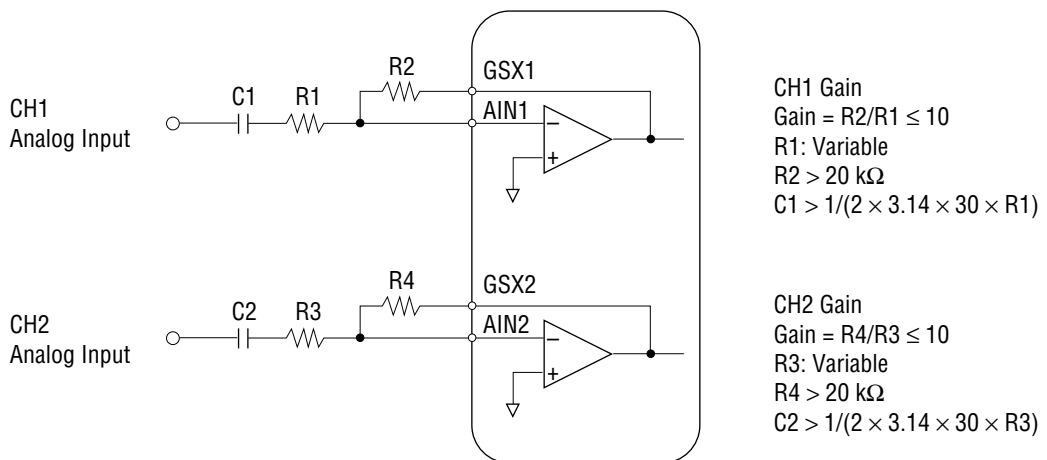
AIN1, AIN2, GSX1, GSX2

AIN1 and AIN2 are the transmit analog inputs for channels 1 and 2.

GSX1 and GSX2 are the transmit level adjustments for channels 1 and 2.

AIN1 and AIN2 are inverting inputs for the op-amp; GSX1 and GSX2 are connected to the output of the op-amp and are used to adjust the level, as shown below.

When not using AIN1 and AIN2, connect AIN1 to GSX1 and AIN2 to GSX2. During power saving and power down mode, the GSX1 and GSX2 outputs are at AG voltage.



AOUT1, AOUT2

AOUT1 is the receive analog output for channel 1 and AOUT2 is used for channel 2.

The output signal has an amplitude of 3.4 V_{PP} above and below the signal ground voltage (SG). When the digital signal of +3 dBmO is input to DIN1 and DIN2, it can drive a load of 600 Ω or more.

During power saving or power down mode, these outputs are at the voltage level of SG with a high impedance.

V_{DD}

Power supply for +5 V.

A power supply for an analog circuit of the system which the device is applied should be used. A bypass capacitor of 0.1 μ F to 1 μ F with excellent high frequency characteristics and a capacitor of 10 μ F to 20 μ F should be connected between this pin and the AG pin if needed.

DIN1

DIN1 is the PCM signal input for channel 1, when the parallel mode is selected.

A serial PCM signal input to this pin is converted to an analog signal in synchronization with the RSYNC signal and BCLK signal.

The analog signal is output from the AOUT1 pin.

The data rate of the PCM signal is equal to the frequency of BCLK signal.

The PCM signal is shifted at a falling edge of the BCLK signal and latched into the internal register when shifted by eight bits.

The start of the PCM data (MSD) is identified at the rising edge of RSYNC.

When the serial mode is selected, this pin is not used and should be connected to GND (0 V).

DIN2

DIN2 is the PCM signal input for channel 2, when the parallel mode is selected.

A serial PCM signal input to this pin is converted to an analog signal in synchronization with the RSYNC signal and BCLK signal.

The analog signal is output from the AOUT2 pin.

The data rate of the PCM signal is equal to the frequency of BCLK signal.

The PCM signal is shifted at a falling edge of the BCLK signal and latched into the internal register when shifted by eight bits.

The start of the PCM data (MSD) is identified at the rising edge of RSYNC.

When the serial mode is selected, this pin is used for the 2ch multiplexed PCM signal input.

BCLK

Shift clock signal input for the DIN1, DIN2, DOUT1, and DOUT2 signals.

The frequency, equal to the data rate, is 64, 96, 128, 192, 256, 384, 512, 768, 1024, 1536, 1544, 2048, or 200 kHz. Setting this signal to logic "1" or "0" drives both transmit and receive circuits to the power saving state.

RSYNC

Receive synchronizing signal input.

The eight bits PCM data required are selected from serial PCM signals on the DIN1 and DIN2 pins by the receive synchronizing signal.

Signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the BCLK (generated from the same clock source as BCLK). The frequency should be 8 kHz \pm 50 ppm to guarantee the AC characteristics which are mainly the frequency characteristic of the receive section.

However, if the frequency characteristic of the system used is not strictly specified, this device can operate in the range of 6 kHz to 9 kHz, but the electrical characteristics in this specifications are not guaranteed.

XSYNC

Transmit synchronizing signal input.

The PCM output signal from the DOUT1 and DOUT2 pins is output in synchronization with this transmit synchronizing signal. This synchronizing signal triggers the PLL and synchronizes all timing signals of the transmit section.

This synchronizing signal must be synchronized in phase with BCLK.

The frequency should be 8 kHz \pm 50 ppm to guarantee the AC characteristics which are mainly the frequency characteristic of the transmit section.

However, if the frequency characteristic of the system used is not strictly specified, this device can operate in the range of 6 kHz to 9 kHz, but the electrical characteristics in this specification are not guaranteed.

Setting this signal to logic "1" or "0" drives both transmit and receive circuits to power saving state.

DOUT1

PCM signal output of channel 1 when the parallel mode is selected.

The PCM output signal is output from MSD in a sequential order, synchronizing with the rising edge of the BCLK signal.

MSD may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.

This pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power saving or power down mode.

When the serial mode is selected, this pin is for the output of serial multiplexed 2ch PCM signal. A pull-up resistor must be connected to this pin because it is an open drain output.

This device is compatible with the ITU-T recommendation on coding law and output coding format.

The MSM7534(A-law) outputs the character signal, inverting the even bits.

| Input/Output Level | PCMIN/PCMOUT | | | | | | | | | | | | | | | |
|--------------------|------------------------|---|---|---|-----------------|---|---|---|---|---|---|---|---|---|---|---|
| | MSM7533H (μ -law) | | | | MSM7534 (A-law) | | | | | | | | | | | |
| | MSD | | | | MSD | | | | | | | | | | | |
| +Full scale | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| +0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| -0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| -Full scale | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

DOUT2

PCM signal outputs for channel 2 when the parallel mode is selected.

The PCM output signal is output from MSD in a sequential order, synchronizing with the rising edge of the BCLK signal.

MSD may be output at the rising edge of the XSYNC signal, based on the timing between BCLK and XSYNC.

This pin is in a high impedance state except during 8-bit PCM output. It is also in a high impedance state during power saving or power down modes.

When the serial mode is selected, this pin is left open.

A pull-up resistor must be connected to this pin because it is an open drain output.

This device is compatible with the ITU-T recommendation on coding law and output coding format.

The MSM7534(A-law) outputs the character signal, inverting the even bits.

CHPS

Control signal input for the mode selection of PCM input and output.

When this signal is at a logic "1" level, the PCM input and output are in the parallel mode. The PCM data of CH1 and CH2 is input to DIN1 and DIN2, and output from DOUT1 and DOUT2 with the same timing.

When this signal is at a logic "0" level, the PCM input and output is in the serial mode. The PCM data of CH1 and CH2 is input to DIN2 and output from DOUT1 as time division multiplexed data.

The parallel mode is conveniently applied to the digital interface to the echo canceller (MSM7520), and the serial mode is applied to the digital interface to PCM multiplexer's for PABXs.

PDN

Power down control signal.

When PDN is at a logic "0" level, both transmit and receive circuits are in a power down state.

AG

Analog signal ground.

DG

Ground for the digital signal circuits.

This ground is separate from the analog signal ground. The DG pin must be connected to the AG pin on the printed circuit board to make a common analog ground.

SGC

Used to generate the signal ground voltage level by connecting a bypass capacitor.

Connect a 0.1 μ F capacitor with excellent high frequency characteristics between the AG pin and the SGC pin.

ALAW

Control signal input of the companding law selection.

Provides only for the MSM7533VRS/MSM7533VGS-K. The CODEC will operate in the μ -law when this pin is at a logic "0" level and the CODEC will operate in the A-law when this pin is at a logic "1" level. The CODEC operates in the μ -law if the pin is left open, since this pin is internally pulled down.

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | Unit |
|-----------------------|------------------|-----------|-------------------------------|------|
| Power Supply Voltage | V _{DD} | — | 0 to 7 | V |
| Analog Input Voltage | V _{AIN} | — | -0.3 to V _{DD} + 0.3 | V |
| Digital Input Voltage | V _{DIN} | — | -0.3 to V _{DD} + 0.3 | V |
| Storage Temperature | T _{STG} | — | -55 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|------------------|---|---|------|------------------------|-----------------|
| Power Supply Voltage | V _{DD} | Voltage must be fixed | 4.75 | 5.0 | 5.25 | V |
| Operating Temperature | T _a | — | -30 | +25 | +85 | °C |
| Analog Input Voltage | V _{AIN} | Gain = 1 | — | — | 3.4 | V _{PP} |
| Digital Input High Voltage | V _{IH} | XSYNC, RSYNC, BCLK, DIN1, DIN2, PDN, CHPS | 2.2 | — | V _{DD} | V |
| Digital Input Low Voltage | V _{IL} | | 0 | — | 0.8 | V |
| Clock Frequency | F _C | BCLK = (eliminates 64, 96 kHz, when 2ch serial mode) | 64, 128, 256, 512, 1024, 2048, 96, 192, 384, 768, 1536, 1544, 200 | | | kHz |
| Sync Pulse Frequency | F _S | XSYNC, RSYNC | 6.0 | 8.0 | 9.0 | kHz |
| Clock Duty Ratio | D _C | BCLK | 40 | 50 | 60 | % |
| Digital Input Rise Time | t _{ir} | XSYNC, RSYNC, BCLK, DIN1, DIN2, PDN, CHPS | — | — | 50 | ns |
| Digital Input Fall Time | t _{if} | | — | — | 50 | ns |
| Transmit Sync Pulse Setting Time | t _{XS} | BCLK→XSYNC, See Timing Diagram | 100 | — | — | ns |
| | t _{SX} | XSYNC→BCLK, See Timing Diagram | 100 | — | — | ns |
| Receive Sync Pulse Setting Time | t _{RS} | BCLK→RSYNC, See Timing Diagram | 100 | — | — | ns |
| | t _{SR} | RSYNC→BCLK, See Timing Diagram | 100 | — | — | ns |
| Sync Pulse Width | t _{WS} | XSYNC, RSYNC | 1 BCLK | — | 100 | μs |
| DIN Set-up Time | t _{DS} | DIN1, DIN2 | 100 | — | — | ns |
| DIN Hold Time | t _{DH} | DIN1, DIN2 | 100 | — | — | ns |
| Digital Output Load | R _{DL} | Pull-up resistor, DOUT1, DOUT2 | 0.5 | — | — | kΩ |
| | C _{DL} | DOUT1, DOUT2 | — | — | 100 | pF |
| Analog Input Allowable DC Offset | V _{off} | Transmit gain stage, Gain = 1 | V _{DD} /2-100 | — | V _{DD} /2+100 | mV |
| | | Transmit gain stage, Gain = 10 | V _{DD} /2-10 | — | V _{DD} /2+10 | mV |
| Allowable Jitter Width | — | XSYNC, RSYNC | — | — | 500 | ns |

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

($V_{DD} = +5\text{ V} \pm 5\%$, $T_a = -30^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|-----------|---|------|------|----------|---------------|
| Power Supply Current | I_{DD1} | Operating mode, No signal | — | 7.0 | 14.0 | mA |
| | I_{DD2} | Power-save mode, PDN = 1, XSYNC or BCLK OFF | — | 1.3 | 3.0 | mA |
| | I_{DD3} | Power-down mode, PDN = 0 | — | 0.01 | 0.05 | mA |
| Input High Voltage | V_{IH} | — | 2.2 | — | V_{DD} | V |
| Input Low Voltage | V_{IL} | — | 0.0 | — | 0.8 | V |
| High Level Input Leakage Current | I_{IH} | — | — | — | 2.0 | μA |
| Low Level Input Leakage Current | I_{IL} | — | — | — | 0.5 | μA |
| Digital Output Low Voltage | V_{OL} | Pull-up resistance $> 500\ \Omega$ | 0.0 | 0.2 | 0.4 | V |
| Digital Output Leakage Current | I_O | — | — | — | 10 | μA |
| Input Capacitance | C_{IN} | — | — | 5 | — | pF |

Transmit Analog Interface Characteristics

($V_{DD} = +5\text{ V} \pm 5\%$, $T_a = -30^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------------|------------|--------------------|------|------|------|------------------|
| Input Resistance | R_{INX} | AIN1, AIN2 | 10 | — | — | $\text{M}\Omega$ |
| Output Load Resistance | R_{LGX} | GSX1, GSX2 | 20 | — | — | $\text{k}\Omega$ |
| Output Load Capacitance | C_{LGX} | with respect to SG | — | — | 30 | pF |
| Output Amplitude | V_{OGX} | | — | — | +1.7 | V |
| Offset Voltage | V_{OSGX} | Gain = 1 | -20 | — | +20 | mV |

Receive Analog Interface Characteristics

($V_{DD} = +5\text{ V} \pm 5\%$, $T_a = -30^\circ\text{C}$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------------|------------|--|------|------|------|------------------|
| Output Load Resistance | R_{LAO} | AOUT1, AOUT2 (each) with respect to SG | 0.6 | — | — | $\text{k}\Omega$ |
| Output Load Capacitance | C_{LAO} | AOUT1, AOUT2 | — | — | 50 | pF |
| Output Amplitude | V_{OAO} | AOUT1, AOUT2, $R_L = 0.6\ \text{k}\Omega$, with respect to SG | -1.7 | — | +1.7 | V |
| Offset Voltage | V_{OSAO} | AOUT1, AOUT2 with respect to SG | -100 | — | +100 | mV |

AC Characteristics

(V_{DD} = +5 V ±5%, T_a = -30°C to +85°C)

| Parameter | Symbol | Freq. (Hz) | Level (dBm0) | Condition | Min. | Typ. | Max. | Unit |
|-------------------------------------|---------|------------|--------------|-----------|-----------|-------|-------|------|
| Transmit Frequency Response | Loss T1 | 60 | 0 | | 20 | 26 | — | dB |
| | Loss T2 | 300 | | | -0.15 | +0.07 | +0.20 | |
| | Loss T3 | 1020 | | | Reference | | | dB |
| | Loss T4 | 2020 | | | -0.15 | -0.04 | +0.20 | |
| | Loss T5 | 3000 | | | -0.15 | +0.06 | +0.20 | |
| | Loss T6 | 3400 | | | 0 | 0.4 | 0.80 | |
| Receive Frequency Response | Loss R1 | 300 | 0 | | -0.15 | -0.03 | +0.20 | dB |
| | Loss R2 | 1020 | | | Reference | | | |
| | Loss R3 | 2020 | | | -0.15 | -0.02 | +0.20 | dB |
| | Loss R4 | 3000 | | | -0.15 | +0.15 | +0.20 | |
| | Loss R5 | 3400 | | | 0.0 | 0.45 | 0.80 | |
| Transmit Signal to Distortion Ratio | SD T1 | 1020 | 3 | *1 | 35 | 43 | — | dB |
| | SD T2 | | 0 | | 35 | 41 | — | |
| | SD T3 | | -30 | | 35 | 38 | — | |
| | SD T4 | | -40 | | 29 | 31.5 | — | |
| | SD T5 | | -45 | | 24 | 27 | — | |
| Receive Signal to Distortion Ratio | SD R1 | 1020 | 3 | *1 | 36 | 43 | — | dB |
| | SD R2 | | 0 | | 36 | 41 | — | |
| | SD R3 | | -30 | | 36 | 40 | — | |
| | SD R4 | | -40 | | 30 | 33.5 | — | |
| | SD R5 | | -45 | | 25 | 30 | — | |
| Transmit Gain Tracking | GT T1 | 1020 | 3 | | -0.3 | +0.01 | +0.3 | dB |
| | GT T2 | | -10 | | Reference | | | |
| | GT T3 | | -40 | | -0.3 | -0.09 | +0.3 | |
| | GT T4 | | -50 | | -0.5 | -0.09 | +0.5 | |
| | GT T5 | | -55 | | -1.2 | -0.1 | +1.2 | |
| Receive Gain Tracking | GT R1 | 1020 | 3 | | -0.3 | 0 | +0.3 | dB |
| | GT R2 | | -10 | | Reference | | | |
| | GT R3 | | -40 | | -0.3 | +0.09 | +0.3 | |
| | GT R4 | | -50 | | -0.5 | +0.2 | +0.5 | |
| | GT R5 | | -55 | | -1.2 | +0.23 | +1.2 | |

*1 Psophometric filter is used

AC Characteristics (Continued)

(V_{DD} = +5 V ±5%, Ta = -30°C to +85°C)

| Parameter | Symbol | Freq. (Hz) | Level (dBm0) | Condition | Min. | Typ. | Max. | Unit |
|--|--------------------|------------|--------------|---|-------|-------|-------|-------|
| Idle Channel Noise | Nidle T | — | — | AIn = SG *1 *2 | — | -73.5 | -70 | dBmOp |
| | Nidle R | — | — | *1 *3 | — | -78 | -75 | |
| Absolute Level (Initial Difference) | AV T | 1020 | 0 | V _{DD} = 5.0 V Ta = 25°C *4 | 0.821 | 0.850 | 0.880 | Vrms |
| | AV R | | | | 0.821 | 0.850 | 0.880 | |
| Absolute Level (Deviation of Temperature and Power) | AV Tt | 1020 | 0 | V _{DD} = 5 V ± 5% Ta = -30 to 85°C *4 | -0.2 | — | +0.2 | dB |
| | AV Rt | | | | -0.2 | — | +0.2 | dB |
| Absolute Delay | Td | 1020 | 0 | A to A BCLK = 64 kHz | — | — | 0.6 | ms |
| Transmit Group Delay | t _{gd} T1 | 500 | 0 | *5 | — | 0.19 | 0.75 | ms |
| | t _{gd} T2 | 600 | | | — | 0.11 | 0.35 | |
| | t _{gd} T3 | 1000 | | | — | 0.02 | 0.125 | |
| | t _{gd} T4 | 2600 | | | — | 0.05 | 0.125 | |
| | t _{gd} T5 | 2800 | | | — | 0.07 | 0.75 | |
| Receive Group Delay | t _{gd} R1 | 500 | 0 | *5 | — | 0.00 | 0.75 | ms |
| | t _{gd} R2 | 600 | | | — | 0.00 | 0.35 | |
| | t _{gd} R3 | 1000 | | | — | 0.00 | 0.125 | |
| | t _{gd} R4 | 2600 | | | — | 0.09 | 0.125 | |
| | t _{gd} R5 | 2800 | | | — | 0.12 | 0.75 | |
| Crosstalk Attenuation | CR T | 1020 | 0 | TRANS → RECV | 75 | 80 | — | dB |
| | CR R | | | RECV → TRANS | 70 | 76 | — | |
| | CR CH | | | CH to CH | 73 | 78 | — | |

*1 Psophometric filter is used

*2 Upper is specified for the μ-law, lower for the A-law

*3 Input "0" code to PCMIN

*4 AVT is defined between GSX and DOUT and AVR between DIN and AOUT

*5 Minimum value of the group delay distortion

AC Characteristics (Continued)

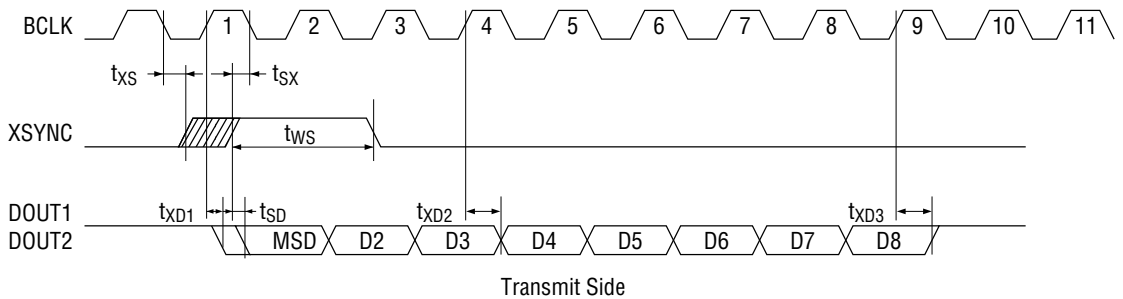
(V_{DD} = +5 V ±5%, T_a = -30°C to +85°C)

| Parameter | Symbol | Freq. (Hz) | Level (dBm0) | Condition | Min. | Typ. | Max. | Unit |
|------------------------------------|------------------|--|---------------------|----------------------------------|------|-------|------|------|
| Discrimination | DIS | 4.6 kHz to 72 kHz | 0 | 0 to 4000 Hz | 30 | 32 | — | dB |
| Out-of-band Spurious | S | 300 to 3400 | 0 | 4.6 kHz to 100 kHz | — | -37.5 | -35 | dBm0 |
| Intermodulation Distortion | IMD | f _a = 470 f _d = 320 | -4 | 2f _a - f _d | — | -52 | -35 | dBm0 |
| Power Supply Noise Rejection Ratio | PSR T | 0 to 50 kHz | 50 mV _{PP} | *6 | — | 30 | — | dB |
| | PSR R | | | | | | | |
| Digital Output Delay Time | t _{SD} | C _L = 100 pF + 1 LSTTL | | | 20 | — | 200 | ns |
| | t _{XD1} | | | | 20 | — | 200 | |
| | t _{XD2} | | | | 20 | — | 200 | |
| | t _{XD3} | | | | 20 | — | 200 | |

*6 The measurement under idle channel noise

TIMING DIAGRAM

Transmit Timing



Receive Timing

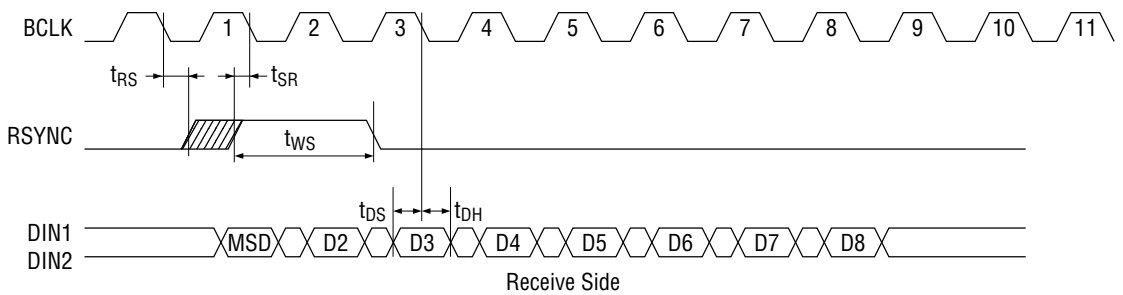


Figure. 1 Timing Diagram in the Parallel Mode (CHPS = 1)

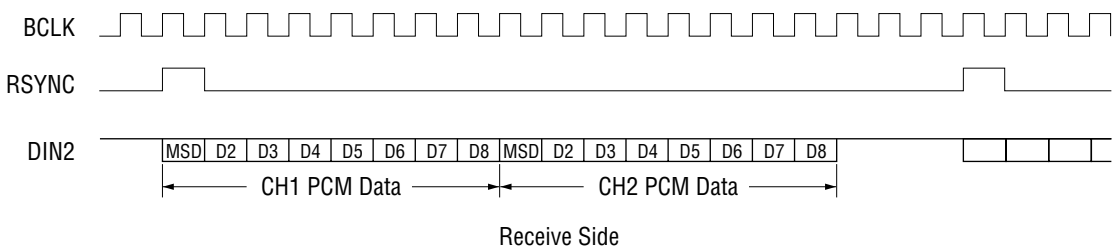
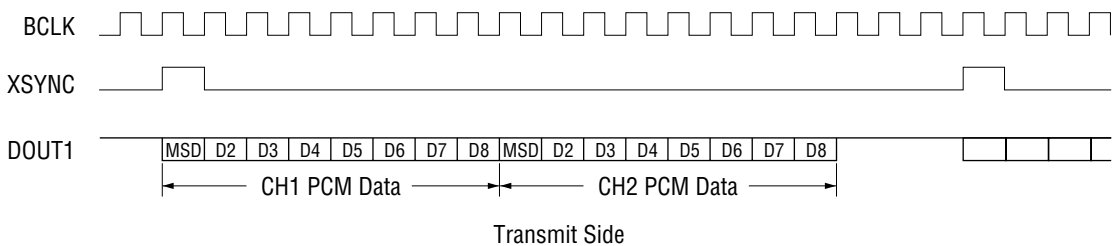
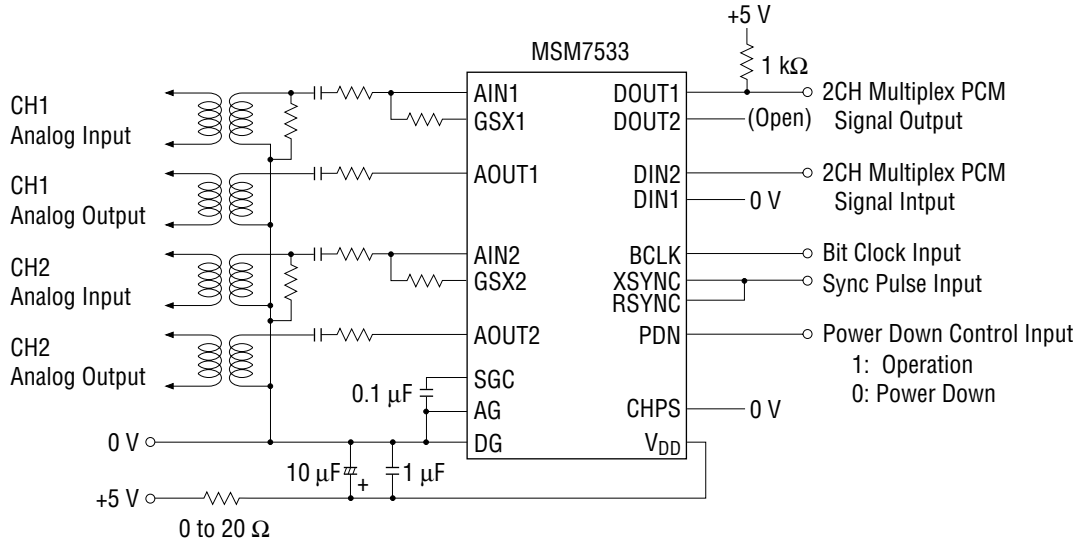


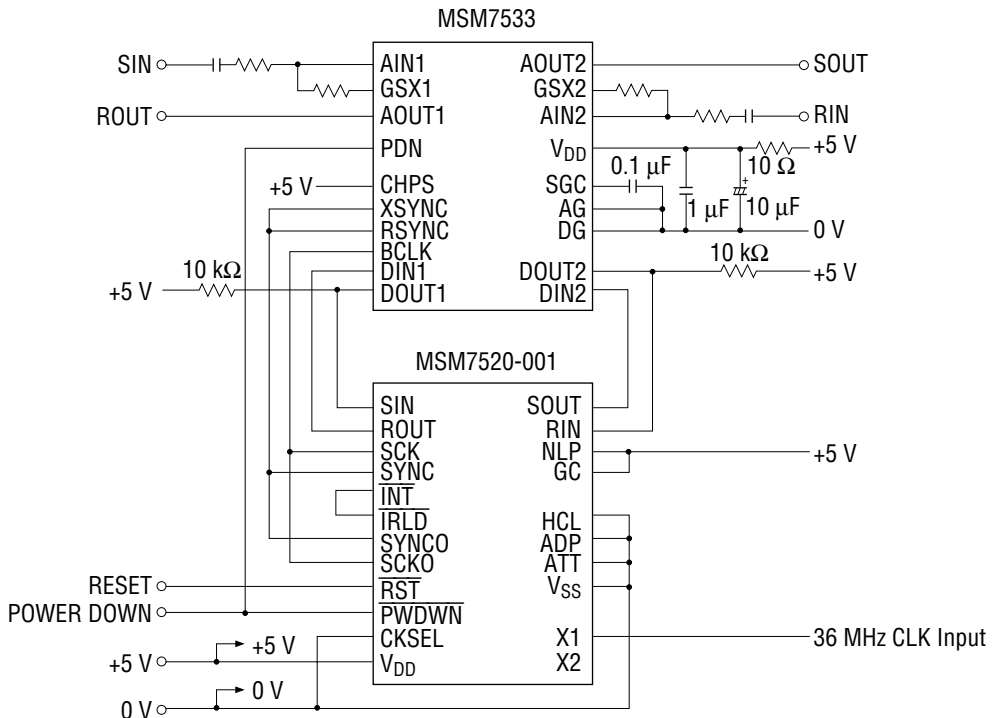
Figure. 2 Timing Diagram in the Serial Mode (CHPS = 0)

APPLICATION CIRCUIT

Example of Basic Connection (PCM Serial Mode Operation)



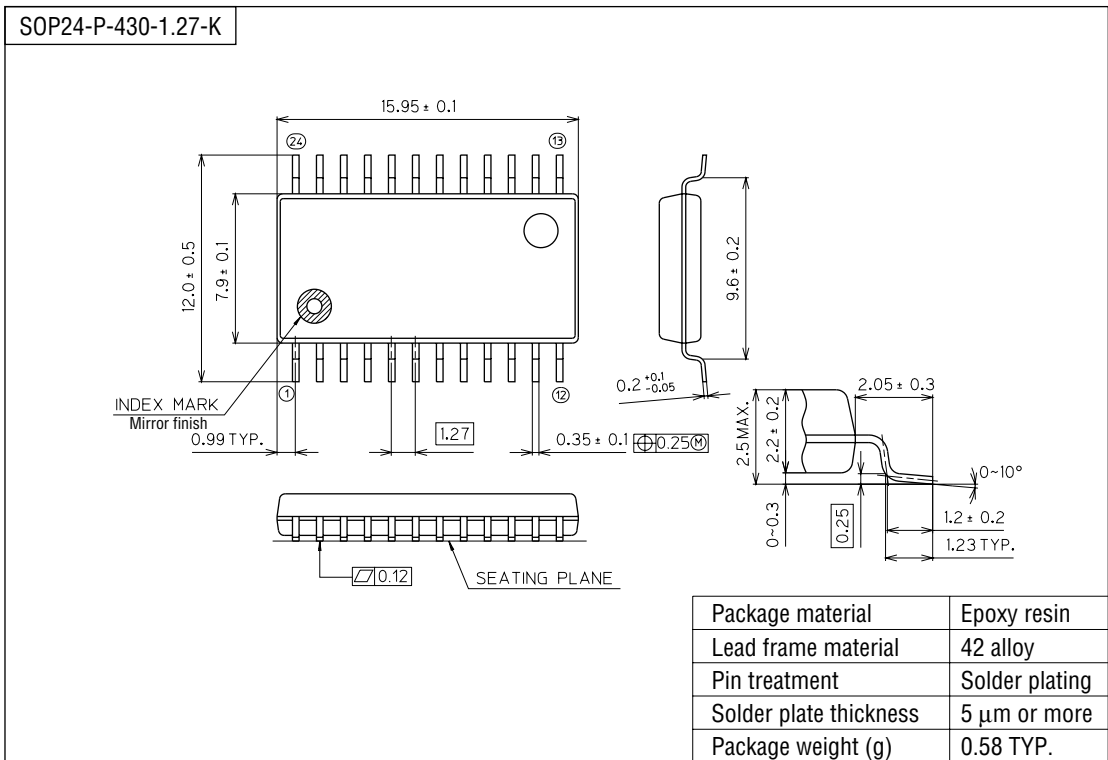
Example of Interface to the Echo Canceller MSM7520



RECOMMENDATIONS FOR ACTUAL DESIGN

- To assure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and the DG pin each other as close as possible. Connect to the system ground with low impedance.
- Mount the device directly on the board when mounted on PCBs. Do not use IC sockets. If an IC socket is unavoidable, use the short lead type socket.
- When mounted on a frame, use electro-magnetic shielding, if any electro-magnetic wave source such as power supply transformers surround the device.
- Keep the voltage on the V_{DD} pin not lower than -0.3 V even instantaneously to avoid latch-up phenomenon when turning the power on.
- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of these devices.

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki’s responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).