

MSM6808/6818

SPLIT FILTER LSI FOR MODEM FUNCTION IN THE CELLULAR MOBILE PHONE

GENERAL DESCRIPTION

The MSM6808 and MSM6818 perform the split filtering functions in the modem part of the cellular mobile phone.

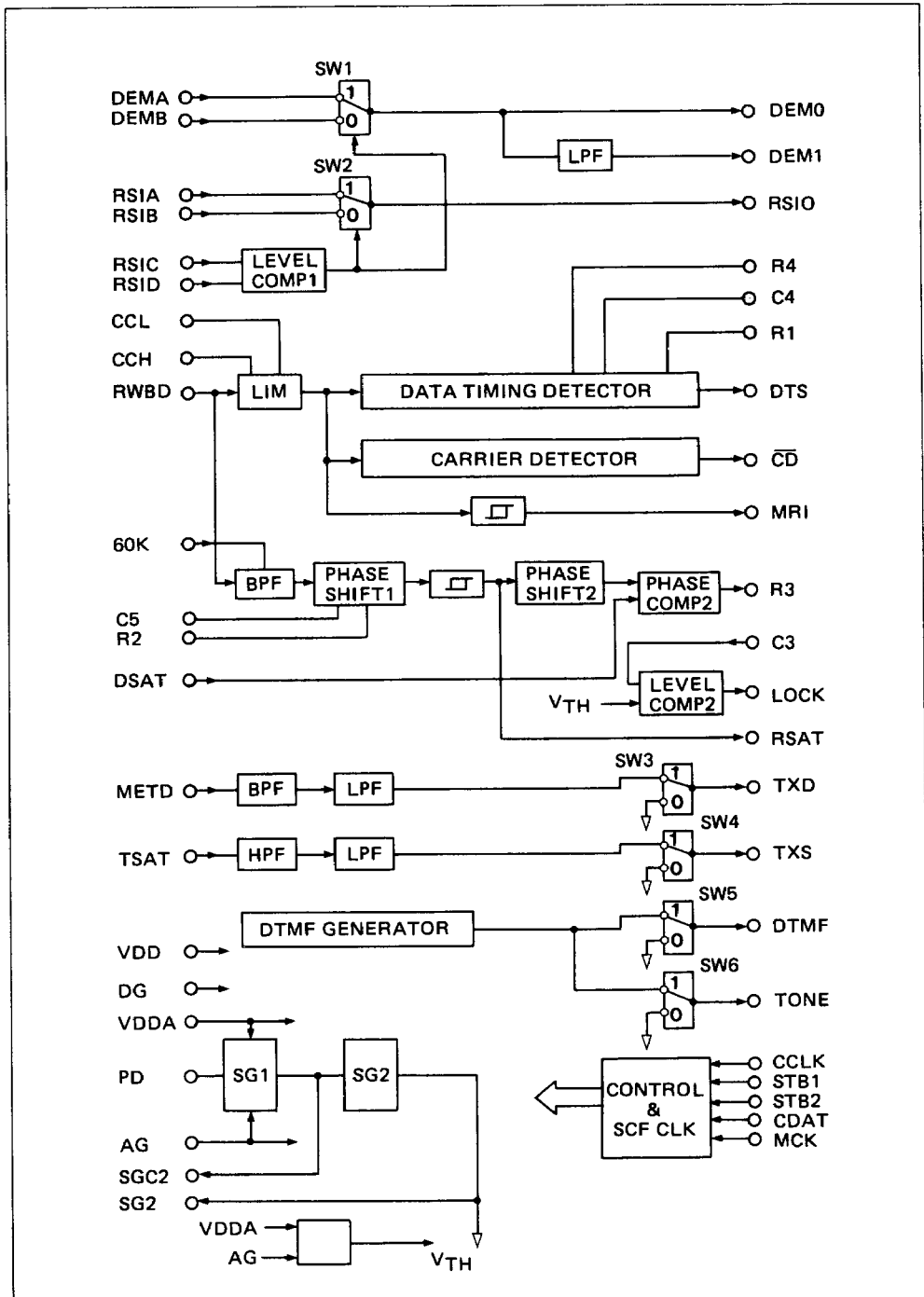
Each of the MSM6808 and MSM6818 consists of a Received Wide Band Data (RWBD) detector, a MODEM DATA Signal (MODEM DATA) transmitter, a Supervisory Audio Tone (SAT) receiver, a SAT transmitter, and a DTMF signal transmitter and is fabricated by OKI's low power consumption CMOS silicon gate technology.

In combination with the MSM74017, MSM6808 can realize a 10K bps SPL modem for AMPS (Advanced Mobile Phone Service) system. MSM6818 can realize a 8K bps SPL modem for TACS (Total Access Communications System) system.

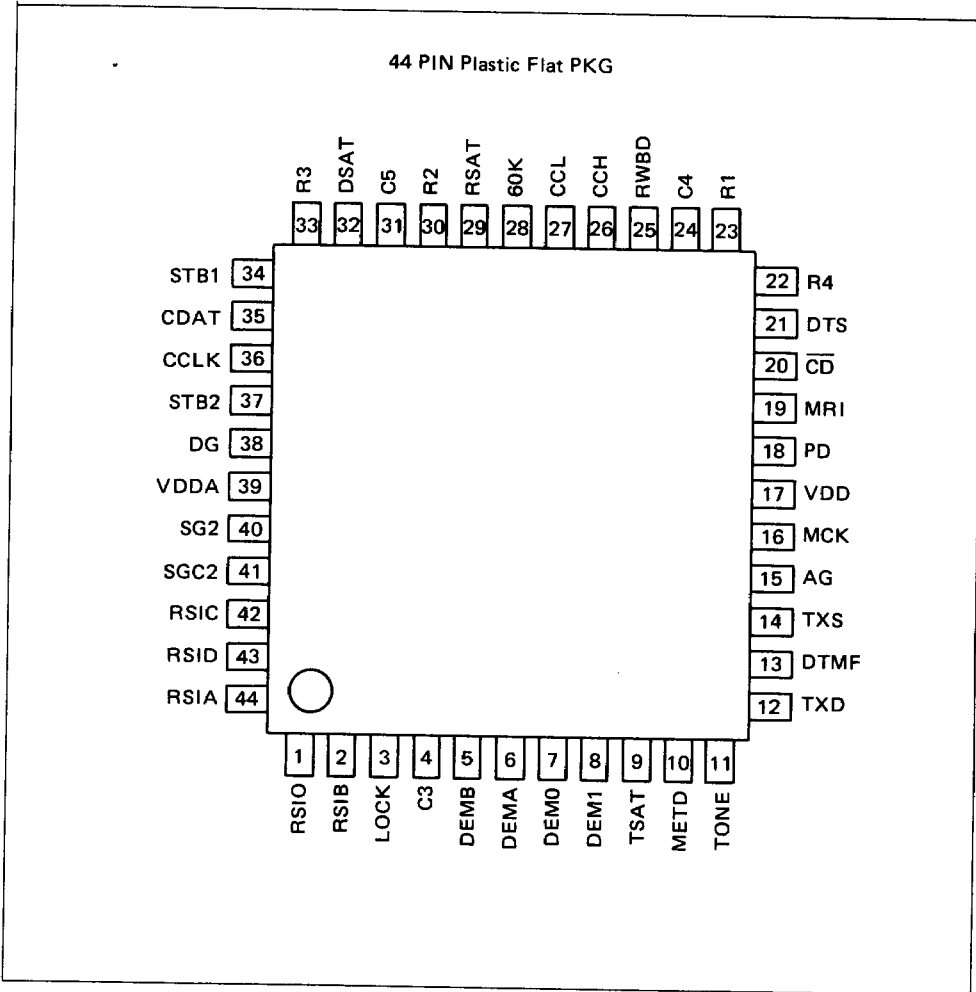
FEATURES

- Built-in timing re-generating circuit for received data.
- Built-in Switched Capacitor Filters for SAT and MODEM data.
- Built-in Anti-Aliasing filters and Smoothing Filters.
- DTMF generator circuit on chip.
- Received signal level comparator for diversity system.
- Microcomputer interface serial control data.
- Power supply: +5 V.
- Low power consumption: 40 mW (typ).
- 44-pin plastic FLAT package.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	Pin No.	I/O	Function
RSIO	1	O	Received signal Strength Output. The larger DC level applied to RSIA and RSIB is put out of RSIO.
RSIB	2	I	Received signal Strength Input (B). DC levels are applied to RSIA and RSIB pins.
LOCK	3	O	SAT (Supervisory Audio Tone) Lock. The LOCK determines whether RSAT (Received SAT) and TSAT (Transmitting SAT) are synchronized or not. The LOCK is set at logical 1, when the phase of DSAT exceeds $+270^\circ$ compared with that of the RSAT signal.
C3	4	I	Form LPF by connecting a resistor and a capacitor between R3 and C3. See Figure 7.
DEMB	5	I	Demodulated signal input (B). The DEMB pin is enabled if $RSIC < RSID$.
DEMA	6	I	Demodulated signal input (A). The DEMA pin is enabled if $RSIC > RSID$.
DEMO	7	O	Demodulated signal output (0). Connect this pin to DEMO of MSM6807.
DEM1	8	O	Demodulated signal output (1). Connect this pin to RWBD.
TSAT	9	I	Transmitting SAT signal. The phase of TSAT should be more than $+270^\circ$ compared with that of the RSAT output signal. The TSAT signal is same as the DSAT signal.
METD	10	I	Transmitting Manchester Encoded Data.
TONE	11	O	DTMF SIDETONE output. Connect this pin to TONE of MSM6807.
TXD	12	O	Transmitting Data. Digital data applied to METD becomes sinusoidal wave signals coming through filters.
DTMF	13	O	Dual Tone Multi Frequency. Each DTMF signal consists of two sinusoidal waves, one from a low group (697, 770, 852, 941 Hz) and the other from a high group (1209, 1336, 1477, 1633, 2016 Hz).

Pin Name	Pin No.	I/O	Function
DTMF	13	O	The level has +6 dB/oct. pre-emphasis characteristics. CCLK, STB2 and CDAT control the frequency, selection of dual tone or single tone. See Table 2.
TXS	14	O	Transmitting SAT. The digital signal input to TSAT becomes sinusoidal wave through a band limited filter.
AG	15	—	Analog Ground. This pin should be common with the DG at the point which is as close as possible to the system ground.
MCK	16	I	Master Clock. Use a 1 MHz ($\pm 0.01\%$) MCK.
VDD	17	—	Power supply pin for the digital circuit. +5V shall be applied.
PD	18	I	Power Down function enable pin. The PD signal selects power on or off; logical 0 enables the power down mode. In the power down mode, transmitting function, SAT function and DTMF output function are suspended.
MRI	19	O	Output for the Manchester Encoded data derived from RWBD input data. See Figure 6.
\overline{CD}	20	O	Carrier Detection. The carrier detector detects dotting pattern (10101010) input to the RWBD. When the frequency of input signal to MSM6808 is approx. 5 kHz, the \overline{CD} of MSM6808 becomes logical 0, while \overline{CD} is logical 1 for any other frequencies. When the frequency of input signal to MSM6818 is approx. 4 kHz, the \overline{CD} of MSM6818 becomes logical 0, while \overline{CD} is logical 1 for any other frequencies.
DTS	21	O	Derived Timing Signal. Output for the timing clock derived from the RWBD input data. When a 5 kHz data is input to the RWBD of MSM6808, a 10 kHz signal is obtained. When a 4 kHz data is input to the RWBD of MSM6818, a 8 kHz signal is obtained.
R4	22	—	DTS sensitivity adjustment. An external resistor R9 shall be connected between R4 and SG2.

◆ WIRELESS SYSTEM - MSM6808/18 ◆

Pin Name	Pin No.	I/O	Function																		
R1	23	—	DTS phase adjustment. An external resistor R8 shall be connected between R1 and SG2.																		
C4	24	—	DTS phase adjustment. If phase cannot be sufficiently adjusted, connect an external capacitor between C4 and R1. C4 pin shall be left open when it is not used.																		
RWBD	25	I	Received Wide Band Data input pin. Received data and SAT signal are input to this pin. This pin shall be connected to DEM1 directly.																		
CCH	26	—	An external resistor and capacitor shall be connected between CCL and CCH. See Figure 7.																		
CCL	27	—																			
60K	28	I	<p>The 60K signal controls the center frequency of the BPF (RWBD block). According to the SAT frequency input to RWBD, the frequency of control signal input to the 60K pin changes as below.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2">SAT (WRBD)</th> <th colspan="2">RS10</th> <th colspan="2">Center Frequency (BPF)</th> </tr> </thead> <tbody> <tr> <td>5970</td> <td rowspan="3" style="text-align: center; vertical-align: middle;">Hz</td> <td>59.7</td> <td rowspan="3" style="text-align: center; vertical-align: middle;">kHz</td> <td>5970</td> <td rowspan="3" style="text-align: center; vertical-align: middle;">Hz</td> </tr> <tr> <td>6000</td> <td>60.0</td> <td>6000</td> </tr> <tr> <td>6030</td> <td>60.3</td> <td>6030</td> </tr> </tbody> </table> <p>Normally the 60K control signal is made by the digital PLL.</p>	SAT (WRBD)		RS10		Center Frequency (BPF)		5970	Hz	59.7	kHz	5970	Hz	6000	60.0	6000	6030	60.3	6030
SAT (WRBD)		RS10		Center Frequency (BPF)																	
5970	Hz	59.7	kHz	5970	Hz																
6000		60.0		6000																	
6030		60.3		6030																	
RSAT	29	O	Received SAT. The RSAT output signal is applied to the external digital PLL. The phase of RSAT through the PLL exceeds +270°.																		
R2	30	—	Received SAT signal phase adjustment. An external resistor R7 shall be connected between R2 and SG2.																		
C5	31	—	Received SAT signal phase adjustment. An external capacitor C22 shall be connected between C5 and R2.																		
DSAT	32	I	Data SAT. The "PHASE COMP2" judges the difference of the phase between RSAT and DSAT. The phase of DSAT (equals to TSAT) should be exceeded +270° compared with RSAT. In other cases, RSAT and TSAT is not locked. See "BLOCK DIAGRAM".																		

Pin Name	Pin No.	I/O	Function
R3	33	—	Refer to the description of pin 4.
STB1	34	I	Strobe 1. Refer to the description of CDAT.
CDAT	35	I	Serial Control Data. The CDAT and STB1 signal control the internal switches. DTMF frequency is selected by CDAT and STB2. See Table 1.
CCLK	36	I	Control timing clock. See Table 1.
STB2	37	I	Strobe 2. Refer to the description of CDAT.
DG	38	—	Digital Ground. This pin should be common with the AG at the point which is as close as possible to the system ground.
VDDA	39	—	Power supply pin for the analog circuit. +5V shall be applied.
SG2	40	Power	SG2 is built-in analog ground. This voltage is nearly $\frac{VDDA}{2}$ V, so the analog line interface must be implemented by AC-coupling except in the case of connecting with MSM6807. To make its impedance lower, it is necessary to be AC grounded for AG via a bypass capacitor of more than 2.2 μ F.
SGC2	41	Power	This is voltage reference for SG and is obtained by two-equal resistors division among VDDA and AG. It is necessary to be AC grounded for AG via a bypass capacitor of more than 2.2 μ F so as to keep SG2 silent.
RSIC	42	I	Received signal Strength input (C). The rectified signal of the RSIA input signal is applied to this pin through external LPF. See "APPLICATION".
RSID	43	I	Received signal Strength input (D). Same as RSIC, the rectified signal of the RSIB is applied to this pin through LPF. The DC levels of RSIC and RSID determine the status of SW1, SW2. See Table 1.
RSIA	44	I	Received signal Strength input (A). DC levels are applied to RSIA and RSIB.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Type	Max	Unit
Power Supply Voltage	V_{DD} V_{DDA}	$T_a = +25^\circ\text{C}$ With respect to AG or DG	-0.3	—	7	V
Analog Input Voltage* ¹	V_{IA}		-0.3	—	$V_{DDA} + 0.3$	
Digital Input Voltage* ²	V_{ID}		-0.3	—	$V_{DD} + 0.3$	
Operating Temperature	T_{op}		-40	—	85	°C
Storage Temperature	T_{stg}		-55	—	125	

*¹ DEMA, DEMB, RSIA, RSIB, RWBD*² RSIC, RSID, RS10, DSAT, METD, TSAT, STB1, STB2, CDAT, MCK, CCLK

Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply Voltage	V_{DD} V_{DDA}	With respect to AG or DG	4.75	5.0	5.25	V
Operating Temperature	T_{op}		-30	—	70	°C
Master Clock Frequency	f_{MCK}		0.9999	1	1.0001	MHz

DC AND DIGITAL INTERFACE CHARACTERISTICS

 $V_{DDA}, V_{DD} = 5V \pm 5\%$, $T_a = -30 \sim 70^\circ\text{C}$

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Power Dissipation (standby)	I_{DD}	—	—	10	15	mA	—
	I_{DDS}		—	6	9		
Input Leak Current	I_{IL}	$V_I = 0V$	-10	—	10	μA	MCK STB1 STB2 CLK CDAT
	I_{IH}	$V_I = V_{DD}$	-10	—	10		
Input Voltage	V_{IL}	—	0	—	$0.3 V_{DD}$	—	DTS MRI CD RSAT
	V_{IH}		$0.7 V_{DD}$	—	V_{DD}		
Output Voltage	V_{OL}	$I_{OL} = -1.6 \text{ mA}$	—	—	$0.3 V_{DD}$	—	DTS MRI CD RSAT
	V_{OH}	$I_{OH} = 400 \mu\text{A}$	$0.7 V_{DD}$	—	—		

ANALOG INTERFACE CHARACTERISTICS

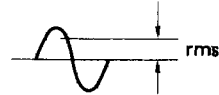
$$V_{DDA}, V_{DD} = 5V \pm 5\%, T_a = -30 \sim 70^\circ C$$

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Input Impedance*1	R _{AIN}	—	100	—	—	k Ω	—

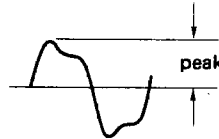
*1 RSIC, RSID, RWBD, METD, TSAT, DSAT

Definition of Units

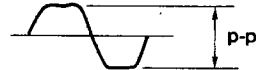
dBV_{rms} : $20 \cdot \log V$, where V denotes the root mean square value of the signal voltage.



dBV_p : $20 \cdot \log V$, where V denotes the peak value of the signal voltage.



V_{p-p} : Peak-peak value of the signal voltage.



DEM, RSSI CHARACTERISTICS

$$V_{DDA}, V_{DD} = 5V \pm 5\%, T_a = -30 \sim 70^\circ C$$

Parameter	Symbol	Condition		Min	Typ	Max	Unit	Note
DEM0 Output Level	V _{ODEM0}	V _i (DEM) = -14.2 dBV _{rms} f _i = 1 kHz		—	-11.2	—	dBV _{rms}	+3dB
DEM1 Output Level	V _{ODEM1}			—	2.2	—	V _{p-p}	+12dB
RSIO Output Level	V _{ORSIL}	V _I =0V	R _L ≥ 100K	—	0	—	V	—
	V _{ORSIH}	V _I =3.15V		—	3.15	—		
RSSI Hysteresis	V _{HYS}	—		—	30	—	mV	RSIC RSID
DEM1 LPF Cut-off frequency	f _{CDEM}	At the point 2dB lower		20	—	—	kHz	—
DEM1 Undesired Wave Leakage	—	DEMA, DEMB silent		—	—	-50	dBV _{rms}	—

RWBD SAT

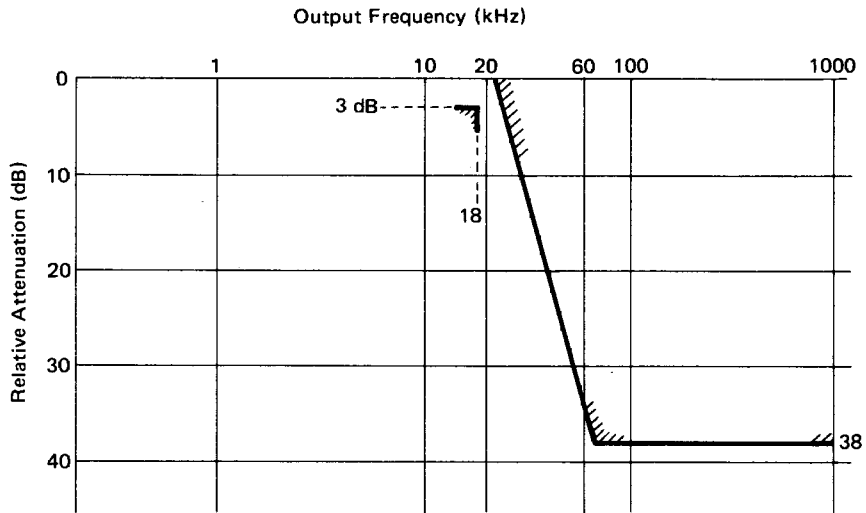
$V_{DDA}, V_{DD} = 5V \pm 5\%, T_a = -30 \sim 70^\circ C$

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note		
DTS Output Duty Ratio	DRDTS	V_i (RWBD) = 2.3Vp-p $f_i = 5$ kHz	-	50	-	%	$f_{DTS} =$ kHz		
\overline{CD}	Sensitivity	V_i (RWBD) = 2.3Vp-p	MSM6808	MSM6818	-	V_{DD}	-	-	
			$f_i = 3.5k \pm 100Hz$	$f_i = 2.8k \pm 100Hz$					
			FSCD1	FSCD2					5k \pm 100Hz
	FSCD3	6.5k \pm 100Hz	5.2k \pm 100Hz	-	V_{DD}	-			
	Response	t_{D1}	Figure 5		-	-	2		ms
t_{D2}		2	-	-					
MRI/DTS Delay Time	t_d	R9 = 10 Ω R8 = 175 k Ω C4 open	-	21	-	μs	Figure 6		
RSAT Sensitivity	V_{RSAT}	$f_i = 5970$ Hz 6000 6030	-20	-	-	dBV-rms			

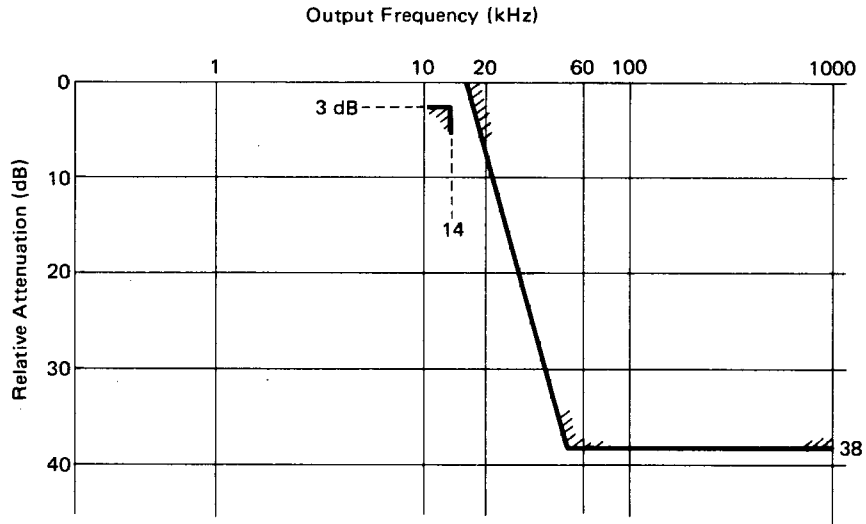
TX-AUDIO (TXD/TXS/DTMF) CHARACTERISTICS

 $V_{DDA}, V_{DD} = 5V \pm 5\%$, $T_a = -30 \sim 70^\circ\text{C}$

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
METD Output Level	VOTXD	$V_{IL} = 0\text{ V}$, $V_{IH} = V_{DD}$ $f_i = 10\text{ kHz}$ (MSM6808) $f_i = 8\text{ kHz}$ (MSM6818) square wave (50%)	—	-8.2	—	dBVp	SW3="1"
METD Frequency Characteristics	—	$V_{IL} = 0\text{ V}$, $V_{IH} = V_{DD}$ square wave (50%)	Figure 1			—	—
TXS Output Level	VOTXS	$V_{IL} = 0\text{ V}$, $V_{IH} = V_{DD}$ square wave (50%) $f_i = 6\text{ kHz}$	—	-23.2	—	dBVrms	SW4="1"
TSAT Frequency Characteristics	—	$V_{IL} = 0\text{ V}$, $V_{IH} = V_{DD}$ square wave (50%)	Figure 2			—	—
DTMF Output Level	VOL1	$f_0 = 697\text{ Hz}$	—	-19.3	—	dBVrms	Emphasis (6dB/oct) Figure 3 MCK=1MHz
	VOL2	770	—	-18.4	—		
	VOL3	852	—	-17.6	—		
	VOL4	941	—	-16.7	—		
	VOH1	$f_0 = 1209\text{ Hz}$	—	-14.5	—		
	VOH2	1336	—	-13.6	—		
	VOH3	1477	—	-12.8	—		
VOH4	1633	—	-11.9	—			
Sounder Output Level	VOTONE	$f_0 = 2016\text{ Hz}$	—	-25	—	dBVrms	SW6="1"
DTMF Side Tone Output Level	VODST	697, 1633 Hz Pair	—	-22	—	dBVrms	
DTMF Distortion	D _{DTMF}	—	—	—	10	%	—
DTMF Output Frequency Error	ΔF_{DTMF}	MCK = 1 MHz	-1.5	—	+1.5	%	—
TONE Undesired Wave Leakage	—	TXD/TXS/DTMF	—	—	-61	dBVrms	SW3="0" SW4="0" SW5="0"
Out-band Noise Level	—	TX-AUDIO RX-AUDIO	Figure 4			—	—



METD Frequency Characteristics (MSM6808)



METD Frequency Characteristic (MSM6818)

Figure 1

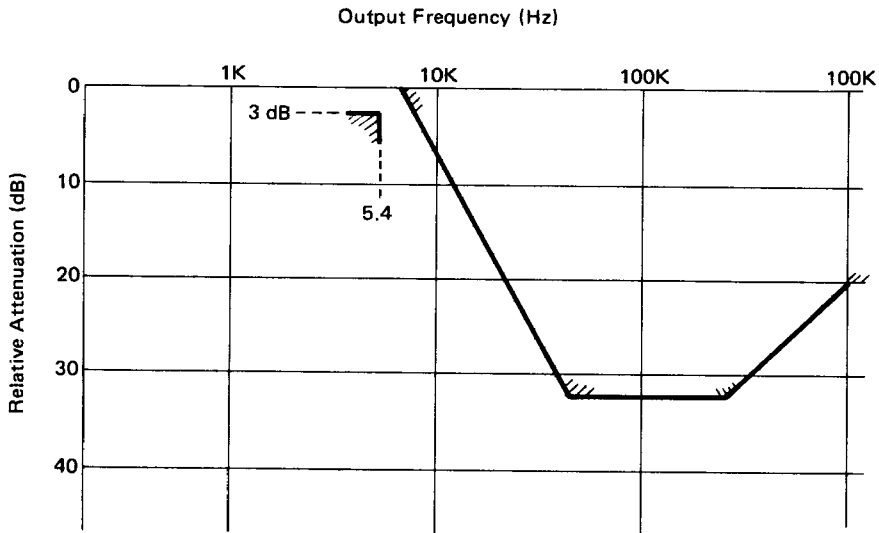


Figure 2 TSAT Frequency Characteristic

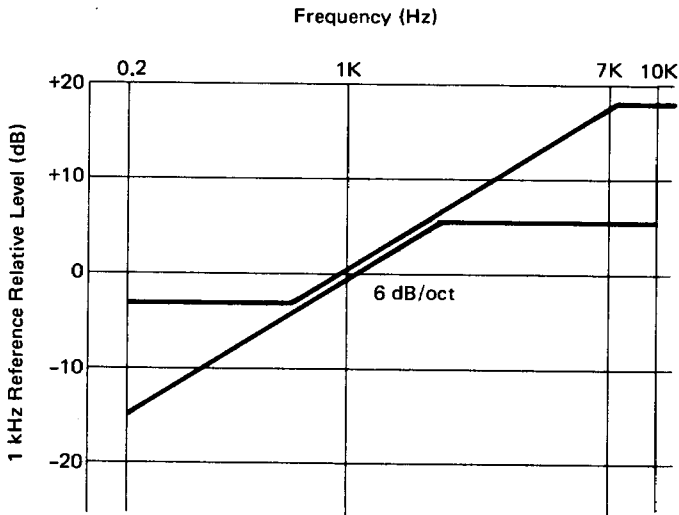


Figure 3 DTMF Emphasis Characteristic

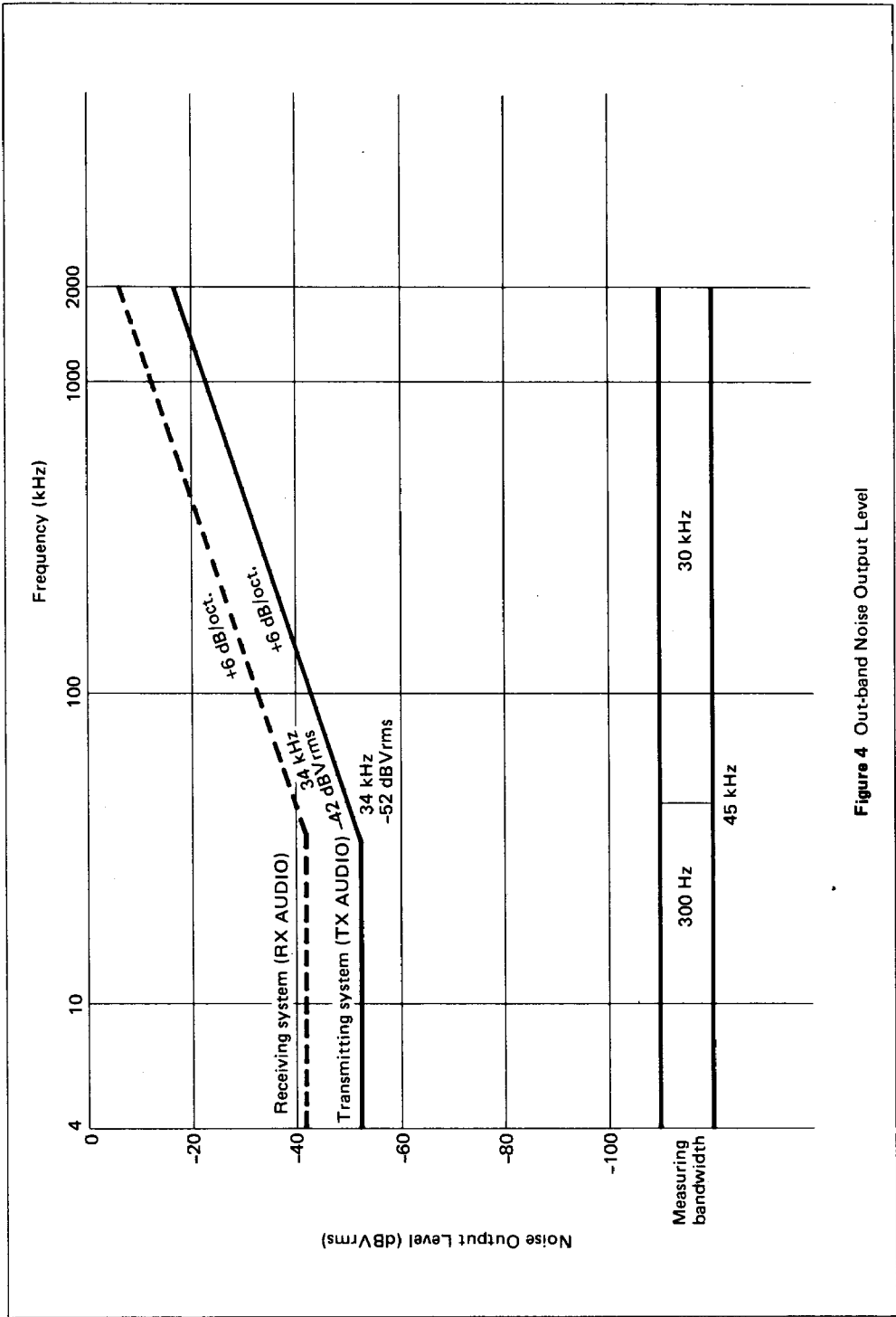
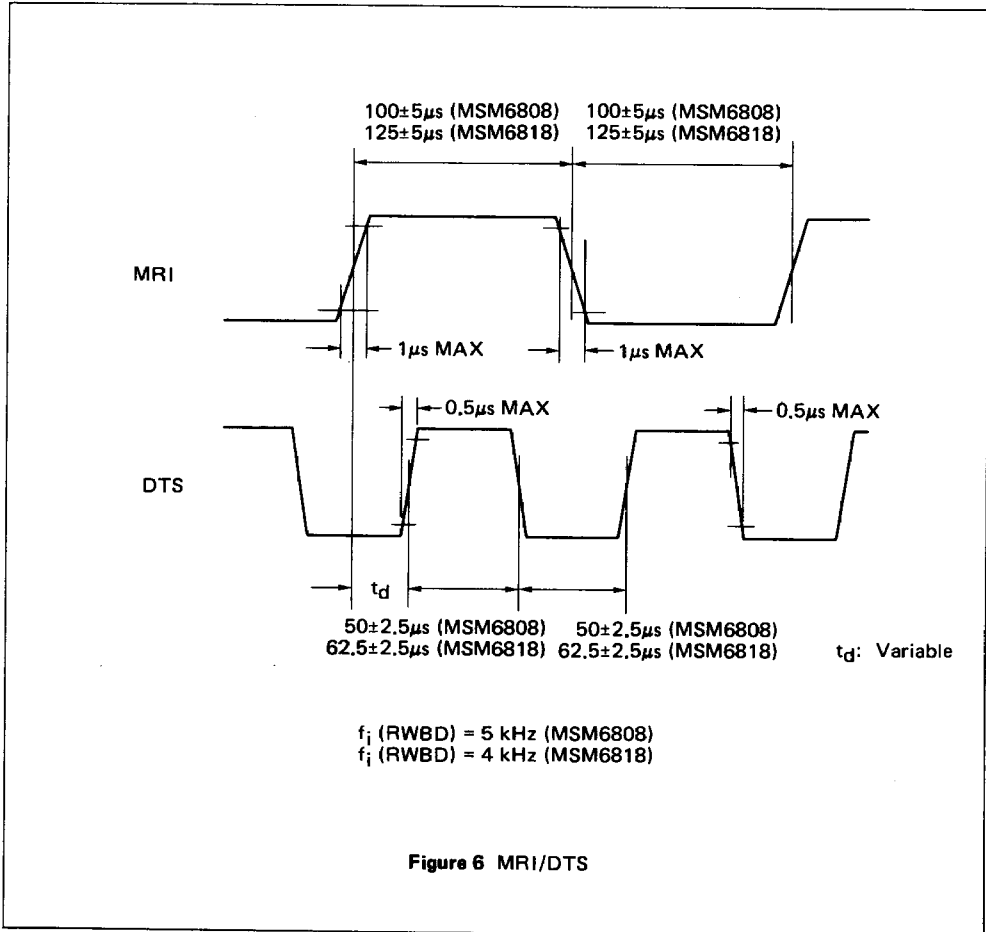
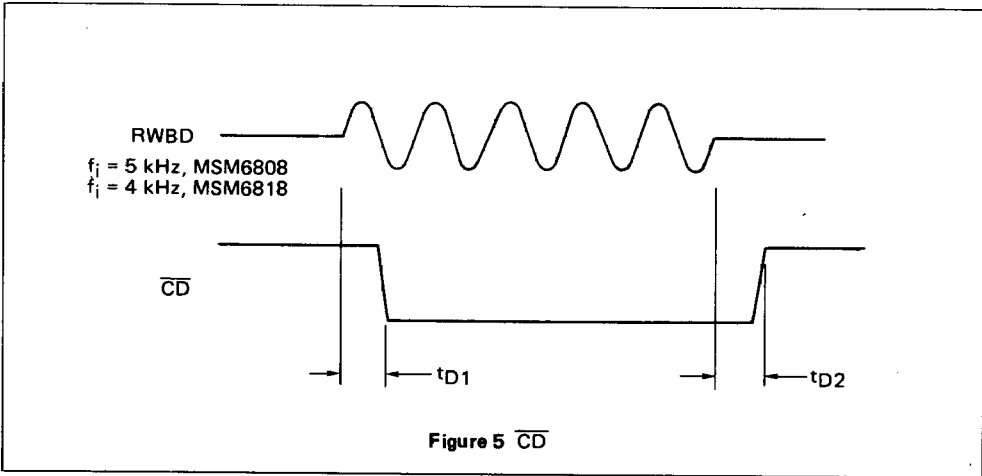
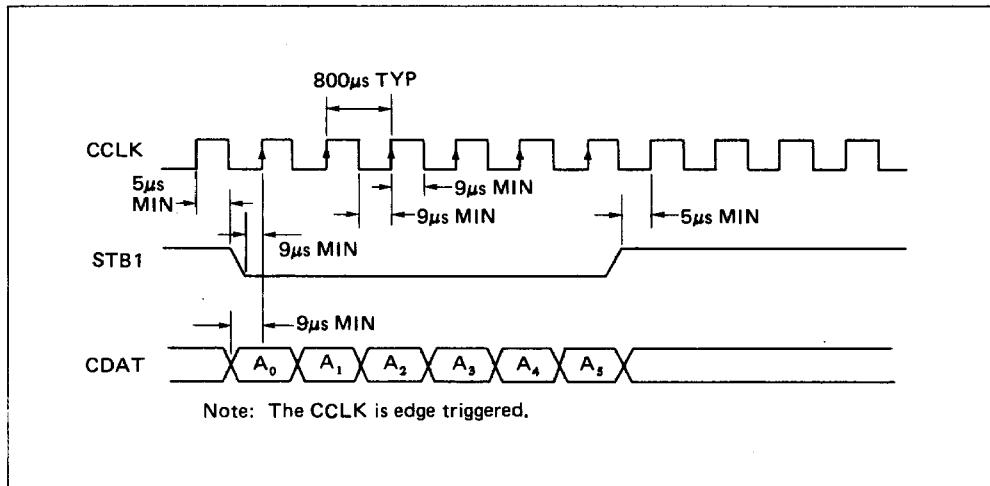


Figure 4 Out-band Noise Output Level



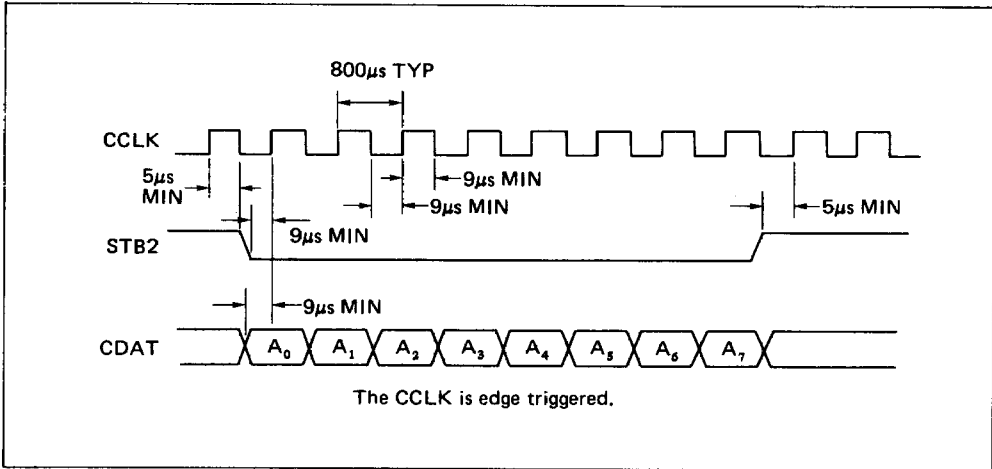
CONTROL PIN SPECIFICATIONS



Symbol	Name	Switch Status				
		RSIC, RSID Input DC Level		Switch Status		
A ₀	(DEMA, DEMB) (RSIA, RSIB) selection switch	RSIC > RSID	A0	A1	SW1	SW2
			L	L	0	0
			L	H	1	1
			H	L	1	1
A ₁	(DEMA, DEMB) (RSIA, RSIB) selection switch enable	RSIC < RSID	L	L	0	0
			L	H	0	0
			H	L	1	1
			H	H	0	0
		Control data	L:	Logic Low Level		
			H:	Logic High Level		
		Switch status "0", "1":	Refer to the block diagram			
A ₂	Data transmission enable	H: SW3 = "1", L: SW3 = "0"				
A ₃	SAT transponder enable	H: SW4 = "1", L: SW4 = "0"				
A ₄	DTMF transmission enable	H: SW5 = "1", L: SW5 = "0"				
A ₅	Side tone enable	H: SW6 = "1", L: SW6 = "0"				

Table 1

See the block diagram



A ₀	A ₁	A ₂	A ₃	A ₄	A ₅	A ₆	A ₇	Low Tone Frequency (Hz)	High Tone Frequency (Hz)	Remarks
0	0	0	x	x	x	x	x	697		
0	0	1	x	x	x	x	x	770		
0	1	0	x	x	x	x	x	852		
0	1	1	x	x	x	x	x	941		
1	0	0	x	x	x	x	x			A ₆ = H: Low tone on
1	0	1	x	x	x	x	x			L: Low tone off
1	1	0	x	x	x	x	x			
1	1	1	x	x	x	x	x			
x	x	x	0	0	0	x	x		1209	A ₇ = H: High tone on
x	x	x	0	0	1	x	x		1336	
x	x	x	0	1	0	x	x		1477	L: High tone on
x	x	x	0	1	1	x	x		1633	
x	x	x	1	0	0	x	x		2016	
x	x	x	1	0	1	x	x			
x	x	x	1	1	0	x	x			
x	x	x	1	1	1	x	x			

Table 2

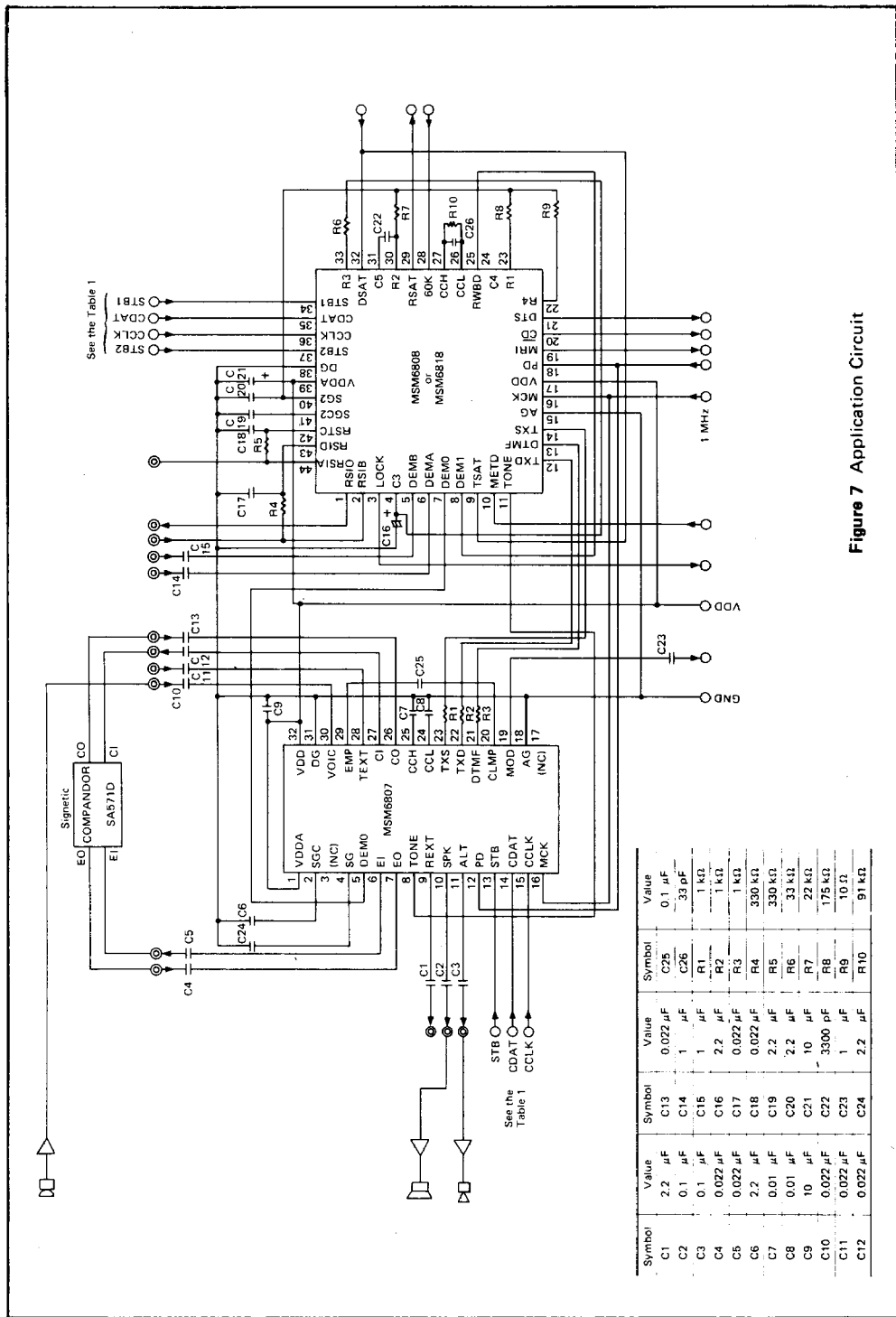


Figure 7 Application Circuit

Symbol	Value	Symbol	Value	Symbol	Value
C1	2.2 μ F	C13	0.022 μ F	C25	0.1 μ F
C2	0.1 μ F	C14	1 μ F	C26	33 pF
C3	0.1 μ F	C15	1 μ F	R1	1 k Ω
C4	0.022 μ F	C16	2.2 μ F	R2	1 k Ω
C5	0.022 μ F	C17	0.022 μ F	R3	1 k Ω
C6	2.2 μ F	C18	0.022 μ F	R4	330 k Ω
C7	0.01 μ F	C19	2.2 μ F	R5	330 k Ω
C8	0.01 μ F	C20	2.2 μ F	R6	33 k Ω
C9	10 μ F	C21	10 μ F	R7	22 k Ω
C10	0.022 μ F	C22	3300 pF	R8	175 k Ω
C11	0.022 μ F	C23	1 μ F	R9	10 Ω
C12	0.022 μ F	C24	2.2 μ F	R10	91 k Ω