MSM6807

BASEBAND FILTER LSI FOR CELLULAR MOBILE TELEPHONE

GENERAL DESCRIPTION

The MSM6807 performs the baseband filtering function for PM transmitter/receiver in the cellular mobile telephone.

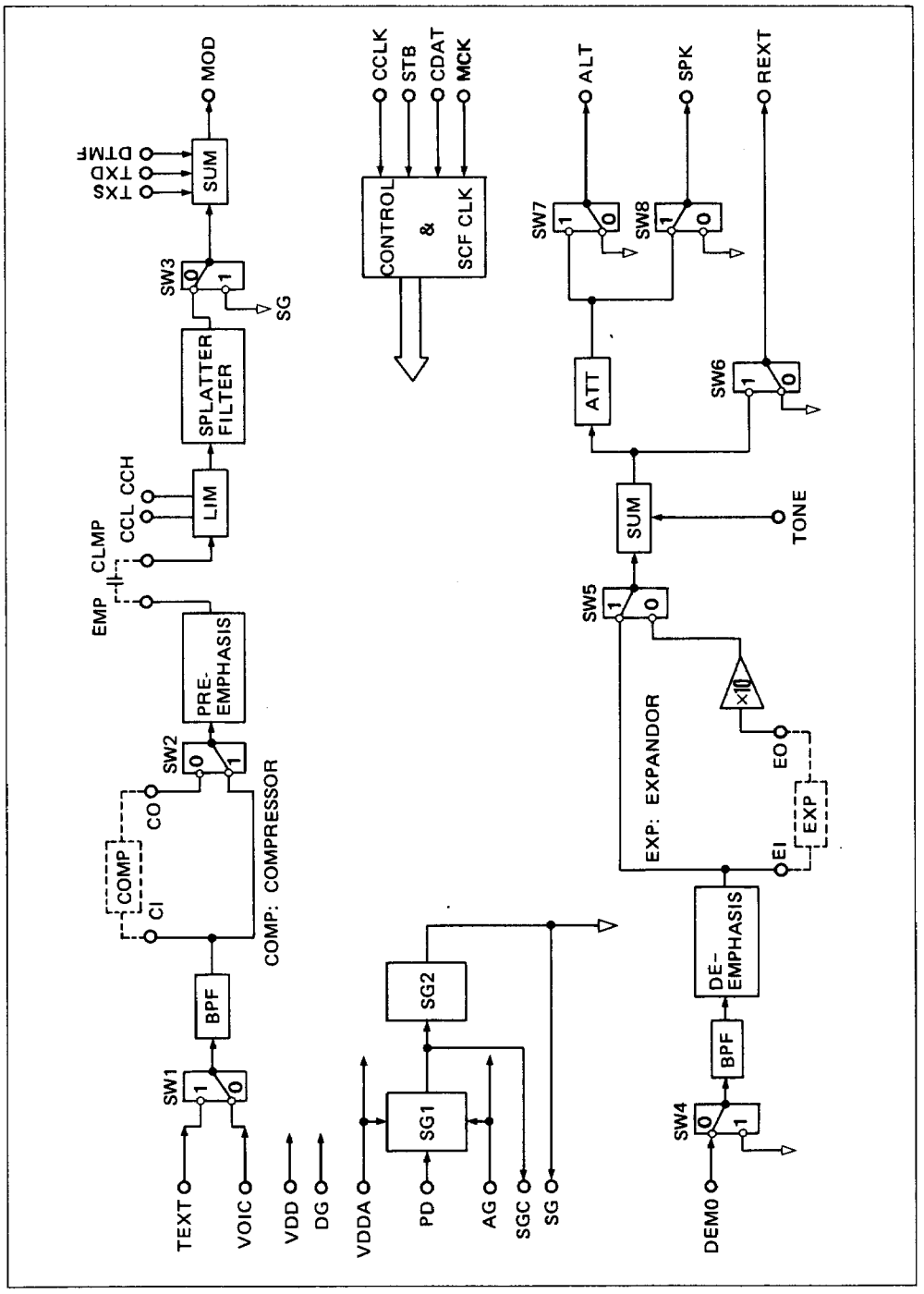
MSM6807 consists of a voice band-pass filter, pre-emphasis and de-emphasis circuit, a deviation limitter, a splatter filter, a receiver volume control attenuator, and a muting circuit and is fabricated by OKI's low power consumption CMOS silicon gate technology.

MSM6807 realizes the baseband filtering for AMPS (Advanced Mobile Phone Service) system.

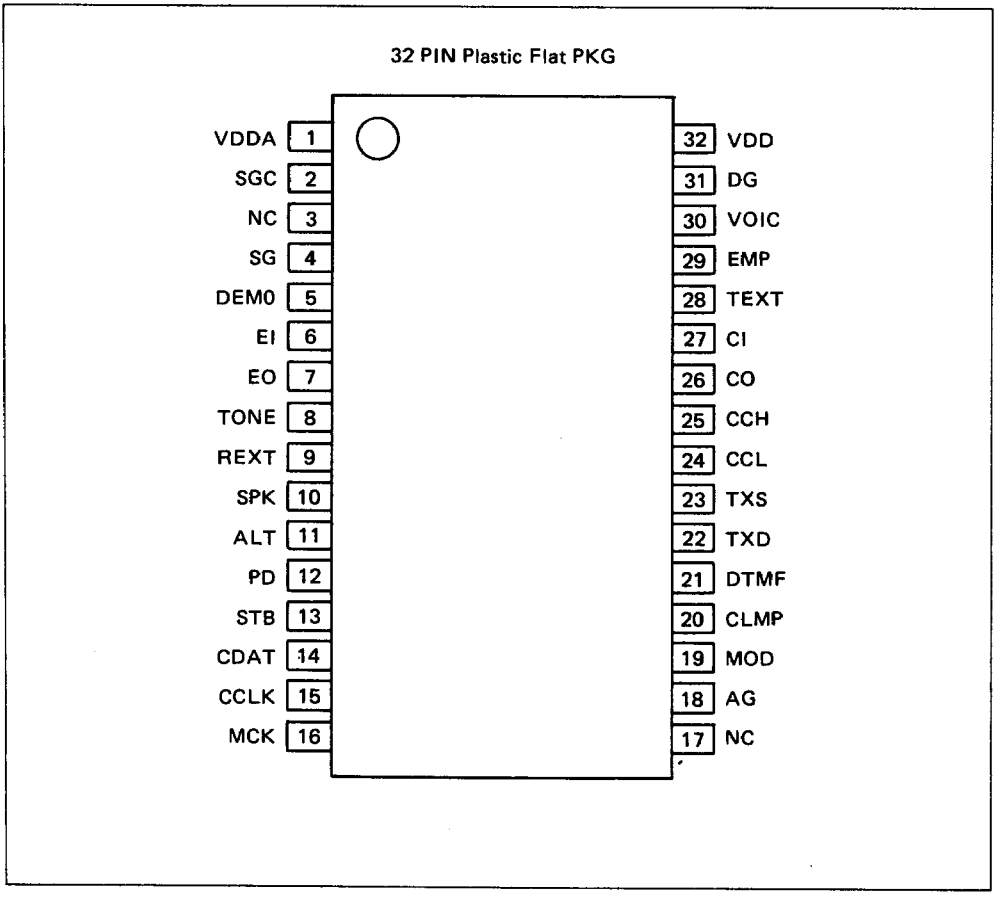
FEATURES

- Built-in mixing amplifier for transmitting MODEM data and DTMF signals.
- Built-in anti-aliasing filter and smoothing filter.
- Pre-emphasis, de-emphasis circuit on chip.
- Microcomputer interface serial control data.
- CMOS sillicon gate process.
- Power supply: +5V.
- Low power consumption: 30 mW.
- 32 pin plastic FLAT package.

BLOCK DIAGRAM

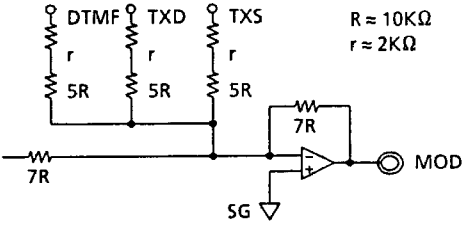


PIN CONFIGURATION



PIN DESCRIPTIONS

Pin Name	Pin No.	I/O	Function
VDDA	1	Power	Power supply pin for the analog circuit. +5V shall be applied.
SGC	2	O	This is the voltage reference for SG and is obtained by two-equal resistors division between VDDA and AG. It is necessary to be AC grounded for AG via a bypass capacitor of more than 2.2 μF so as to keep SG silent.
SG	4	O	SG is built-in analog ground. This voltage is nearly $\frac{VDDA}{2}$ V. To make its impedance lower, it is necessary to be AC grounded for AG via a bypass capacitor of more than 2.2 μF.
DEM0	5	I	Demodulated signals input. The demodulated baseband signal input to DEM0 can be sent out via ALT, SPK, REXT and EI.
EI	6	O	Expandor Input. When the control data B0 (refer to table 1) is logical 0, the transmitting circuit shall include the expandor portion of a 2:1 compandor. For every 1 dB change in input level to a 1:2 expandor, the change in output level is 2 dB. See Figure 6.
EO	7	I	Expandor Output. The signal input to EO has 20 dB gain between EO and SUM. Refer to description of pin 6 for details.
TONE	8	I	This is an input to SUM (Summing Amplifier) in the received audio line. In an application, DTMF SIDE TONE signal shall be injected. When not used, connect this pin to SG.
REXT	9	O	These are received analog outputs. The REXT, SPK and ALT are selective. One of three outputs is available at any one time. The ALT and SPK output level can be adjusted by the CDAT. See Table 1.
SPK	10	O	
ALT	11	O	
PD	12	I	Power Down function enable pin. A logical 0 enables the power down function.

Pin Name	Pin No.	I/O	Function
STB	13	I	Strobe signal. STB, CDAT and CCLK control the status of internal switches, and attenuation of output level through ALT, SPK. See Table 1 for an explanation of how these control signals shall be set at.
CDAT	14	I	Control Data. Refer to the description of pin 13 for details.
CCLK	15	I	Control Clock. Refer to the description of pin 13 for details.
MCK	16	I	Master Clock. The MCK pin must be injected with a 1 MHz (±0.01%) input signal.
AG	18	Power	Analog Ground. This pin should be common with DG at the point which is as close as possible to the system ground.
MOD	19	O	Transmitting Modulated analog signals output. When the B1 bit of CDAT is logical 1, the input of SUM is connected to SG.
CLMP	20	I	LIM input. This pin should be connected to EMP through a capacitor.
DTMF	21	I	These are inputs to SUM in the transmitting line. The internal circuit is as follows.  These pins shall be connected with SG when these are not used. The value of R is about 70 kΩ.
TXD	22	I	
TXS	23	I	
CCL	24	I	This is an input pin for Deviation Limitter cramp level (low level). When any reference voltage is not supplied to this pin, a built-in reference voltage (-.375V with respect to SG) will be supplied to the Limitter. In this case, it is necessary to be AC grounded for AG via a bypass capacitor. In addition, the cramp level can be adjusted by supplying an external reference voltage. See Figure 5.

Pin Name	Pin No.	I/O	Function
CCH	25	I	This is an input pin for Deviation Limitter cramp level (high level). A built-in reference shows +.375V with respect to SG. Refer to the description about CCL.
CO	26	I	Compressor Output. When the control data B0 (refer to Table 1) is logical 0, the receive circuit shall include the compressor portion of a 2:1 compandor. For every 2 dB change in input level to a 2:1 compressor, the change in output level is 1 dB. See Figure 6.
CI	27	O	Compressor Input. Refer to the description about pin 26 for details.
TEXT	28	I	Tone External. Transmit baseband signals input. As TEXT is biased internally to SG with a resistor (200 kΩ), the interface must be implemented by AC-coupling.
EMP	29	O	Emphasis Output. Refer to the description about pin 20.
VOIC	30	I	Transmitting baseband signals input. Refer to the description about pin 28 for detials.
DG	31	Power	Digital Ground. This pin should be common with AG at the point which is as close as possible to the system ground.
VDD	32	Power	Power supply pin for the digital circuit. +5 V shall be supplied to this pin.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Type	Max	Unit
Power Supply Voltage	V_{DD} V_{DDA}	T_a = +25°C With respect to AG or DG	-0.3	—	7	V
Analog Input Voltage*1	V_{IA}		-0.3	—	V_{DDA} +0.3	
Digital Input Voltage*2	V_{ID}		-0.3	—	V_{DD} +0.3	
Operating Temperature	T_{op}	—	-40	—	85	°C
Storage Temperature	T_{stg}		-55	—	125	

*1 TEXT, VOIC, DEM0, TONE, CLMP, TXS, TXD, DTMF
*2 CCLK, STB, CDAT, MCK, PD

Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power supply Voltage	V_{DD} V_{DDA}	With respect to AG or DG	4.75	5.0	5.25	V
Operating Temperature	T_{op}		-30	—	70	°C
Master Clock Frequency	f_{MCK}		0.9999	1	1.0001	MHz

DC AND DIGITAL INTERFACE CHARACTERISTICS

V_{DDA}, V_{DD} = 5V ±5%, T_a = -30 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Power Dissipation (standby)	I_{DD}	—	—	7	14	mA	—
	I_{DDS}		—	0.2	0.5		
Input Leak Current	I_{IL}	V_I = 0V	-10	—	10	μA	CCLK CDAT STB MCK PD
	I_{IH}	V_I = V_{DD}	-10	—	10		
Input Voltage	V_{IL}	—	0	—	0.3 V_{DD}	V	
	V_{IH}		0.7 V_{DD}	—	V_{DD}		

ANALOG INTERFACE CHARACTERISTICS

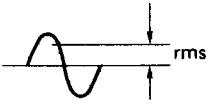
V_{DDA}, V_{DD} = 5V ±5%, T_a = -30 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Input Impedance	R_I	f ≦ 4 KHz	100	–	–	kΩ	*1
Deviation Limitter Cramp Level	V_{CCL}	V_{DDA} = 5 V With respect to SG	–	+0.375	–	V	CCL
	V_{CCH}		–	-0.375	–		CCH

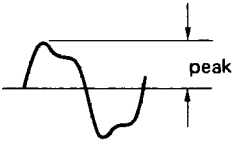
*1 TEXT, VOIC, DEM0, EO, CO, TONE, CLMP

Definitions of Units

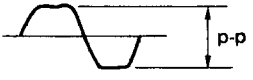
dBV_{rms} : 20*logV, where V denotes the root mean square value of the signal voltage.



dBVp : 20*logV, where V denotes the peak value of the signal voltage.



Vp-p : Peak-peak value of the signal voltage.



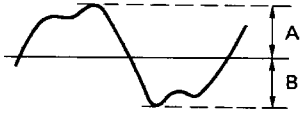
TRANSMIT CHARACTERISTICS (MOD)

V_{DDA}, V_{DD} = 5V ±5%, T_a = -30 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
VOIC/TEXT Standard Deviation Input Level	V_{ITX}	Vo (MOD) =-8.2 dBVp fi=1 kHz	–	-11.2	–	dBVrms	
MOD Standard Deviation Distortion	D_{MOD}		–	–	-26	dB	SW2="1"
MOD MAX Deviation Output Level	V_{OTX}	Vi (VOIC) =0 dBVrms fi=1 kHz	–	–	-6	dBVp	SW3="0"
MOD Output Signal Peak Ratio*1	V_{SYM}		-5	–	-5	%	
TX-AUDIO Muting Attenuation	L_{TXM}	Vi (VOIC) =-11.2 dBVrms fi=1 kHz	40	–	–	dB	SW3="0" → "1"
TX-AUDIO BPF Characteristics	–	–	–	Figure 1	–	–	CI
TX-AUDIO Overall Response	–	–	–	Figure 2	–	–	MOD SW2="1" SW3="0"
MOD In-band Noise Level	–	0.3~3 kHz CMESS filter	–	–	-62	dBVrms	SW2="1"
MOD Out-band Noise Level	–	VOIC/TEXT silent	–	Figure 4	–	–	

*1 MOD output signal (after DC cutting)

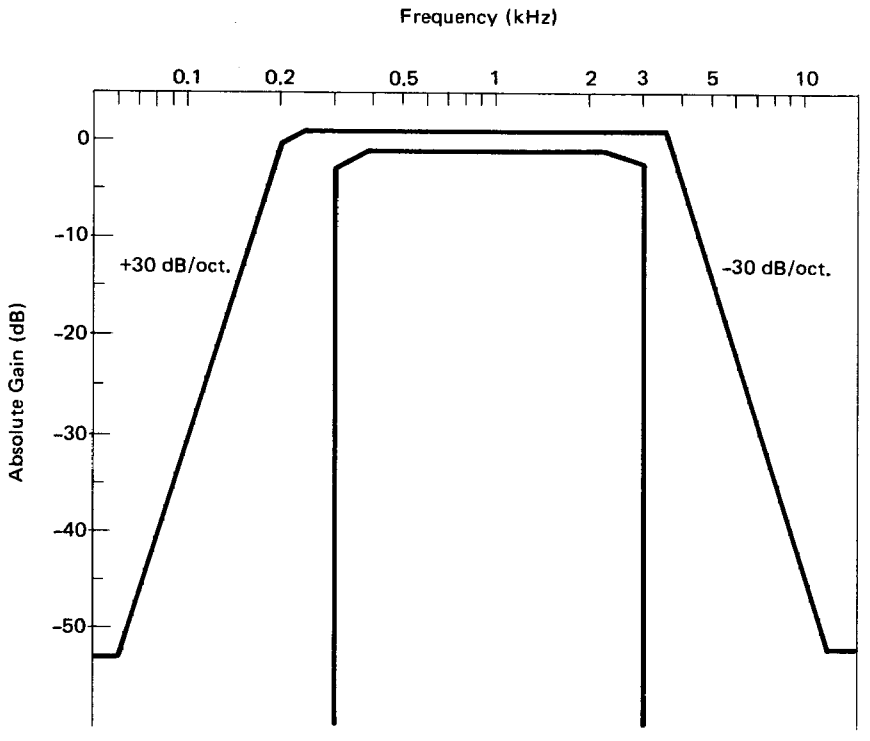
100*(A/B-1) ; (%)



RECEIVE CHARACTERISTICS (ALT/SPK/REXT)

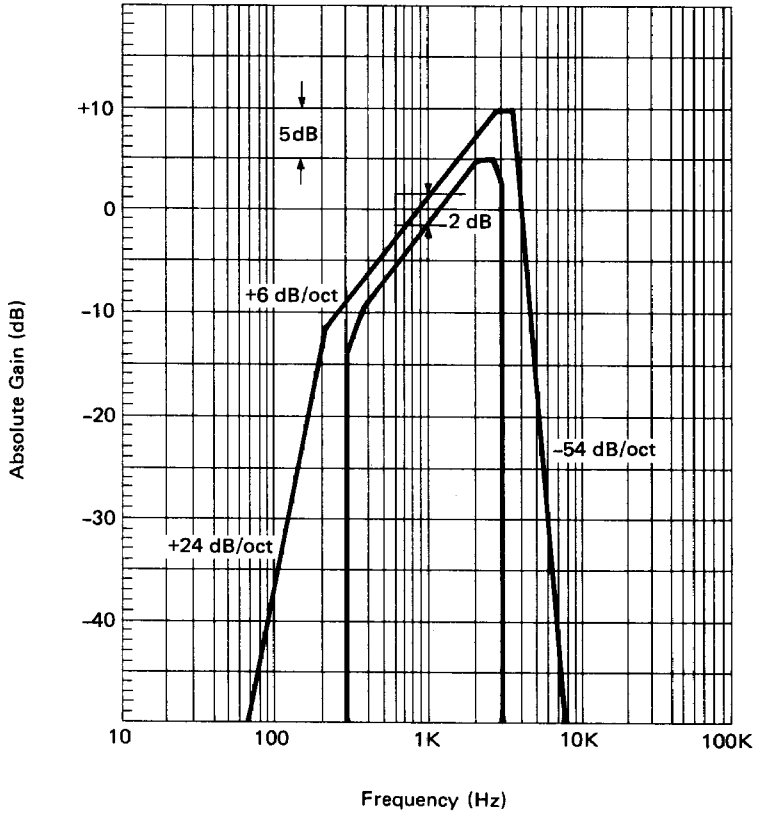
V_{DDA}, V_{DD} = 5V ±5%, T_a = -30 ~ 70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
ALT/SPK/REXT Standard Demodulation Output Level	V_{ORX}	Vi (DEM0) =-11.2 dBVrms fi=1 kHz ATT=0 dB	–	-11.2	–	dBVrms	SW5="1"
ALT/SPK/REXT Output Distortion	D_R		–	–	-40	dB	
ATT Attenuation Step	G_{ATT}	–	–	2.5	–	dB	
RX-AUDIO Overall Response	–	–	–	Figure 3	–	–	
ALT/SPK/REXT In-band Noise Level	–	CMESS filter 0.3 ~ 3.0 kHz	–	–	-62	dBVrms	
ALT/SPK/REXT Out-band Noise Level	–	–	–	Figure 4	–	–	



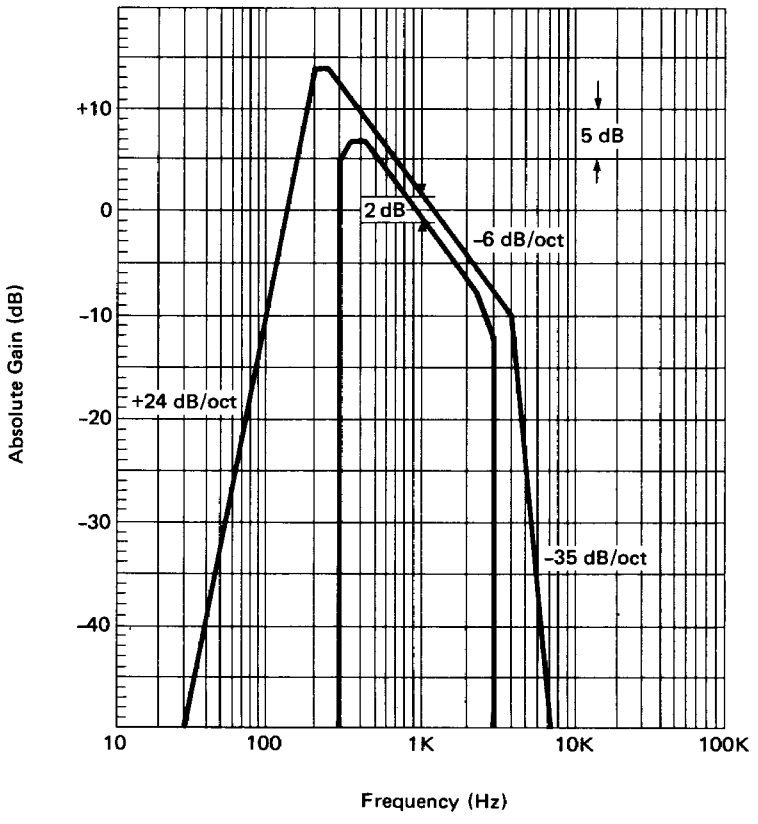
Upper Limits:	(1)	below 60 Hz	Less than	-53 dB
	(2)	200 Hz		-0.5 dB
	(3)	240 Hz		+1.0 dB
	(4)	240~3500 Hz		Flat
	(5)	above 12 kHz		-52 dB
Lower Limits:	(1)	300 Hz		-3 dB
	(2)	400 Hz		-1 dB
	(3)	400~2200 Hz		Flat
	(4)	3000 Hz		-2.6 dB

Figure 1 BPF Frequency Characteristics



Upper limits:	1	200 to 3000 Hz	: 6 dB/oct
	2	3000 to 3500 Hz	: Flat
Lower limits:	1	400 to 2250 Hz	: 2 dB below the upper limit line
	2	300 Hz	: 4.5 dB below 400 Hz
	3	2250 to 2500 Hz	: Flat
	4	3000 Hz	: 3 dB below 2500 Hz

Figure 2 TX-AUDIO Overall Response



Upper limits:	1	240 to 3800 Hz	: -6 dB/oct
	2	200 to 240 Hz	: Flat
Lower limits:	1	400 to 2250 Hz	: 2 dB below the upper limit line
	2	360 to 400 Hz	: Flat
	3	300 Hz	: 3 dB below 360 Hz
	4	3000 Hz	: 4.5 dB below 2250 Hz

Figure 3 RX-AUDIO Overall Response

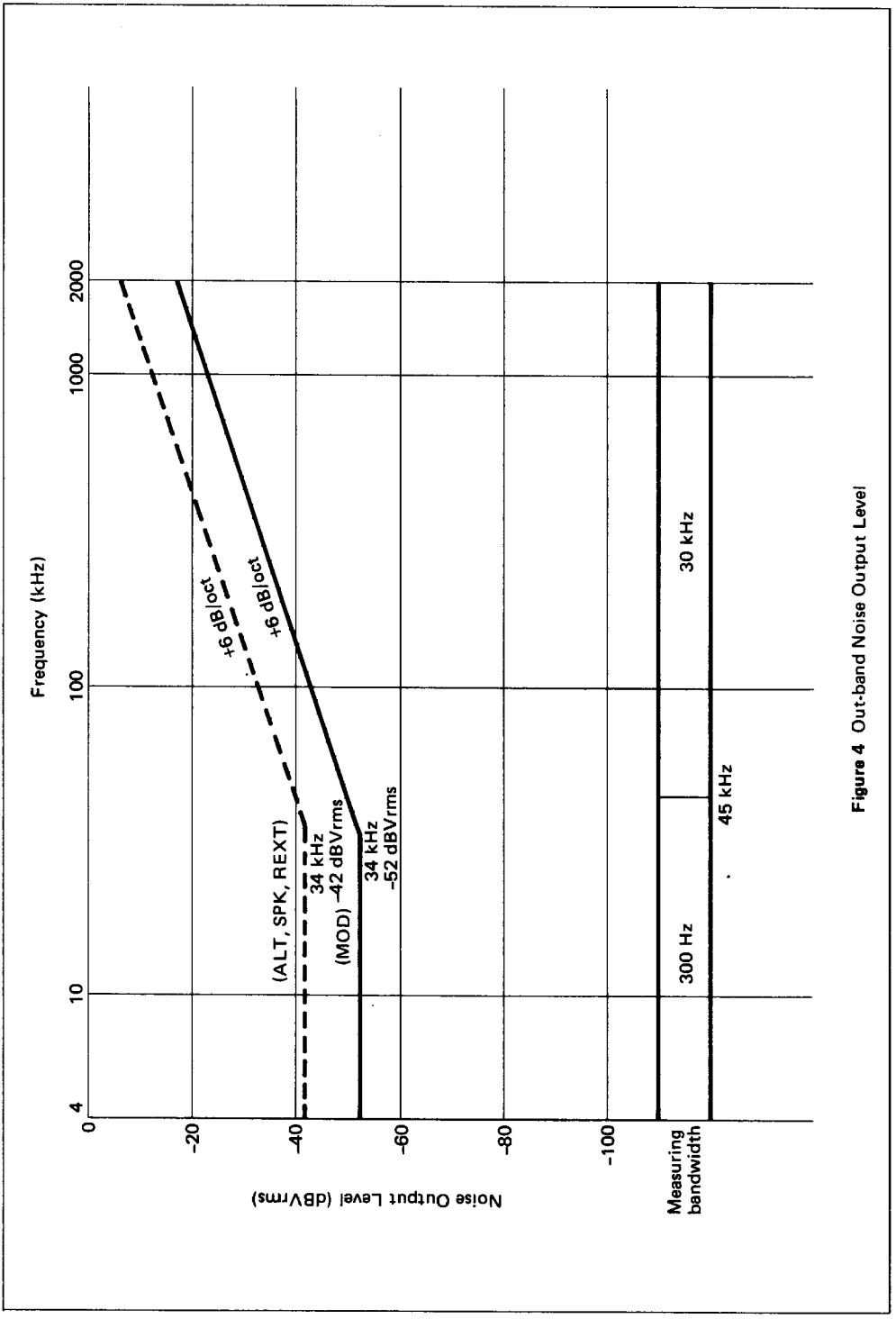
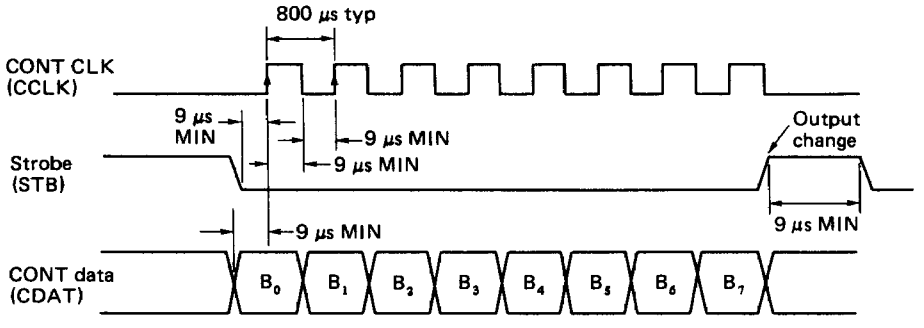


Figure 4 Out-band Noise Output Level

Control Pin Specifications



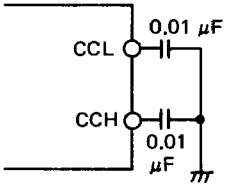
The CONT CLK (CCLK) is edge triggered.

Symbol	Name	Switch Status
B0	COMPANDOR selection	H: SW2 = "1", L: SW2 = "0" SW5 = "1", SW5 = "0"
B1	TX-AUDIO mute	H: SW3 = "1", L: SW3 = "0"
B2	RX-AUDIO mute	H: SW4 = "1", L: SW4 = "0"
B6	TEXT/VOIC selection	H: SW1 = "1", L: SW1 = "0"
B6, B7	ALT/SPK/REXT selection	B6 | B7 | output 1 | X | REXT 0 | 0 | SPK 0 | 1 | ALT X: Irrespective of 1/0.

ATT CONT			Attenuation (dB)
B5	B4	B3	
0	0	0	0
0	0	1	2.5
0	1	0	5
0	1	1	7.5
1	0	0	10
1	0	1	12.5
1	1	0	15
1	1	1	17.5

Table 1

Internal Reference Voltage



CCL = VDDA/2 - 0.375 (V)
CCH = VDDA/2 + 0.375 (V)

External Reference Voltage

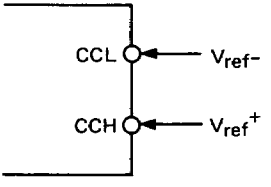


Figure 5 Deviation Limitter

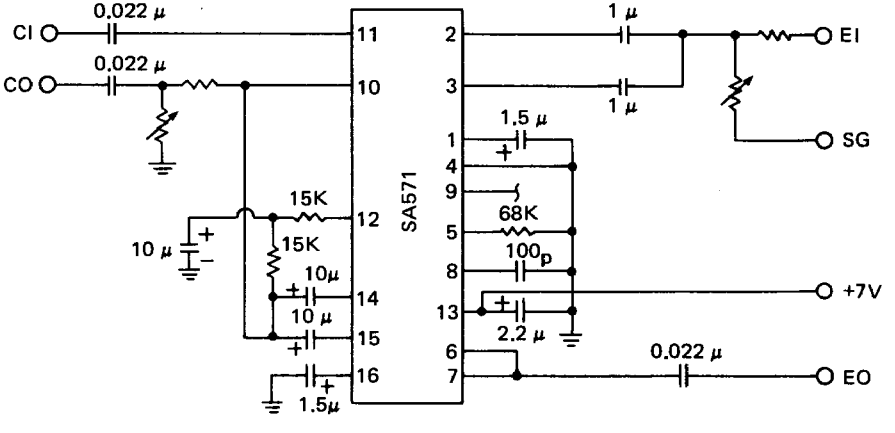
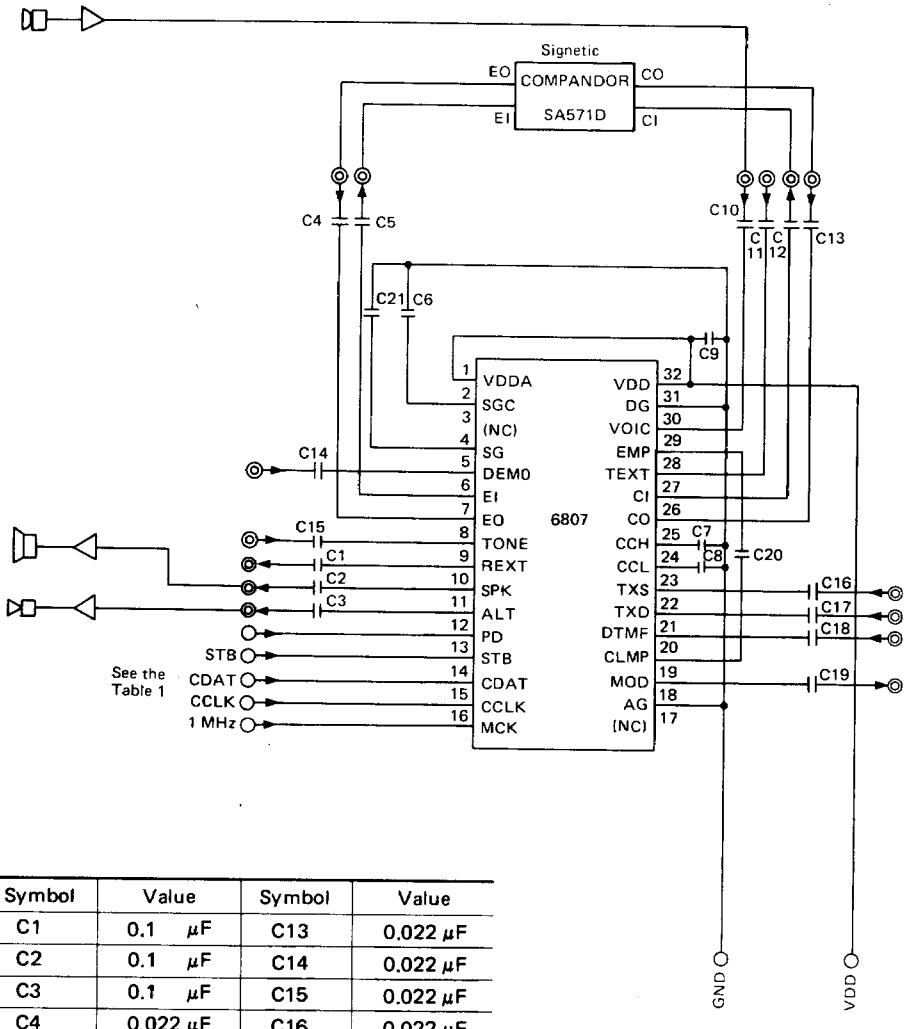


Figure 6 Compandor



Symbol	Value	Symbol	Value
C1	0.1 μF	C13	0.022 μF
C2	0.1 μF	C14	0.022 μF
C3	0.1 μF	C15	0.022 μF
C4	0.022 μF	C16	0.022 μF
C5	0.022 μF	C17	0.022 μF
C6	2.2 μF	C18	0.022 μF
C7	0.01 μF	C19	0.022 μF
C8	0.01 μF	C20	0.1 μF
C9	10 μF	C21	2.2 μF
C10	0.022 μF		
C11	0.022 μF		
C12	0.022 μF		

Figure 7 Application