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**MSM6669**

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**80-DOT LCD SEGMENT DRIVER**

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**GENERAL DESCRIPTION**

The MSM6669 is a dot matrix LCD segment driver which is fabricated using CMOS low power silicon gate technology.

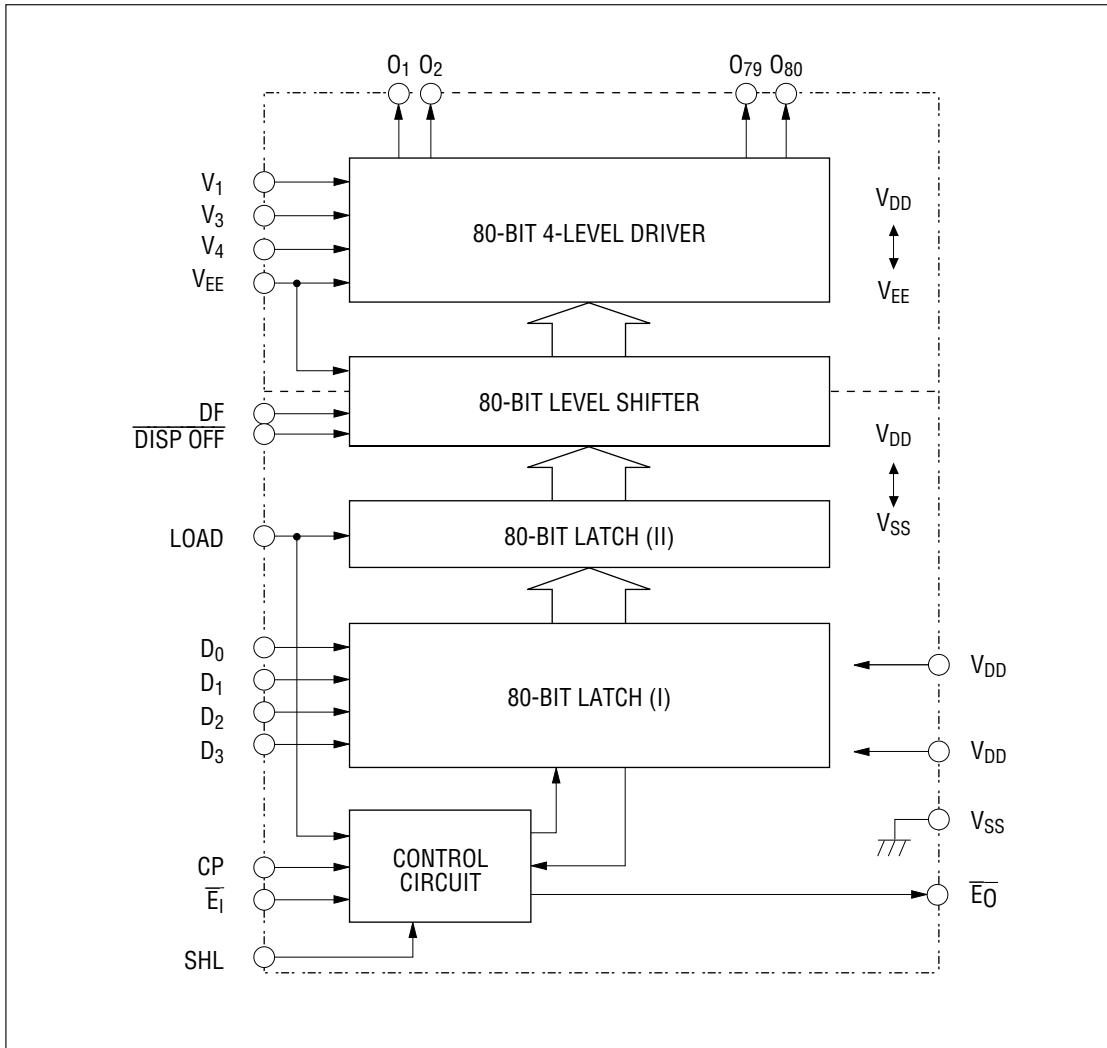
This LSI consists of 80-bit latches I and II, 80-bit level shifter, and 80-bit 4-level driver.

It latches the 4-bit parallel display data from the LCD controller LSI or microcontroller, and then outputs the signal for the LCD driving.

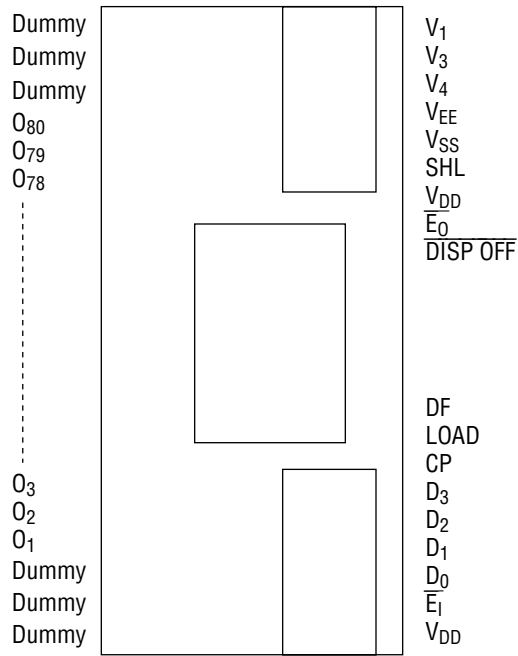
**FEATURES**

- Logic supply voltage : 2.7V to 5.5V
- LCD driving voltage : 14V to 28V
- Applicable LCD duty : 1/64 to 1/256
- Bias voltage can be supplied externally
- LCD output : 80
- 4-bit parallel data processing has improved the transfer speed to 1/4 that of the conventional serial transfer, thereby achieving low power consumption
- Applicable common driver : MSM6778 (120 outputs)
- Structure:
  - TCP mounting with 35mm wide film (Product name: MSM6669AV-Z-05)
  - Sn-plated
  - Outer lead pitch : 220 $\mu$ m
  - User area : 7.5mm

**BLOCK DIAGRAM**



**PIN CONFIGURATION (TOP VIEW)**



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	$V_{DD}$	$T_a=25^{\circ}\text{C}$	-0.3 to +6.5	V
Supply Voltage (2)	$V_{LCD}$	$T_a=25^{\circ}\text{C}, V_{DD} - V_{EE}^*$	0 to 30	V
Input Voltage	$V_I$	$T_a=25^{\circ}\text{C}$	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	$T_{STG}$	—	-30 to +85	$^{\circ}\text{C}$

\*  $V_1 > V_3 > V_4 > V_{EE}, V_{DD} \geq V_1 > V_3 \geq V_{DD} - 10\text{V}, V_{EE} + 10\text{V} \geq V_4 > V_{EE}$

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (1)	$V_{DD}$	—	2.7	5.0	5.5	V
Supply Voltage (2)	$V_{LCD}$	$V_{DD} - V_{EE}^*$	14	—	28	V
Operating Temperature	$T_{op}$	—	-20	—	75	$^{\circ}\text{C}$

\*  $V_1 > V_3 > V_4 > V_{EE}, V_{DD} \geq V_1 > V_3 \geq V_{DD} - 7\text{V}, V_{EE} + 7\text{V} \geq V_4 > V_{EE}$

**ELECTRICAL CHARACTERISTICS**

**DC Characteristics**

( $V_{DD} = 2.7$  to  $5.5V$ ,  $T_a = -20$  to  $+75^\circ C$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	$V_{IH}$ *1	—	$0.8 V_{DD}$	—	$V_{DD}$	V
"L" Input Voltage	$V_{IL}$ *1	—	—	—	$0.2 V_{DD}$	V
"H" Input Current	$I_{IH}$ *1	$V_{IH} = V_{DD}$	$V_{SS}$	—	1	$\mu A$
"L" Input Current	$I_{IL}$ *1	$V_{IL} = 0V$	—	—	-1	$\mu A$
"H" Output Voltage	$V_{OH}$ *2	$I_O = -0.2mA$	$V_{DD} - 0.4$	—	—	V
"L" Output Voltage	$V_{OL}$ *2	$I_O = 0.2mA$	—	—	0.4	V
On Resistance	$R_{ON}$ *4	$V_{DD} - V_{EE} = 25V$ $V_{DD} = 2.7V$ $ V_N - V_O  = 0.25V$ *3	—	1.5	3.0	$k\Omega$
Stand-by Current	$I_{DDSBY}$	$f_{CP} = 6.0MHz$ , $V_{DD} = 3.0V$ $V_{DD} - V_{EE} = 25V$ No load, $f_{LOAD} = 21.6kHz$ *5	—	—	0.3	mA
Supply Current (1)	$I_{DD1}$	$f_{CP} = 6.0MHz$ , $V_{DD} = 3.0V$ $V_{DD} - V_{EE} = 25V$ No load, $f_{LOAD} = 21.6kHz$ *6	—	—	$1.5 (V_{DD})$ $1.0 (V_{EE})$	mA
Supply Current (2)	$I_V$	$f_{CP} = 6.0MHz$ , $V_{DD} = 3.0V$ $V_{DD} - V_{EE} = 25V$ No load, $f_{LOAD} = 21.6kHz$ *7	—	—	100	$\mu A$
Input Capacitance	$C_I$	$f = 1MHz$	—	5	—	$\mu F$

\*1 Applicable to  $\overline{LOAD}$ , CP, D<sub>0</sub> to D<sub>3</sub>,  $\overline{E_1}$ , DF,  $\overline{DISP OFF}$  pins.

\*2 Applicable to  $\overline{E_0}$  pin.

\*3  $V_N = V_1$  to  $V_{EE}$ ,  $V_4 = 14/16 (V_{DD} - V_{EE})$ ,  $V_3 = 2/16 (V_{DD} - V_{EE})$ ,  $V_{DD} = V_1$ .

\*4 Applicable to O<sub>1</sub> to O<sub>80</sub> pins.

\*5 Display data 1010,  $f_{DF} = 45Hz$ , current that flows from  $V_{DD}$  to  $V_{SS}$  when the display data is not clocked in.

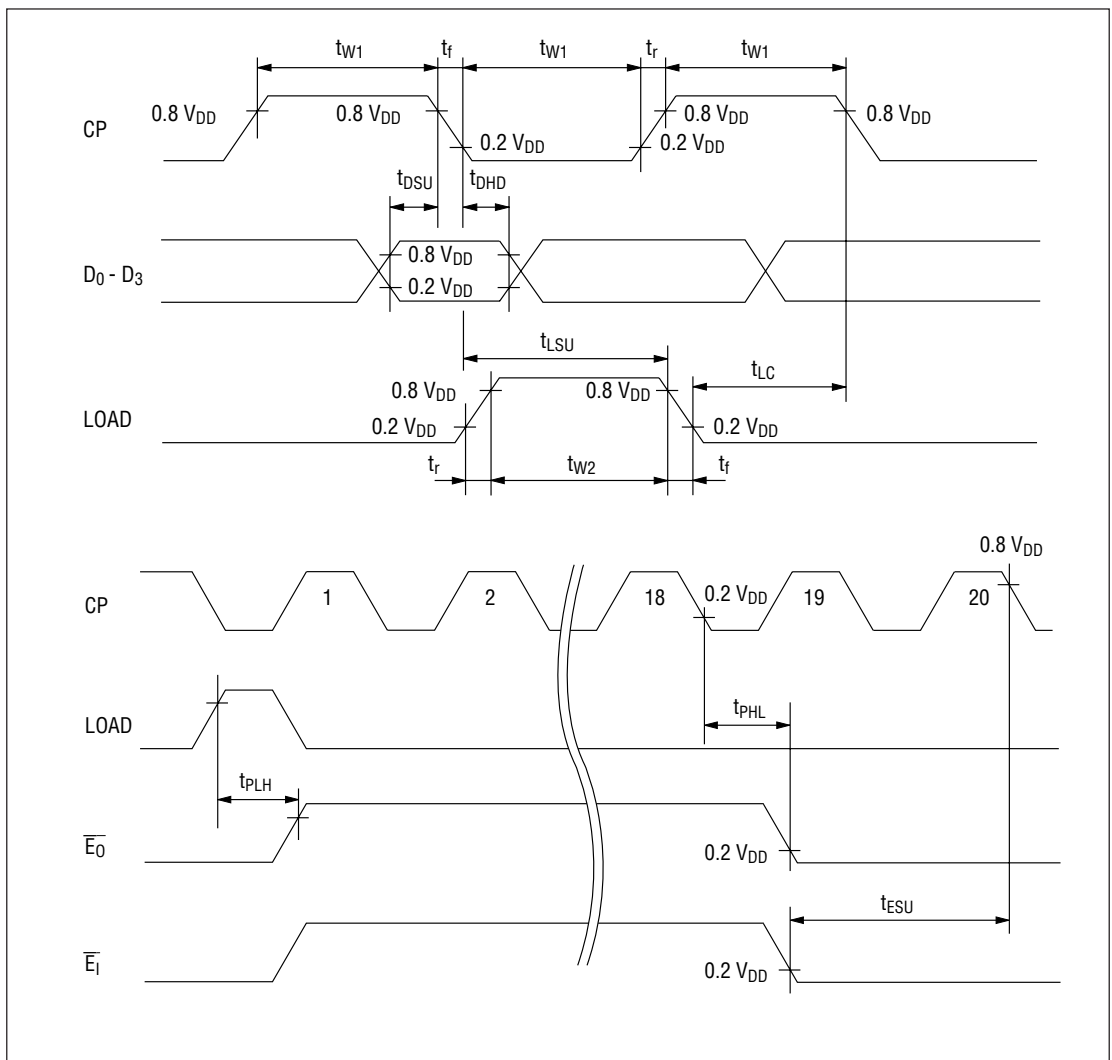
\*6 Display data 1010,  $f_{DF} = 45Hz$ , current ( $V_{DD}$ ) that flows from  $V_{DD}$  to  $V_{SS}$  and  $V_{EE}$ , and current ( $V_{EE}$ ) that flows from  $V_{DD}$  to  $V_{EE}$  when the display data is clocked in.

\*7 Display data 1010,  $f_{DF} = 45Hz$ , current that flows to each of the  $V_1$ ,  $V_3$  and  $V_4$  pins.

Switching Characteristics

( $V_{DD} = 2.7$  to  $5.5V$ ,  $T_a = -20$  to  $+75^\circ C$ ,  $C_L = 15pF$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency	$f_{CP}$	Duty = 50%	—	—	6.5	MHz
Clock Pulse Width	$t_{W1}$	—	56	—	—	ns
Rise/Fall Time	$t_r, t_f$	—	—	—	20	ns
Data Setup Time	$t_{DSU}$	—	50	—	—	ns
Data Hold Time	$t_{DHD}$	—	50	—	—	ns
Load Pulse Width	$t_{W2}$	—	70	—	—	ns
Load Setup Time	$t_{LSU}$	—	80	—	—	ns
Load → Clock Time	$t_{LC}$	—	80	—	—	ns
"H", "L" Propagation Delay Time	$t_{PLH}$ $t_{PHL}$	—	—	—	236	ns
$\bar{E}_1$ Setup Time	$t_{ESU}$	—	50	—	—	ns



## FUNCTIONAL DESCRIPTION

### Pin Functional Description

- **$\overline{E}_I, \overline{E}_O$**   
These are enable signal input and output pins. When a cascade connection is required, set the first MSM6669's  $\overline{E}_I$  pin at "L" level and connect the  $\overline{E}_O$  pin to the next MSM6669's  $\overline{E}_I$  pin. When a single MSM6669 is used,  $\overline{E}_I$  should be set at "L" level.
- **CP**  
This is a pin for clocking the display data in. Display data is stored into the latch (I) at the falling edge of a clock pulse. A clock pulse through this pin is enabled when the enable F/F is set, and disabled when it is not set.
- **LOAD**  
This is an input pin to latch the display data of one line stored in the latch (I). At the falling edge of a load pulse, the display data stored in the latch (I) is transferred to the latch (II). The control circuit to save the power is reset and the display data on the next line can be stored.
- **DF**  
Synchronous signal input pin for alternate signal for LCD driving.
- **$V_{DD}, V_{SS}$**   
These are power supply pins of this IC. The  $V_{DD}$  pin is generally set to 2.7 to 5.5V.  $V_{SS}$  is a grounding pin, which is generally set to 0V.
- **O1 to O80**  
These are output pins of the 4-level driver of this IC, which correspond directly to the bits of the 80-bit latch (II). One of the four levels  $V_1, V_3, V_4,$  and  $V_{EE}$  is selected and output by a combination of the latch contents (display data) and a DF signal. See the truth table. Connect the output pins to the liquid crystal panel on the segment side.
- **$\overline{DISP OFF}$**   
This is an input pin to control the output pins  $O_1$  to  $O_{80}$ . During low signal input, signals on the  $V_1$  level are output from the output pins  $O_1$  to  $O_{80}$  irrespective of display data. See the truth table.





- **V<sub>1</sub>, V<sub>3</sub>, V<sub>4</sub>, V<sub>EE</sub>**

Bias supply voltage pins to drive the LCD. Bias voltages for the LCD driving are supplied from an external source.

### Truth Table

DF	Latch Data	$\overline{\text{DISP OFF}}$	Driver Output Level (O <sub>1</sub> - O <sub>80</sub> )
L	L	H	V <sub>3</sub>
L	H	H	V <sub>1</sub>
H	L	H	V <sub>4</sub>
H	H	H	V <sub>EE</sub>
X	X	L	V <sub>1</sub>

X: Don't care

### NOTES ON USE

Note the following when turning power on and off:

The LCD drivers of this IC require a high voltage. For this reason, if a high voltage is applied to the LCD drivers with the logic power supply floating, excess current flows. This may damage the IC. Be sure to carry out the following power-on and power-off sequences:

When turning power on:

First V<sub>DD</sub> ON, next V<sub>EE</sub>, V<sub>4</sub>, V<sub>3</sub>, V<sub>1</sub> ON. Or both ON at the same time.

When turning power off:

First V<sub>EE</sub>, V<sub>4</sub>, V<sub>3</sub>, V<sub>1</sub> OFF, next V<sub>DD</sub> OFF. Or both OFF at the same time.