The MRFIC Line

1.8 GHz LNA/Downmixer

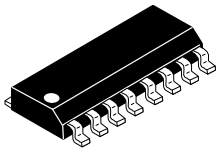
MRFIC1804

1.8 GHz LOW NOISE AMPLIFIER AND DOWNMIXER GaAs MONOLITHIC INTEGRATED CIRCUIT

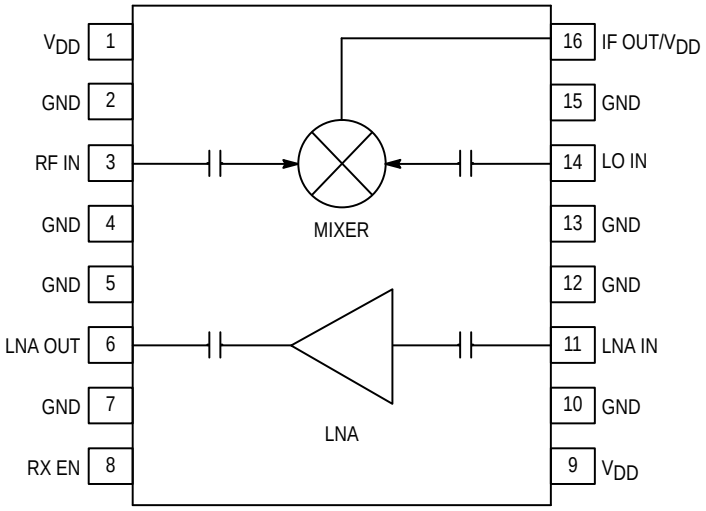
Designed primarily for use in DECT, Japan Personal Handy Phone (JPHP), and other wireless Personal Communication Systems (PCS) applications. The MRFIC1804 includes a low noise amplifier and downmixer in a low-cost SOIC-16 package. The integrated circuit requires minimal off-chip matching while allowing for the maximum in flexibility and efficiency. The mixer is optimized for low side injection and offers reasonable intercept point as well as high efficiency and 4 dB of conversion gain. Image filtering is implemented off-chip to allow maximum flexibility. With both TX and RX enable pins low, the device is in standby mode and draws less than 0.5 mA.

Together with the rest of the MRFIC180X series, this GaAs IC family offers the complete transmit and receive functions, less LO and filters, needed for a typical 1.8 GHz cordless telephone.

- Usable Frequency Range = 1.5 to 2.2 GHz
- 14 dB Gain, 2.3 dB Noise Figure LNA
- 4 dB Gain, 13 dB Noise Figure Mixer
- 0.9 dB Mixer Input Intercept Point
- Simple LO/IF Off-Chip Matching for Maximum Flexibility
- Low Power Consumption = 24 mW (Typ)
- Single Bias Supply = 2.7 to 3.3 V
- Low LO Power Requirement = – 5 dBm (Typ)
- Low Cost Surface Mount Plastic Package
- Available in Tape and Reel by Adding R2 Suffix to Part Number.
  R2 Suffix = 2,500 Units per 16 mm, 13 inch Reel.
- Device Marking = M1804



CASE 751B-05
(SO–16)



Pin Connections and Functional Block Diagram

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

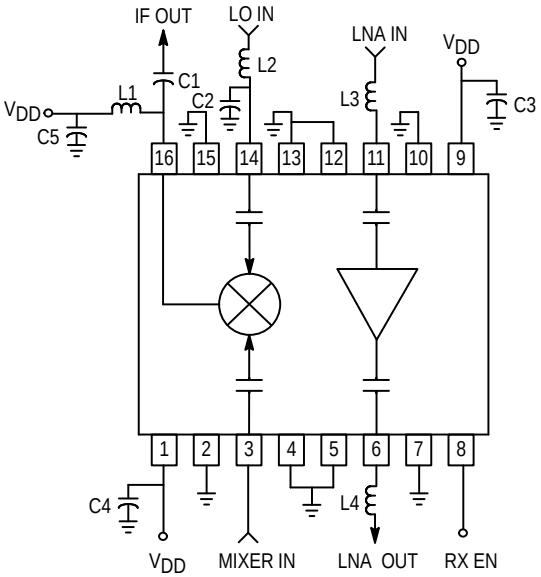
Rating	Symbol	Limit	Unit
Supply Voltage	V_{DD}	5	Vdc
LNA Input Power (Standby Mode)	LNA_{in}	10	dBm
LO Input Power	P_{LO}	0	dBm
Receive Enable Voltage	RX EN	5	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature	T_A	– 30 to +85	°C

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Value	Unit
RF Input Frequency	f_{RF}	1.8 to 1.925	GHz
Mixer LO Frequency	f_{LO}	1.5 to 1.9	GHz
IF Output Frequency	f_{IF}	70 to 325	MHz
Supply Voltage	V_{DD}	2.7 to 3.3	Vdc
Receive Enable Voltage	RX EN	2.7 to 3.3	Vdc

ELECTRICAL CHARACTERISTICS (V_{DD} = 3 V, T_A = 25°C, LO = 1790 MHz @ – 5 dBm, RF = 1.9 GHz , RX EN = 3 V)

Characteristic	Min	Typ	Max	Unit
LNA Gain	—	14	—	dB
LNA Noise Figure	—	2.3	—	dB
LNA Input 3rd Order Intercept	—	–11	—	dBm
Mixer Conversion Gain (into 50 Ω)	—	4	—	dB
Mixer Noise Figure	—	13	—	dB
Mixer Input 3rd Order Intercept	—	0.9	—	dBm
Downconverter Gain (Less Image Filter Loss)	16	—	—	dB
Supply Current, RX Mode (RX EN = 3 V, LO_{off})	—	7	10	mA
Standby Mode Current (RX EN = 0 V, LO off)	—	—	0.5	mA



C1	12 pF (110 MHz) or 7.5 pF (240 MHz)
C2	0.8 pF
C3, C4	100 pF
C5	1000 pF
L1	82 nH (110 MHz) or 15 nH (240 MHz)
L2	8.2 nH
L3, L4	3.0 nH (Microstrip)

Figure 1. Applications Circuit Configuration (for 110 MHz and 240 MHz IF)

Freq (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
1.5	0.801	–64.71	5.65	–63.77	0.025	139.08	0.685	–62.55
1.6	0.741	–70.03	6.07	–80.96	0.033	128.21	0.622	–74.44
1.7	0.641	–73.54	6.63	–98.00	0.038	123.07	0.622	–83.36
1.8	0.559	–72.72	6.70	–113.87	0.047	113.17	0.560	–92.40
1.82	0.533	–71.10	6.58	–117.42	0.046	111.66	0.543	–93.20
1.84	0.512	–71.20	6.32	–120.25	0.046	109.36	0.530	–94.40
1.86	0.494	–69.93	5.92	–123.27	0.049	107.72	0.513	–95.19
1.88	0.478	–68.86	5.79	–126.51	0.052	106.52	0.498	–95.56
1.9	0.467	–67.50	5.88	–129.49	0.054	104.49	0.486	–96.35
1.92	0.452	–66.18	5.98	–132.33	0.055	103.55	0.476	–97.14
2.0	0.383	–57.10	5.57	–143.54	0.055	97.41	0.412	–96.10
2.1	0.326	–47.69	5.06	–155.69	0.058	92.26	0.344	–90.55
2.2	0.271	–35.10	4.61	–167.78	0.063	86.81	0.276	–83.89
2.3	0.205	–15.07	4.12	175.72	0.072	83.78	0.192	–63.78
2.4	0.708	–12.53	1.84	–155.83	0.073	45.03	0.406	–48.22
2.5	0.462	–34.07	3.18	–178.63	0.055	58.37	0.292	–66.60

Table 1. LNA S–Parameters

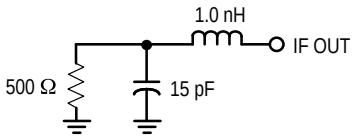


Figure 2. Equivalent IF Output Circuit

TYPICAL CHARACTERISTICS
(V_{DD} = 3 V)

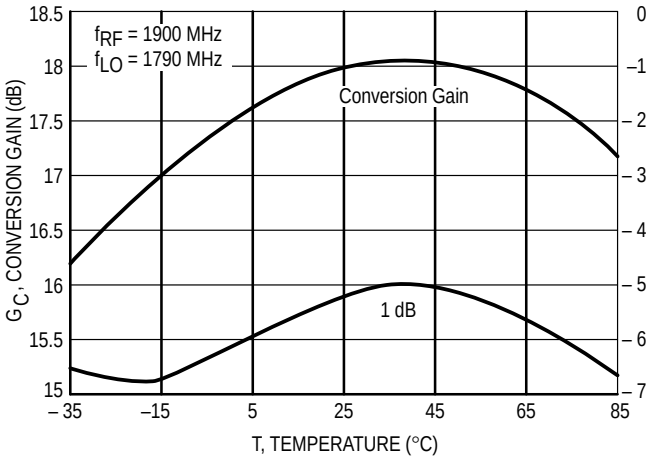


Figure 3. Downconverter Conversion Gain (less Image Filter) and 1 dB Compression versus Temperature

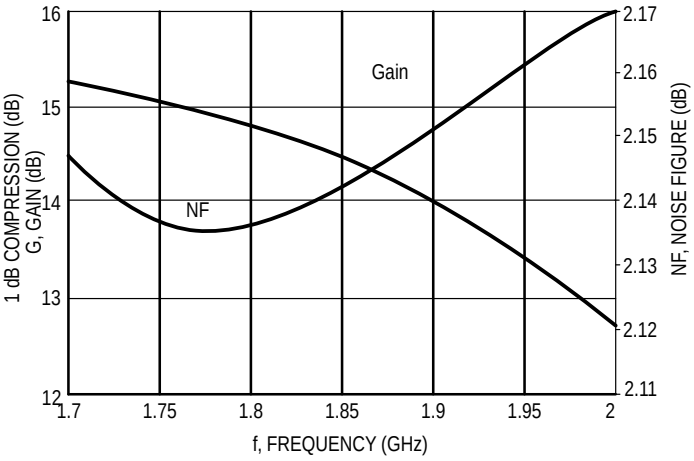


Figure 4. LNA Gain and Noise Figure versus Frequency

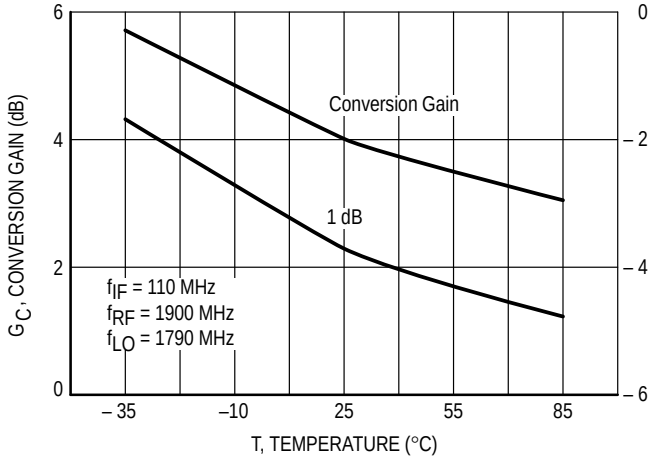


Figure 5. Mixer Conversion Gain and 1 dB Compression versus Temperature

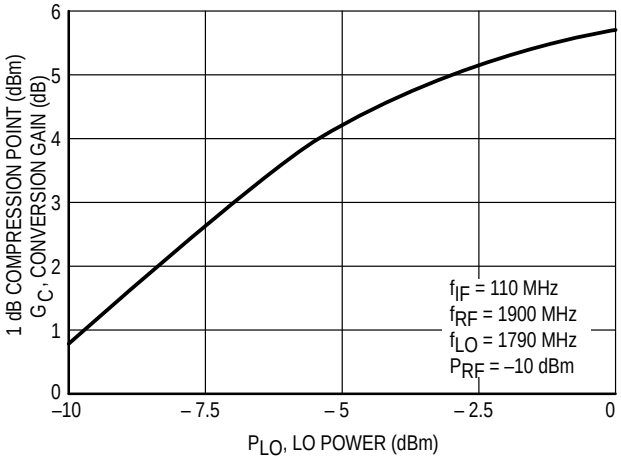


Figure 6. Mixer RF to IF Conversion Gain versus LO Power

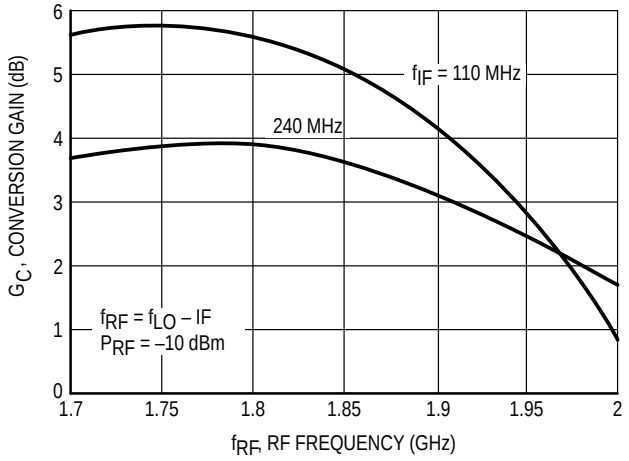


Figure 7. Mixer RF to IF Conversion Gain versus RF Frequency

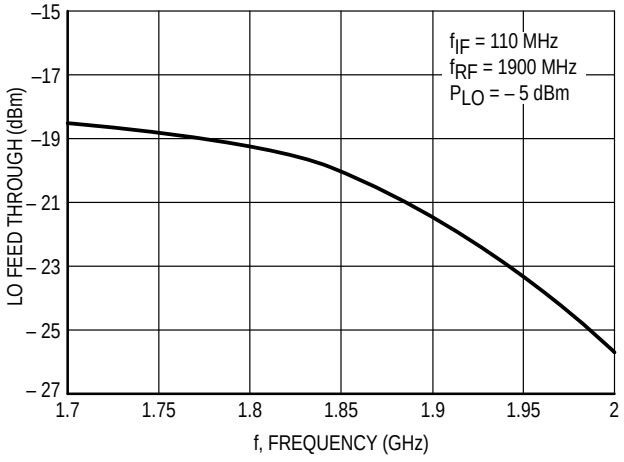


Figure 8. Mixer LO to IF Feed Through versus RF Frequency

DESIGN AND APPLICATIONS INFORMATION

The MRFIC1804 consists of a two–stage GaAs MESFET low noise amplifier and a single ended MESFET mixer. The LNA design conserves bias current through stacking of the two FETs, thus reusing the current. The mixer consists of a common gate stage driving a common source stage with the IF output being the drain of the common source stage shunted with 15 pF. The LNA output and mixer input have been separated to allow the addition of an external image filter. Such a filter, usually ceramic, is useful in improving the mixer noise figure and third order intercept performance. It also provides LO rejection to reduce the amount of LO power which may leak to the antenna. Alternatively, image trapping can be implemented at the LNA input or output with discrete or distributed components.

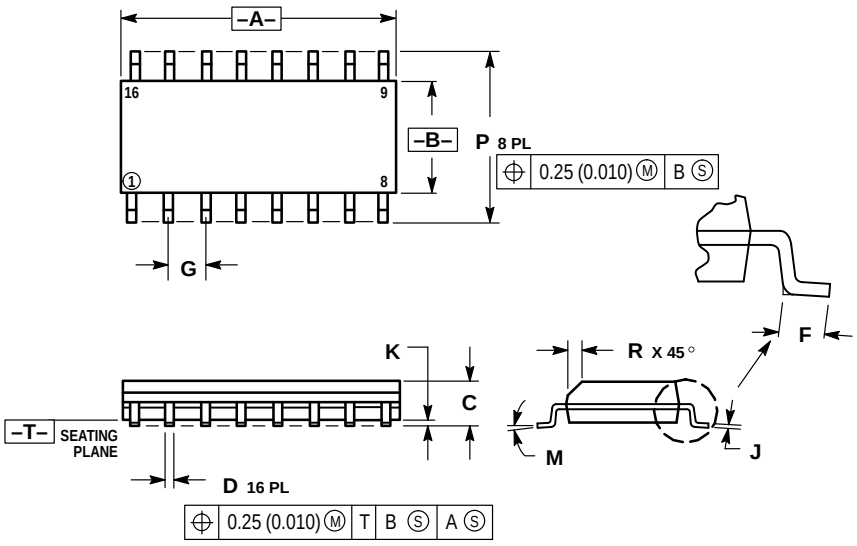
The design has been optimized for application in the PCS bands around 1.9 GHz but is usable from around 1.5 GHz to 2.2 GHz. For applications at 1.9 GHz and IFs of 110 MHz or 240 MHz, the circuit shown in Figure 1 can be used. This circuit was used to derive the characterization data shown in Figures 3 through 8. For other IF frequencies in the 100 MHz to 350 MHz range, use the IF equivalent circuit shown in Figure 2 for matching network design. As can be seen in the characterization curves, performance appears to degrade above about 1.85 GHz. This is partially a function of the circuit shown in Figure 1 and can be improved, first, by adjusting the LO input match, second, by matching LNA input and and the mixer input off chip.

As with all RF circuits, layout is important. Ground vias must be close to the component or lead to be grounded and vias must be plentiful. RF signal lines should be controlled impedance such as microstrip. Bypassing of power supply leads as shown in Figure 1 is essential to avoid oscillation of the circuits.

EVALUATION BOARDS

Evaluation boards are available for RF Monolithic Integrated Circuits by adding a “TF” suffix to the device type. For a complete list of currently available boards and ones in development for newly introduced poduct, please contact your local Motorola Distributor or Sales Office.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

CASE 751B–05
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