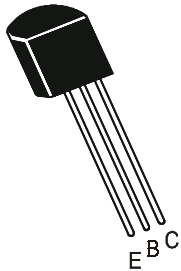


NPN/PNP SILICON PLANAR AMPLIFIER TRANSISTORS

**MPS650 , MPS651 (NPN)
MPS750 , MPS751 (PNP)
TO -92
CBE**



AMPLIFIER TRANSISTORS

ABSOLUTE MAXIMUM RATINGS.

DESCRIPTION	SYMBOL	MPS650	MPS651	UNITS
		MPS750	MPS751	
Collector -Emitter Voltage	V _{CEO}	40	60	V
Collector -Base Voltage	V _{CBO}	60	80	V
Emitter -Base Voltage	V _{EBO}		5.0	V
Collector Current Continuous	I _C		2.0	A
Power Dissipation @Ta=25 degC	P _D		625	mW
Derate Above 25deg C			5.0	mW/deg C
Power Dissipation @Tc=25 degC	P _D		1.5	W
Derate Above 25deg C			12.0	mW/deg C
Operating And Storage Junction Temperature Range	T _j , T _{stg}	-55 to +150		deg C

THERMAL RESISTANCE

Junction to Case	R _{th(j-c)}	83.3	deg C/W
Junction to Ambient	R _{th(j-a)}	200	deg C/W

ELECTRICAL CHARACTERISTICS (Ta=25 deg C Unless Otherwise Specified)

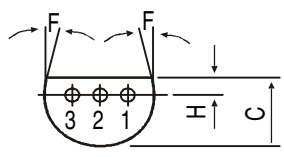
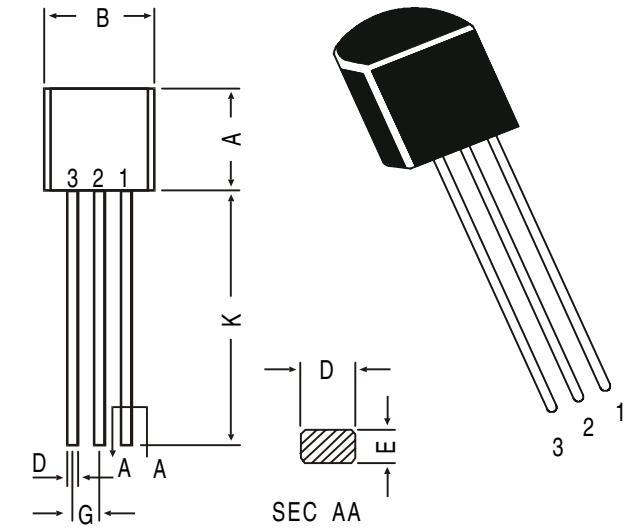
DESCRIPTION	SYMBOL	TEST CONDITION	MPS650	MPS651	UNITS
			MPS750	MPS751	
Collector -Emitter Voltage	V _{CEO} *	I _C =10mA, I _B =0	>40	>60	V
Collector -Base Voltage	V _{CBO}	I _C =100uA, I _E =0	>60	>80	V
Emitter -Base Voltage	V _{EBO}	I _E =10uA, I _C =0	>5.0	>5.0	V
Collector-Cut off Current	I _{CBO}	V _{CB} =60V, I _E =0	<100	-	nA
		V _{CB} =80V, I _E =0	-	<100	nA
Emitter-Cut off Current	I _{EBO}	V _{EB} =4V, I _C =0	<100	<100	nA
DC Current Gain	h _{FE} *	I _C =50mA, V _{CE} =2V	>75	>75	
		I _C =500mA, V _{CE} =2V	>75	>75	
		I _C =1A, V _{CE} =2V	>75	>75	
		I _C =2A, V _{CE} =2V	>40	>40	
Collector Emitter Saturation Voltage	V _{CE(Sat)} *	I _C =2A, I _B =200mA	<0.50	<0.50	V
		I _C =1A, I _B =100mA	<0.30	<0.30	V
Base Emitter on Voltage	V _{BE(on)} *	I _C =1A, V _{CE} =2V	<1.0	<1.0	V
Base Emitter Saturation Voltage	V _{BE(Sat)} *	I _C =1A, I _B =100mA	<1.2	<1.2	V
Current Gain-Bandwidth Product	f _t **	I _C =50mA, V _{CE} =5V f=100MHz	>75	>75	MHz

*Pulse Condition : Length =300us, Duty Cycle=2%

**f_t is defined as the frequency at which /hfe/ extrapolates to unity

TO-92 Plastic Package

TO-92 Transistors on Tape and Ammo Pack

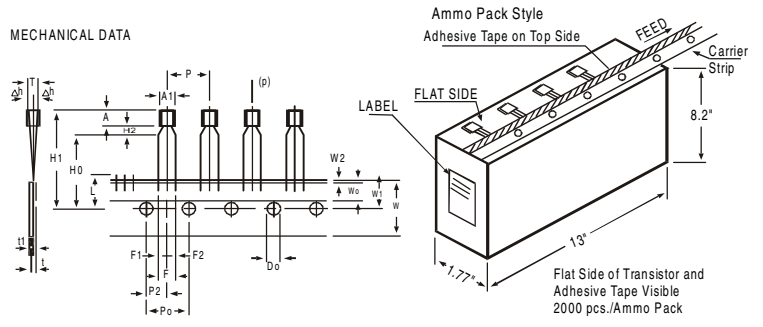


PIN CONFIGURATION
 1. COLLECTOR
 2. BASE
 3. EMITTER

SEC AA

All dimensions in mm.

DIM	MIN.	MAX.
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.41	0.55
E	0.35	0.50
F	5 DEG	
G	1.14	1.40
H	1.14	1.53
K	12.70	—



All dimensions in mm unless specified otherwise

ITEM	SYMBOL	SPECIFICATION				REMARKS
		MIN.	NOM.	MAX.	TOL.	
BODY WIDTH	A1	4.0		4.8		
BODY HEIGHT	A	4.8		5.2		
BODY THICKNESS	T	3.9		4.2		
PITCH OF COMPONENT	P		12.7		±1	
FEED HOLE PITCH	Po		12.7		±0.3	CUMULATIVE PITCH ERROR 1.0 mm/20 PITCH
FEED HOLE CENTRE TO COMPONENT CENTRE	P2		6.35		±0.4	TO BE MEASURED AT BOTTOM OF CLINCH
DISTANCE BETWEEN OUTER LEADS	F	5.08			+0.6 -0.2	
COMPONENT ALIGNMENT	Δh	0		1		AT TOP OF BODY
TAPE WIDTH	W	18			±0.5	
HOLD-DOWN TAPE WIDTH	W0	6			±0.2	
HOLE POSITION	W1	9			+0.7 -0.5	
HOLD-DOWN TAPE POSITION	W2	0.5			±0.2	
LEAD WIRE CLINCH HEIGHT	Ho	16			±0.5	
COMPONENT HEIGHT	H1			23.25		
LENGTH OF SNIPPED LEADS	L			11.0		
FEED HOLE DIAMETER	Do		4		±0.2	
TOTAL TAPE THICKNESS	t			1.2		±0.3 - 0.6
LEAD - TO - LEAD DISTANCE F1,	F2		2.54		+0.4 -0.1	
CLINCH HEIGHT	H2			3		
PULL - OUT FORCE	(P)	6N				

- NOTES**
1. MAXIMUM ALIGNMENT DEVIATION BETWEEN LEADS NOT TO BE GREATER THAN 0.2 mm.
 2. MAXIMUM NON-CUMULATIVE VARIATION BETWEEN TAPE FEED HOLES SHALL NOT EXCEED 1 mm IN 20 PITCHES.
 3. HOLDDOWN TAPE NOT TO EXCEED BEYOND THE EDGE(S) OF CARRIER TAPE AND THERE SHALL BE NO EXPOSURE OF ADHESIVE.
 4. NO MORE THAN 3 CONSECUTIVE MISSING COMPONENTS ARE PERMITTED.
 5. A TAPE TRAILER, HAVING AT LEAST THREE FEED HOLES ARE REQUIRED AFTER THE LAST COMPONENT.
 6. SPLICES SHALL NOT INTERFERE WITH THE SPROCKET FEED HOLES.

Packing Detail

PACKAGE	STANDARD PACK		INNER CARTON BOX		OUTER CARTON BOX		
	Details	Net Weight/Qty	Size	Qty	Size	Qty	Gr Wt
TO-92 Bulk	1K/polybag	200 gm/1K pcs	3" x 7.5" x 7.5"	5.0K	17" x 15" x 13.5"	80.0K	23 kgs
TO-92 T&A	2K/ammo box	645 gm/2K pcs	12.5" x 8" x 1.8"	2.0K	17" x 15" x 13.5"	32.0K	12.5 kgs

Customer Notes

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Discrete Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Discrete Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.



CDIL is a registered Trademark of

Continental Device India Limited

C-120 Naraina Industrial Area, New Delhi 110 028, India.

Telephone + 91-11-2579 6150, 5141 1112 Fax + 91-11-2579 5290, 5141 1119

email@cdil.com www.cdilsemi.com