8-STAGE STATIC SHIFT REGISTERS: SYNCHRONOUS PARALLEL OR SERIAL INPUT/SERIAL OUTPUT: MMC 4014 ASYNCHRONOUS PARALLEL INPUT OR SYNCHRONOUS SERIAL INPUT/SERIAL OUTPUT: MMC 4021

GENERAL DESCRIPTION

The MMC 4014, MMC 4021 series types are 8-stage parallel-or serial-input/serial-output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D type, master-slave flip-flop; in addition to an output from stage 8, "Q" outputs are also available from stage 6 and 7.

Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the MMC 4014. In the MMC 4021 serial entry is synchronous with the clock but parallel entry is asynchronous.

In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input.

When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line.

When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line.

In the MMC 4021, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made.

Register expansion using multiple package is permitted.

The MMC 4014, MMC 4021 series types are supplied in 16-lead dual-in-line plastic or ceramic package.

FEATURES

- Medium speed operation-12 MHz (typ.) clock rate at $V_{DD}-V_{SS} = 10$ V
- Fully static operation
- 8 Master-Slave flip-flops plus output buffering and control gating

ABSOLUTE MAXIMUM RATINGS

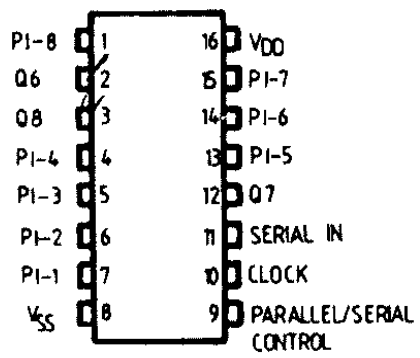
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_I	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		± 10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_I	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



TRUTH TABLE

For 4014

CL	Serial input	Parallel/serial control	P I-1	P I-n	Q_1 (internal)	Q_n	
⎍	X	1	0	0	0	0	
⎍	X	1	1	0	1	0	
⎍	X	1	0	1	0	1	
⎍	X	1	1	1	1	1	
⎍	0	0	X	X	0	Q_n-1	
⎍	1	0	X	X	1	Q_n-1	
⎍	X	X	X	X	Q_1	Q_n	NC

X = Don t care case NC = No change

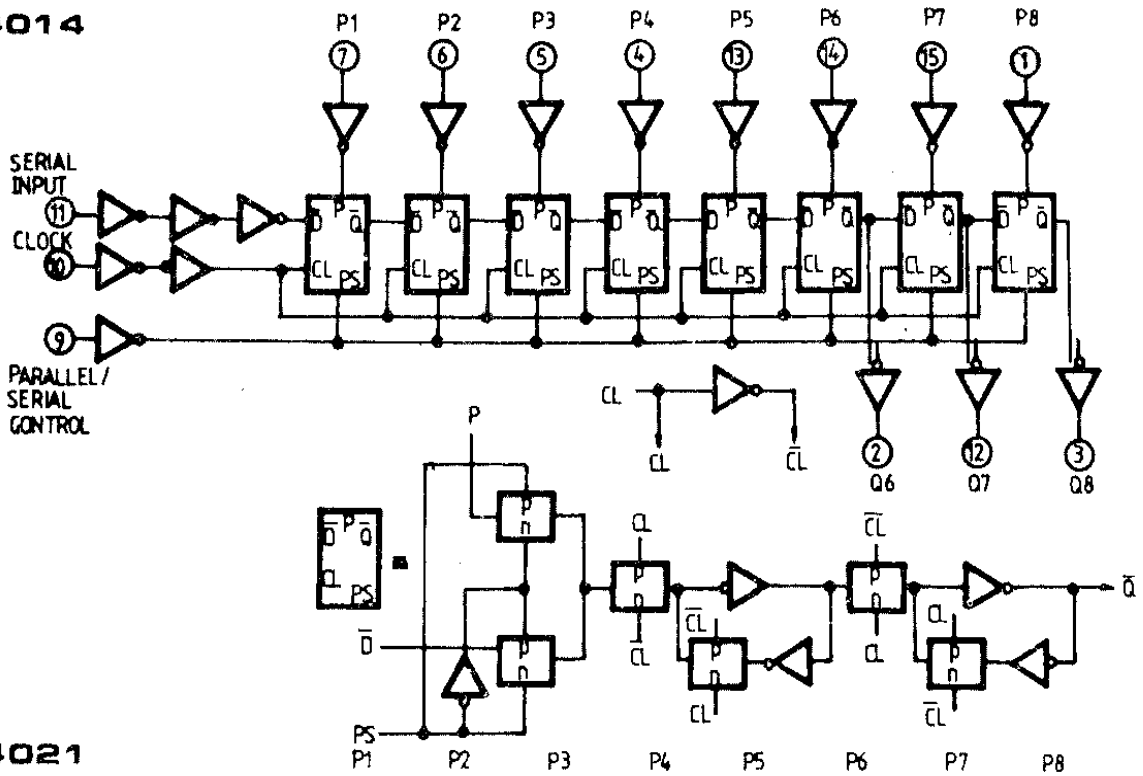
LOGIC DIAGRAMS AND TRUTH TABLE

For MMC 4021

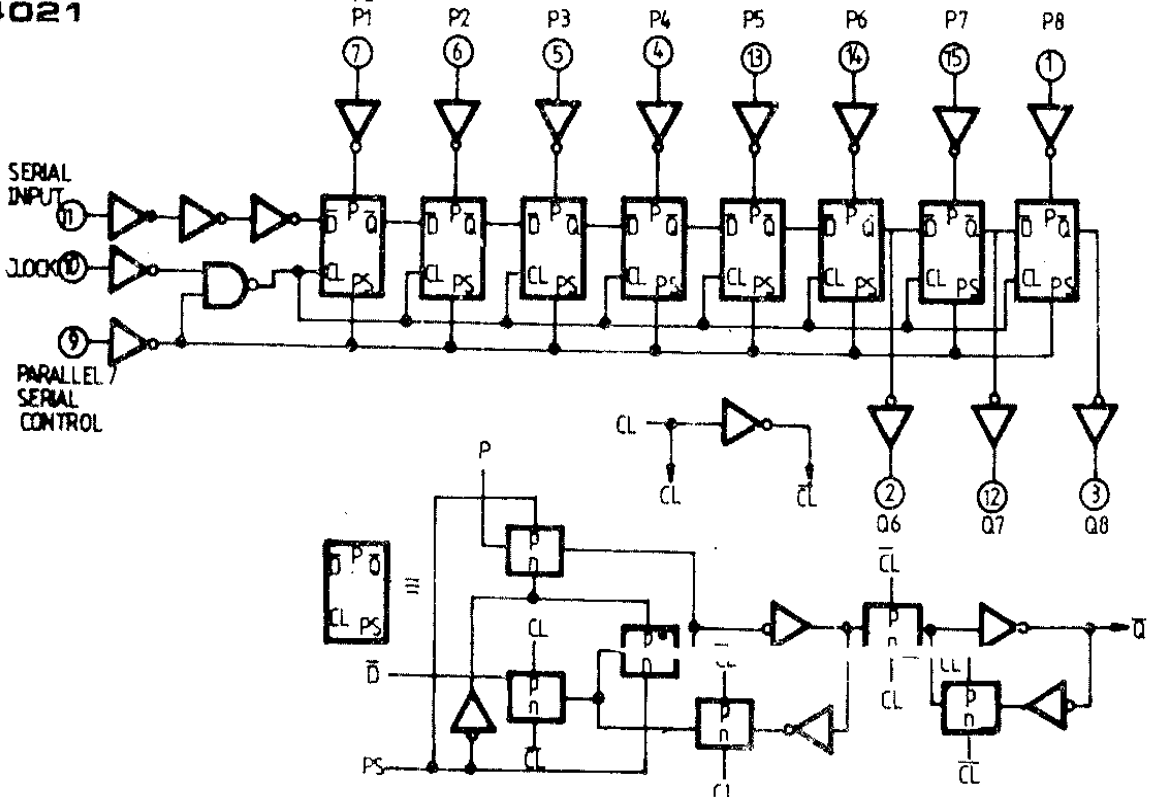
CL	Serial input	Parallel/serial control	P I-1	P I-n	Q_1 (internal)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
⌐	0	0	X	X	0	Q_n-1	
⌐	1	0	X	X	1	Q_n-1	
⌐	X	0	X	X	Q_1	Q_n	NC

X = Don't care case NC = No change

MMC 4014



MMC 4021



STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		E, F types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	.1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		±10 [5]	±0.1		±1	μA
		E, F types	0/15			15		±0.3		±10 [5]	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, R_L = 200 kohm, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall times= 20 ns)

PARAMETER	TEST CONDITIONS	VALUES			UNIT
	V_{DD} (V)	min.	typ.	max.	
Clocked operation					
t_{PLH}, t_{PHL} Propagation delay time	5		160	320	ns
	10		80	160	
	15		60	120	
t_{THL}, t_{TLH} Transition time	5		100	200	ns
	10		50	100	
	15		40	80	
f_{CL}* Maximum clock input frequency	5	3	6		MHz
	10	6	12		
	15	8.5	17		
t_W Clock pulse width	5	180	90		ns
	10	80	40		
	15	50	25		
t_r, t_f Clock input rise or fall time	5			15	µs
	10			15	
	15			15	
t_{setup} Setup time, serial input (ref. to CL)	5	120	60		ns
	10	80	40		
	15	60	30		
t_{setup} Setup time, parallel inputs (4014) (ref. to CL)	5	80	40		ns
	10	50	25		
	15	40	20		
t_{setup} Setup time, parallel inputs (4021)	5	50	25		ns
	10	30	15		
	15	20	10		
t_{setup} Setup time, parallel/serial control (4014) (ref. to CL)	5	180	90		ns
	10	80	40		
	15	60	30		
t_{hold} Hold time, serial in, parallel in, parallel/serial control	5	0			ns
	10	0			
	15	0			
t_{WH} P/S Pulse width (4021)	5	160	80		ns
	10	80	40		
	15	50	25		
t_{rem} P/S Removal, time (4021) (ref. to CL)	5	280	140		ns
	10	140	70		
	15	100	50		

* If more then one unit is cascated t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.