

Regulator+Reset IC Monolithic IC MM1437

Outline

This IC combines a low saturation 5V regulator, adapted for low power consumption, and a reset function (regulator output monitoring), for which there is significant market need, that uses the built-in 4.2V detection delay circuit.

Features

1. Small input/output voltage difference 0.25V typ.
2. High input voltage 18V max.
3. Internal thermal shutdown circuit.
4. Internal current-limiting circuit.
5. Adjustment-free reset detection voltage 4.2V typ.
6. Easy to set delay time from voltage detection to reset release.

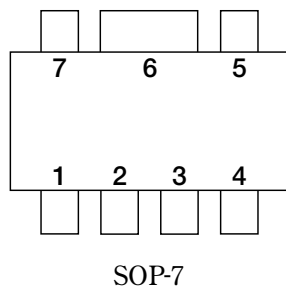
Package

SOP-7
SIP-5

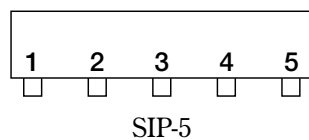
Applications

TV, monitors, air conditioners, others.

Pin Assignment

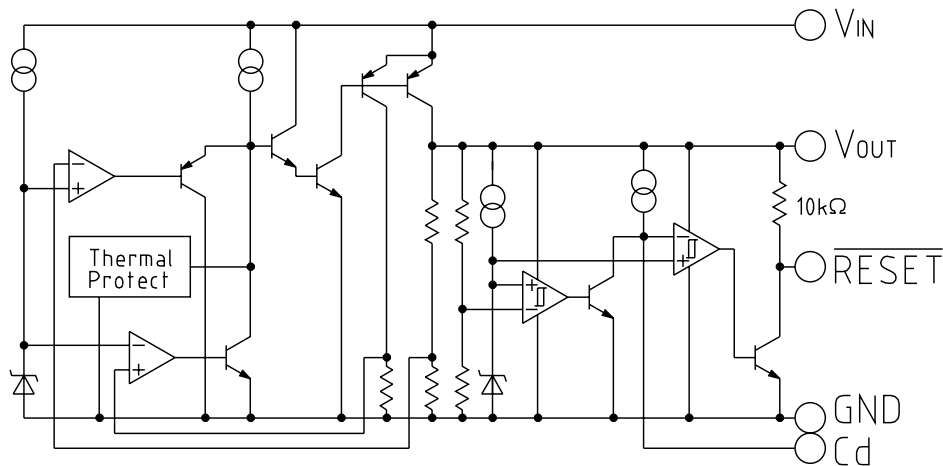


1	GND
2	$\overline{\text{RESET}}$
3	Cd
4	V _{IN}
5	V _{OUT}
6	GND
7	N.C



1	$\overline{\text{RESET}}$
2	Cd
3	V _{IN}
4	V _{OUT}
5	GND

Equivalent Circuit Diagram



Pin Description

Pin No.	Pin name	Functions	Equivalent circuit diagram						
1 (SOP-7) 5 (SIP-5)	GND	GND pin							
2 (SOP-7) 1 (SIP-5)	$\overline{\text{RESET}}$	Output pin voltage detection output V_{OUT} pin voltage detection output pin $\overline{\text{RESET}}$ pin logic <table border="1" style="margin-left: 20px;"> <tr> <td></td> <td>$\overline{\text{RESET}}$</td> </tr> <tr> <td>$V_{\text{OUT}} < V_{\text{S}}$</td> <td>L</td> </tr> <tr> <td>$V_{\text{OUT}} > V_{\text{S}}$</td> <td>H</td> </tr> </table>		$\overline{\text{RESET}}$	$V_{\text{OUT}} < V_{\text{S}}$	L	$V_{\text{OUT}} > V_{\text{S}}$	H	
	$\overline{\text{RESET}}$								
$V_{\text{OUT}} < V_{\text{S}}$	L								
$V_{\text{OUT}} > V_{\text{S}}$	H								
3 (SOP-7) 2 (SIP-5)	Cd	Delay time capacitor pin $\overline{\text{RESET}}$ pin output delay time can be set by the capacitance connected to the Cd pin. $t_{\text{PLH}} = 100000 \cdot C$ t_{PLH} : transmission delay time [S] C: capacitor value [F]							
4 (SOP-7) 3 (SIP-5)	V_{IN}	Voltage supply input pin							
5 (SOP-7) 4 (SIP-5)	V_{OUT}	Regulator output pin							
6 (SOP-7)	GND	GND pin							
7 (SOP-7)	N.C								

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Operating temperature	T _{OPR}	-20~+85	°C
Storage temperature	T _{STG}	-40~+125	°C
Supply voltage	V _{CC}	-0.3~+18	V
Output current	I _{OUT}	200	mA
Power dissipation	P _d	650*	mW

Note: * When mounted on a 55×20 mm paper phenol board (SOP-7)
 When mounted on a 45×45 mm paper phenol board (SIP-5)

Recommended Operating Conditions

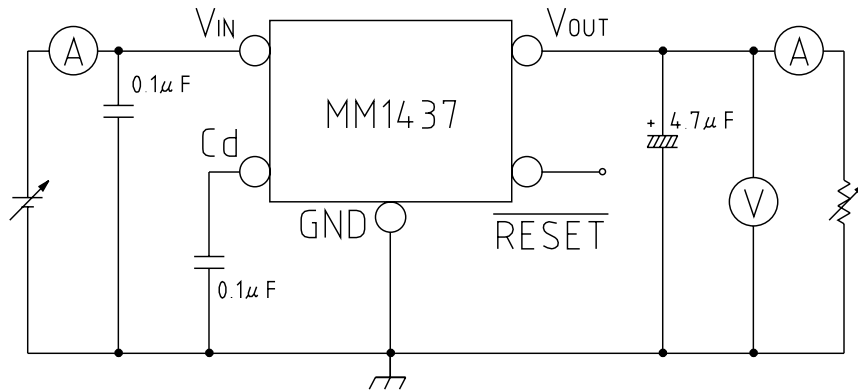
Item	Symbol	Ratings	Unit
Operating temperature	T _{OP}	-20~+85	°C
Output current	I _{OP}	0~150	mA
Operating voltage	V _{OP}	2~16	V

Electrical Characteristics (Except where noted otherwise, T_a=25°C)

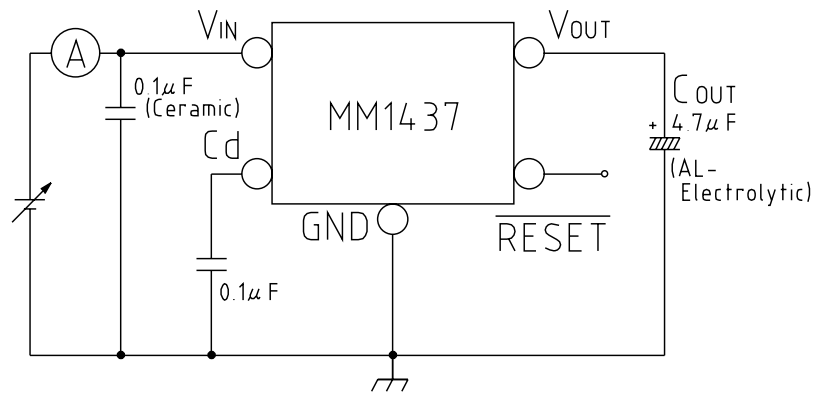
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
No-load input current 1	I _{ccq1}	V _{IN} =6V I _{OUT} =0mA		400	800	μA
No-load input current 2	I _{ccq2}	V _{IN} =4V I _{OUT} =0mA		2.5		mA
Regulator						
Output voltage	V _{OUT}	V _{IN} =6V I _{OUT} =30mA	4.90	5.00	5.10	V
Input-output differential voltage	V _{i0}	V _{IN} =4.8V I _{OUT} =150 mA		0.25	0.50	V
Line regulation	ΔV ₁	V _{IN} =6V~10V I _{OUT} =30mA		10	30	mV
Load regulation	ΔV ₂	V _{IN} =6V I _{OUT} =0~150mA		40	80	mV
Vo temperature coefficient *1	ΔV _{OUT} /ΔT	T _j =-20~+85°C V _{IN} =6V I _{OUT} =30mA		100		ppm/°C
Ripple rejection *1	RR	V _{IN} =6V f=120Hz V _{RIPPLE} =1V _{P-P} , I _{OUT} =30mA	50	60		dB
Output noise voltage *1	V _n	V _{IN} =6V, f=20~80kHz I _{OUT} =30mA		200	400	μV _{rms}
Reset						
Detecting voltage	V _S	V _{IN} =H→L	4.03	4.2	4.37	V
Vs temperature coefficient *1	ΔV _S /ΔT	T _j =-20~+85°C		100		ppm/°C
Hysteresis voltage	ΔV _S	V _{OUT} =H→L→H	25	50	100	mV
Low-level output voltage	V _{OL}	V _{OUT} =3.9V		100	200	mV
RESET delay time	t _{PLH}	C _d =0.1μF	5	10	15	mS
"L" transmission delay time *1	t _{PHL}	C _d =0.1μF		30	90	μS
Threshold operating voltage	V _{OPL}	V _{OL} =0.4V		0.65	0.85	V

Note 1: design guaranteed

Measuring Circuit



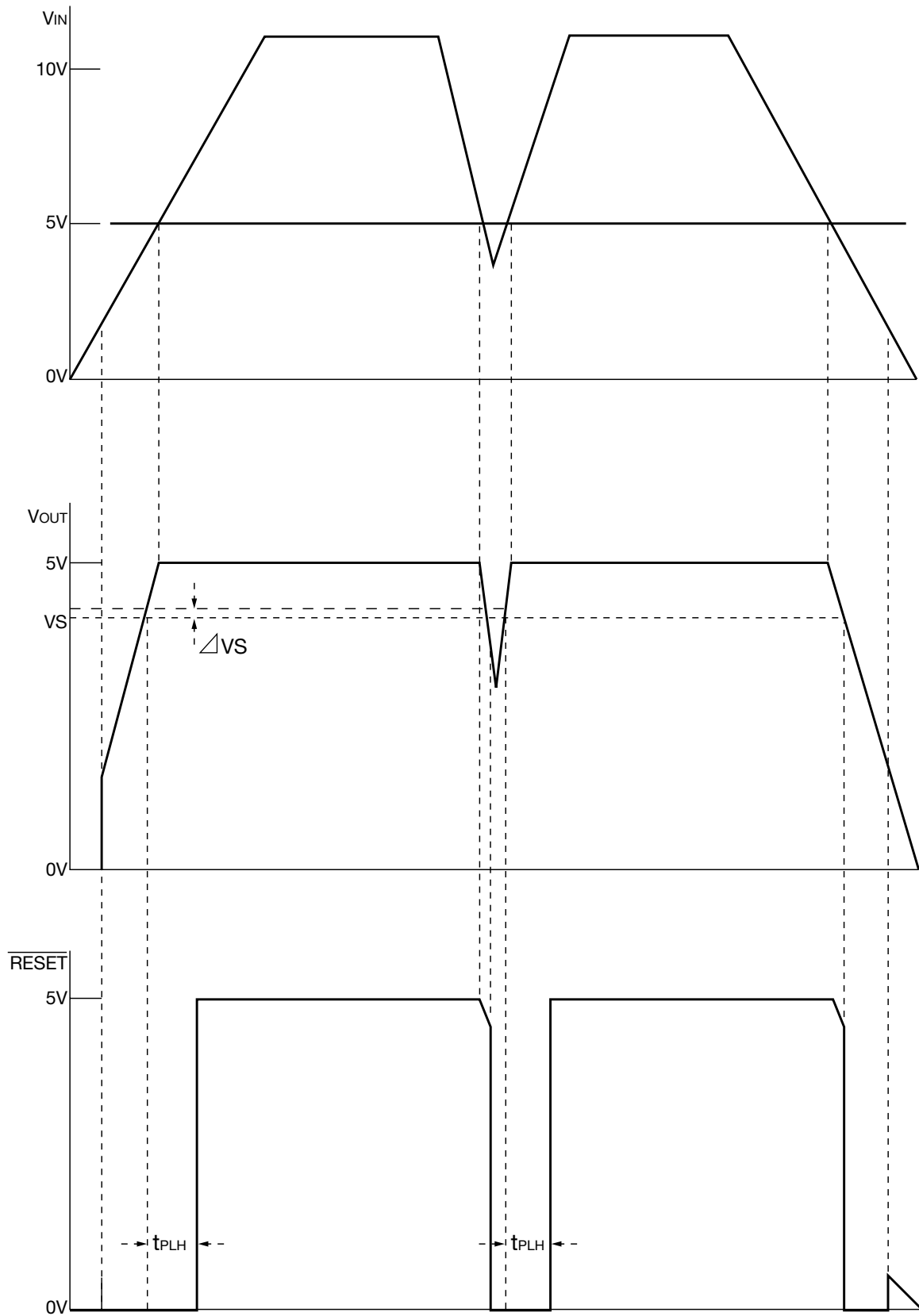
Application Circuit



Note 1 : This regulator is not internally compensated and thus requires an external output-capacitor (C_{OUT}) for stability.

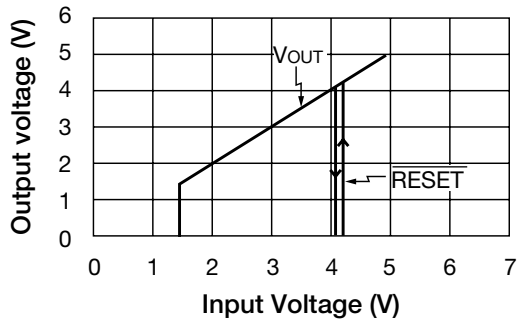
Note 2 : \overline{RESET} -terminal with a built-in pull-up resistance (10k Ω).

Timing Chart

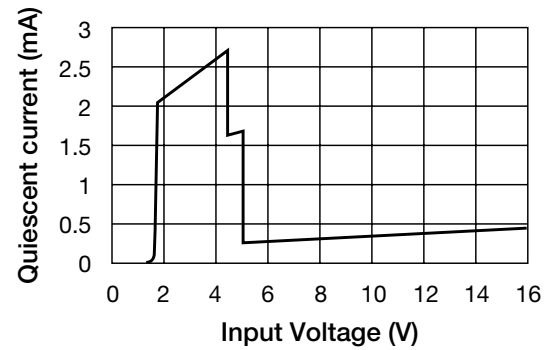


Characteristics

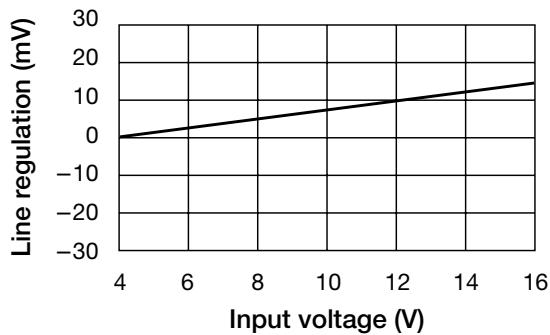
Detection voltage (I_{OUT}=0mA)



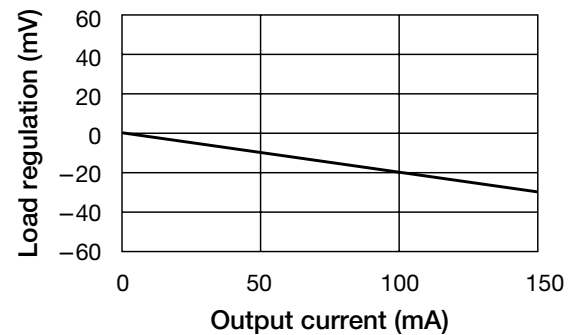
Quiescent current (I_{OUT}=0mA)



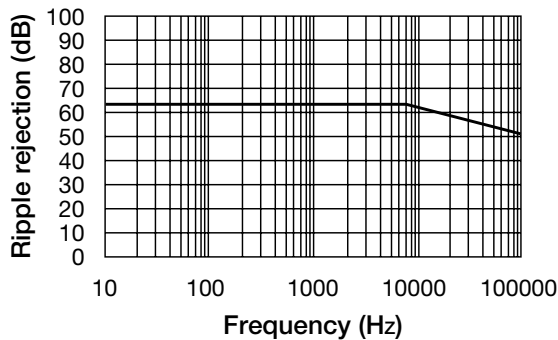
Line regulation



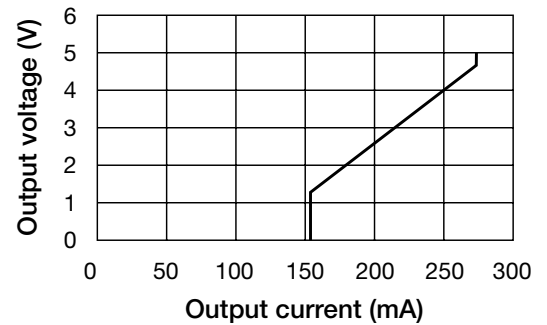
Load regulation



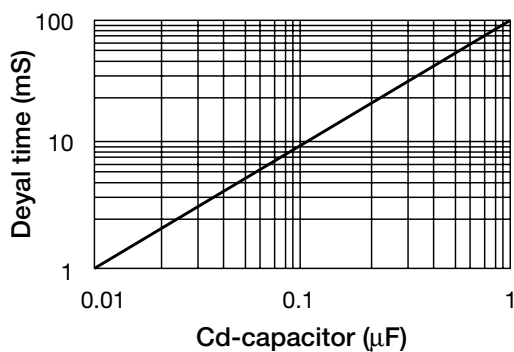
Ripple rejection



Current limit



RESET delay time



Allowable loss

