

Superimpose Monolithic IC MM1166

Outline

This is a superimpose IC that supports S-VHS, with 1 circuit for Y signals and 1 circuit for C signals, with built-in character level and border level. The level is suppressed to eliminate the problem of spike noise generated when switching between input video signal and character signal.

Features

1. Supports S-VHS
2. Built-in character and border levels
3. Frequency response Y : 10MHz C : 5MHz
4. Input/output signal 1V_{P-P}
5. Operating power supply voltage range 4.5~5.5V

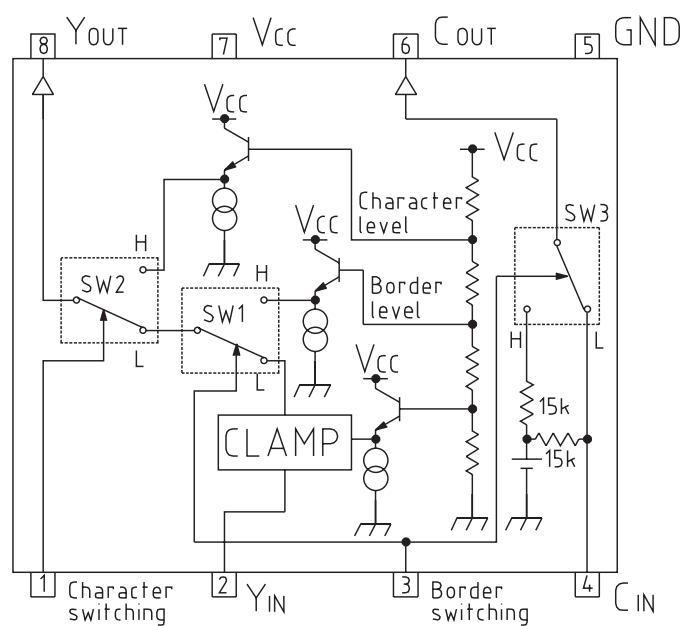
Package

SOP-8C (MM1166XF)

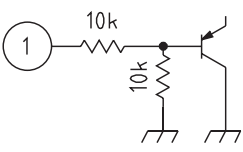
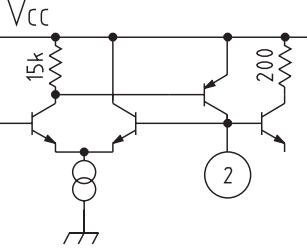
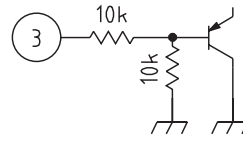
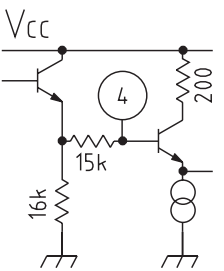
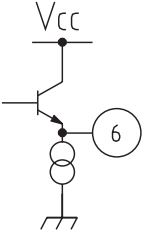
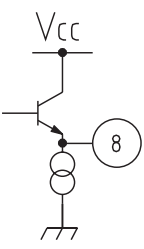
Applications

1. TV
2. VCR
3. VCR with camera

Block Diagram



Pin Description

Pin no.	Pin name	Internal equivalent circuit diagram	Pin Description
1	Character switching		Input pin for pulse that switches input signal and character signal High : character level output
2	Y _{IN}		Luminance signal input pin
3	Border switching		Input pin for pulse that switches input signal and border signal High : border level output
4	C _{IN}		Chroma signal input pin
5	GND		GND
6	C _{OUT}		Chroma signal output pin
7	V _{CC}		Power supply pin
8	Y _{OUT}		Luminance signal output pin

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T _{STG}	-40~+125	°C
Operating temperature	T _{OPR}	-20~+75	°C
Power supply voltage	V _{CC} max.	7	V
Allowable loss	P _d	300	mW

Electrical Characteristics (Except where noted otherwise, Ta=25°C, V_{CC}=5.0V, pulse level 0V, SG1~SG2: no signal, SWA, B : 1)

Item	Symbol	Measurement circuit	Measurement conditions	Min.	Typ.	Max.	Units
Operating power supply voltage	V _{CC}			4.5	5.0	5.5	V
Consumption current	I _{CC}				6.5	9.0	mA
Y subsystem							
Voltage gain	G _{v1}	TP5A	SG1 : Sweep signal 1V _{P-P} , 0.1MHz	-0.5	0	+0.5	dB
Frequency characteristic	F _{c1}		SG1 : Sweep signal 1V _{P-P} 10MHz/0.1MHz	-1.0	0	1.0	dB
Differential gain	D _G	TP5B	SG1 : Staircase wave 1V _{P-P} APL=10, 50, 90%	-3.0	1.0	3.0	%
Differential phase	D _P		-3.0	1.0	3.0	deg	
Character level	V _{CH}	TP5A	SG1 : Staircase wave 1V _{P-P} *1	70	75	80	IRE
Edge level	V _{ED}		SG1 : Staircase wave 1V _{P-P} *1	5	10	15	IRE
C subsystem							
Voltage gain	G _{v2}	TP7	SG2 : Sine wave 1V _{P-P} , 0.1MHz	-0.5	0	+0.5	dB
Frequency characteristic	F _{c2}		SG2 : Sine wave 1V _{P-P} , 5MHz/0.1MHz	-1.0	0	1.0	dB
Crosstalk *2							
Y → C	C _{T1}	TP7	SG1 : Sine wave 1V _{P-P} , 4.43MHz SWB : 2		-65	-55	dB
C → Y	C _{T2}	TP5A	SG2 : Sine wave 1V _{P-P} , 4.43MHz SWA : 2		-65	-55	dB
SW input voltage							
Character input H	V _{IH1}	TP5A	SG1 : Staircase wave 1V _{P-P} *3	2.1			V
Character input L	V _{IL1}		SG1 : Staircase wave 1V _{P-P} *4			0.7	V
Edge input H	V _{IH2}		SG1 : Staircase wave 1V _{P-P} *5	2.1			V
Edge input L	V _{IL2}		SG1 : Staircase wave 1V _{P-P} *6			0.7	V

*1 Input a 1V_{P-P} staircase wave to SG1, and pulses as shown in Figure 1 to TP1 and TP3, and measure TP5A.

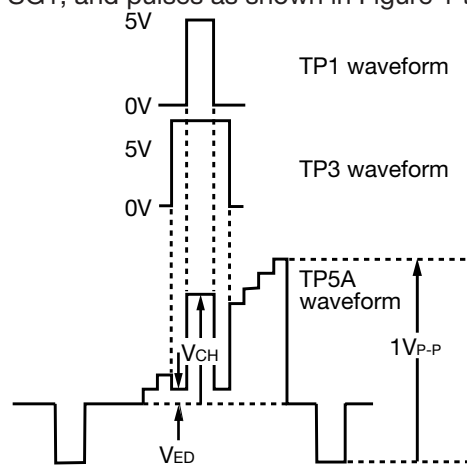


Figure 1 TP1, TP3, TP5A waveforms

*2 Given input signal as V1 and output signal as V2, C_T is obtained as follows.

$$C_T = 20 \log \frac{V_2}{V_1} \text{ dB}$$

*3 Character switching pin (Pin 1) high level voltage

*4 Character switching pin (Pin 1) low level voltage

*5 Border switching pin (Pin 3) high level voltage

*6 Border switching pin (Pin 3) low level voltage

Measuring Circuit

