ML9212

32-Bit Duplex/Triplex (1/2 duty / 1/3 duty) VF Controller/Driver with Digital Dimming

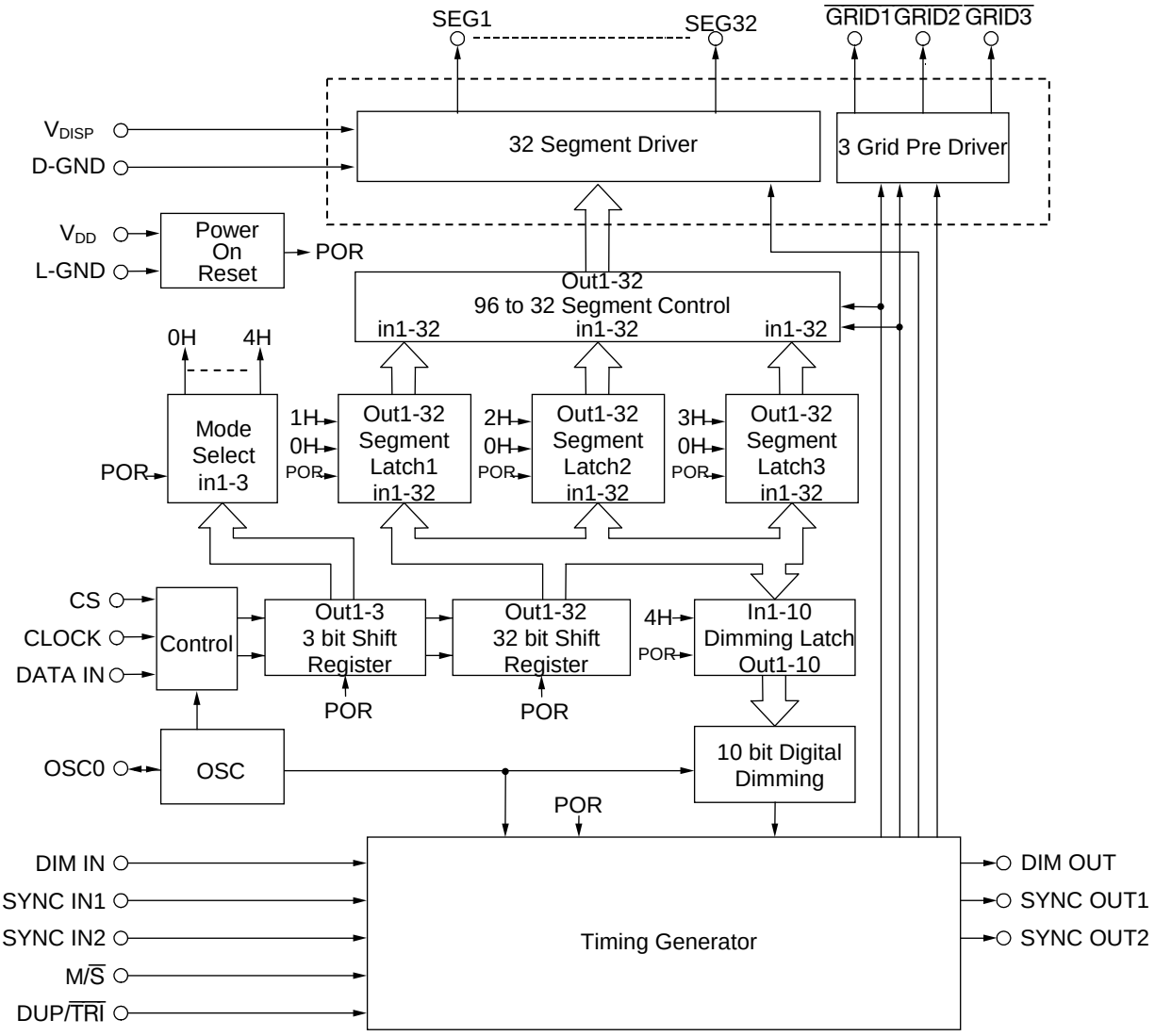
GENERAL DESCRIPTION

The ML9212 is a full CMOS controller/driver for Duplex or Triplex (1/2 duty or 1/3 duty) vacuum fluorescent display tube. It consists of a 32-segment driver multiplexed to drive up to 96 segments, and 10-bit digital dimming circuit.
ML9212 features a selection of a master mode and a slave mode, and therefore it can be used to expand segments for the VFD driver with keyscan and A/D converter function.
ML9212 provides an interface with a microcontroller only by three signal lines: DATA IN, CLOCK and CS.

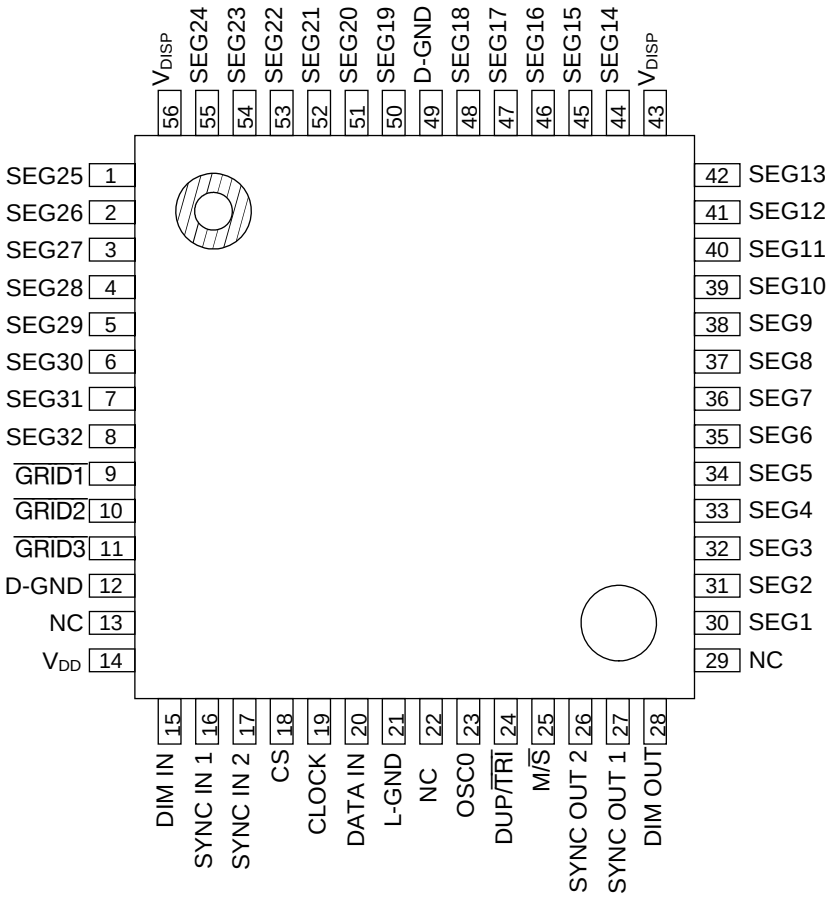
FEATURES

- Logic supply voltage (V_{DD}) : 4.5 to 5.5 V
- Driver supply voltage (V_{DISP}) : 8 to 18 V
- Duplex/Triplex (1/2 duty / 1/3 duty) selectable
  DUP/$\overline{TRI}$ = 1/2 duty selectable at "H" level
  DUP/$\overline{TRI}$ = 1/3 duty selectable at "L" level
- Number of display segments
  Max. 64-segment display (during 1/2 duty mode)
  Max. 96-segment display (during 1/3 duty mode)
- Master/Slave selectable
  M/$\overline{S}$ = Master mode selectable at "H" level
  M/$\overline{S}$ = Slave mode selectable at "L" level
- Interface with a microcontroller
  Three lines: CS, CLOCK, and DATA IN
- 32-segment driver outputs : I_{OH} = –5 mA at V_{OH} = V_{DISP}–0.8 V (SEG1 to 22)
  (can be directly connected to VFD tube : I_{OH} = –10 mA at V_{OH} = V_{DISP}–0.8V (SEG23 to 32)
  and require no external resisters) : I_{OL} = 500 µA at V_{OL} = 2 V (SEG1 to 32)
- 3-grid pre-driver outputs : I_{OH} = –5.0 mA at V_{OH} = V_{DISP}–0.8 V
  (require external drivers) I_{OL} = 10 mA at V_{OL} = 2 V
- Logic outputs : I_{OH} = –200 µA at V_{OH} = V_{DD}–0.8 V
  I_{OL} = 200 µA at V_{OL} = 0.8 V
- Built-in digital dimming circuit (10-bit resolution)
- Built-in oscillation circuit (external R and C)
- Built-in Power-On-Reset circuit
- Package options:
  56-pin plastic QFP (QFP56-P-910-0.65-2K)(ML9212GA)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

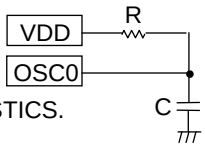


NC: No connection
(OPEN)

56-pin Plastic QFP

PIN DESCRIPTIONS

Symbol	Pin	Type	Description
V_{DISP}	43, 56	—	Power supply pins for VFD driver circuit. 43 pin and 56 pin should be connected externally.
V_{DD}	14	—	Power supply pin for logic drive.
D-GND	12, 49	—	D-GND is ground pin for the VFD driver circuit. L-GND is ground pin for the logic circuit. 12 pin, 21 pin and 49 pin should be connected externally.
L-GND	21	—	
SEG1 to 22	30 to 42, 44 to 48, 50 to 53	O	Segment (anode) signal output pins for a VFD tube. These pins can be directly connected to the VFD tube. External circuit is not required. $I_{OHL} \leq -5$ mA
SEG23 to 32	1 to 8, 54, 55	O	Segment (anode) signal output pins for a VFD tube. These pins can be directly connected to the VFD tube. External circuit is not required. $I_{OHL} \leq -10$ mA
$\overline{GRID1}$ to $\overline{3}$	9, 10, 11	O	Inverted Grid signal output pins. For pre-driver, the external circuit is required. $I_{OL} \leq 10$ mA
CS	18	I	Chip select input pin. Data is not transferred when CS is set to a Low level.
CLOCK	19	I	Shift clock input pin. Serial data shifts at the rising edge of the CLOCK.
DATA IN	20	I	Serial data input pin (positive logic). Data is input to the shift register at the rising edge of the CLOCK signal.
DUP/$\overline{TRI}$	24	I	Duplex/Triplex operation select input pin. Duplex (1/2 duty) operation is selected when this pin is set to V_{DD}. Triplex (1/3 duty) operation is selected when this pin is set to L-GND.
M/$\overline{S}$	25	I	Master/Slave mode select input pin. Master mode is selected when this pin is set to V_{DD}. Slave mode is selected when this pin is set to L-GND.
DIM IN	15	I	Dimming pulse input. When the slave mode is selected, the pulse width of the all segment output are controlled by a input pulse width of DIM IN. Connect this pin to the master side DIM OUT pin at the slave mode. When the master mode is selected, the input level of this pin is ignored and the pulse width of the all grids and segment outputs are controlled by a built-in 10-bit dimming circuit. Connect this pin to V_{DD} or L-GND at the master mode.

Symbol	Pin	Type	Description
SYNC IN 1, 2	16, 17	I	Synchronous signal input. When the slave mode is selected, connect these pins to the master side SYNC OUT 1, and 2 pins. When the master mode is selected, the input level of these pins are ignored. Connect these pins to V_{DD} or L-GND at the master mode.
DIM OUT	28	O	Dimming pulse output. Connect this pin to the slave side DIM IN pin.
SYNC OUT 1, 2	26, 27	O	Synchronous signal output. Connect these pins to the slave side SYNC IN 1, and 2 pins.
OSC0	23	I/O	RC oscillator connecting pins. Oscillation frequency depends on display tubes to be used. For details refer to ELECTRICAL CHARACTERISTICS. 
NC	13,22,29	-	OPEN pins.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Condition	Ratings	Unit
Driver Supply Voltage	V_{DISP}	—	–0.3 to +20	V
Logic Supply Voltage	V_{DD}	—	–0.3 to +6.5	V
Input Voltage	V_{IN}	—	–0.3 to V_{DD}+0.3	V
Power Dissipation	P_D	Ta ≥ 105°C	233	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C
Output Current	I_{o1}	SEG1 to 22	–10.0 to +2.0	mA
	I_{o2}	SEG23 to 32	–20.0 to +2.0	mA
	I_{o3}	$\overline{GRID1}$ to $\overline{3}$	–10.0 to +20.0	mA
	I_{o4}	DIM OUT, SYNC OUT1, SYNC OUT2	–2.0 to +2.0	mA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Driver Supply Voltage	V_{DISP}	—	8.0	13.0	18.0	V
Logic Supply Voltage	V_{DD}	—	4.5	5.0	5.5	V
High Level Input Voltage	V_{IH}	All inputs except OSC0	$0.8V_{DD}$	—	—	V
Low Level Input Voltage	V_{IL}	All inputs except OSC0	—	—	$0.2V_{DD}$	V
Clock Frequency	f_C	—	—	—	2.0	MHz

Parameter	Symbol	Condition		Min	Typ.	Max.	Unit
Oscillation Frequency	f_{OSC}	R = 10 kΩ±5%, C = 27 pF±5%		2.2	3.3	4.4	MHz
Frame Frequency	f_{FR}	R = 10 kΩ±5%, C = 27 pF±5%	1/3 duty	179	269	358	Hz
			1/2 duty	268	403	538	
Operating Temperature	T_{OP}	—		–40	—	+105	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics

Ta = –40 to +105°C, V_{DISP} = 8.0 to 18.0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	*1)	—		$0.8V_{DD}$	—	V
Low Level Input Voltage	V_{IL}	*1)	—		—	$0.2V_{DD}$	V
High Level Input Current	I_{IH}	*1)	$V_{IH} = V_{DD}$		–1.0	+1.0	μA
Low Level Input Current	I_{IL}	*1)	V_{IL} = GND		–1.0	+1.0	μA
High Level Output Voltage	V_{OH1}	SEG1-22	V_{DISP} = 9.5V	I_{OH1} = –5 mA	V_{DISP} – 0.8	—	V
	V_{OH2}	SEG23-32		I_{OH2} = –10 mA	V_{DISP} – 0.8	—	V
	V_{OH3}	$\overline{GRID1-3}$		I_{OH3} = –5 mA	V_{DISP} – 0.8	—	V
	V_{OH4}	*2)	V_{DD} = 4.5 V	I_{OH4} = –200 μA	V_{DD} – 0.8	—	V
Low Level Output Voltage	V_{OL1}	SEG1-22	V_{DISP} = 9.5V	I_{OL1} = 500 μA	—	2.0	V
	V_{OL2}	SEG23-32		I_{OL2} = 500 μA	—	2.0	V
	V_{OL3}	$\overline{GRID1-3}$		I_{OL3} = 10 mA	—	2.0	V
	V_{OL4}	*2)	V_{DD} = 4.5 V	I_{OL4} = 200 μA	—	0.8	V
Supply Current	I_{DISP}	V_{DISP}	R = 10 kΩ±5%, C = 27 pF±5% no load		—	100	uA
	I_{DD}	V_{DD}			—	5.0	mA

*1) CS, CLOCK, DATA IN, DIM IN, SYNC IN 1, SYNC IN 2, M/$\overline{S}$, DUP/$\overline{TRI}$
*2) DIM OUT, SYNC OUT 1, SYNC OUT 2

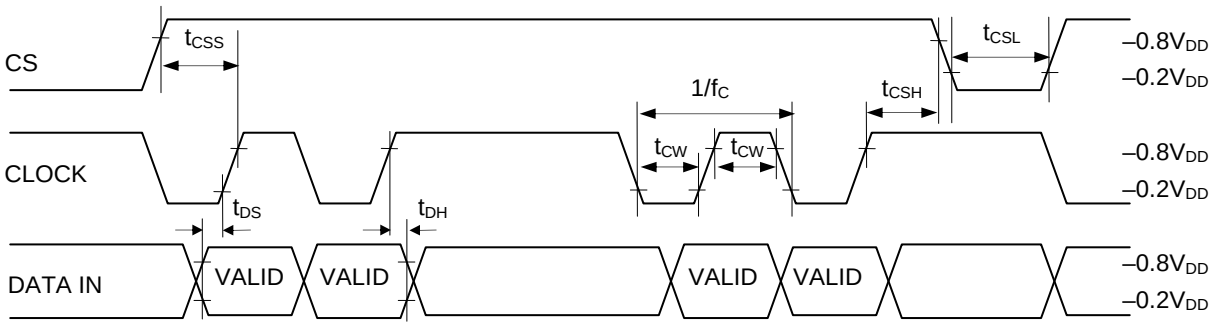
AC Characteristics

Ta = –40 to +105°C, V_{DISP} = 8.0 to 18.0 V, V_{DD} = 4.5 to 5.5 V

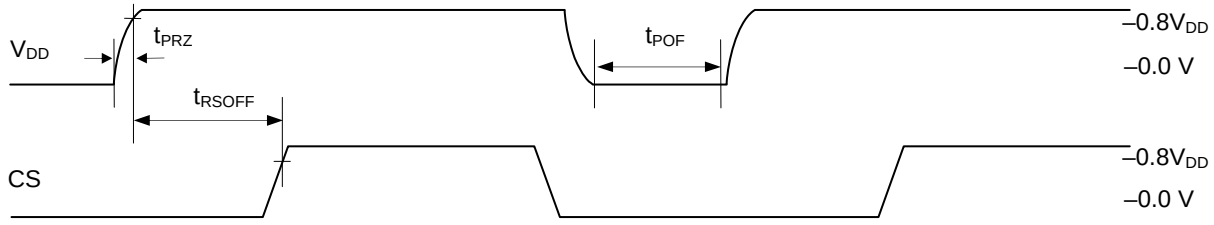
Parameter	Symbol	Condition		Min.	Max.	Unit
Clock Frequency	f_C	—		—	2.0	MHz
Clock Pulse Width	t_{CW}	—		200	—	ns
Data Setup Time	t_{DS}	—		200	—	ns
Data Hold Time	t_{DH}	—		200	—	ns
CS Off Time	t_{CSL}	—		20	—	µs
CS Setup Time (CS-Clock)	t_{CSS}	—		200	—	ns
CS Hold Time (Clock-CS)	t_{CSH}	—		200	—	ns
CS Wait Time	t_{RSOFF}	—		400	—	ns
Output Slew Rate Time	t_R	C_L = 100 pF	t_R = 20% to 80%	—	2.0	µs
	t_F		t_F = 80% to 20%	—	2.0	µs
V_{DD} Rise Time	t_{PRZ}	Mounted in a unit		—	100	µs
V_{DD} Off Time	t_{POF}	Mounted in a unit, V_{DD} = 0.0 V		5.0	—	ms

TIMING DIAGRAM

Data Input Timing

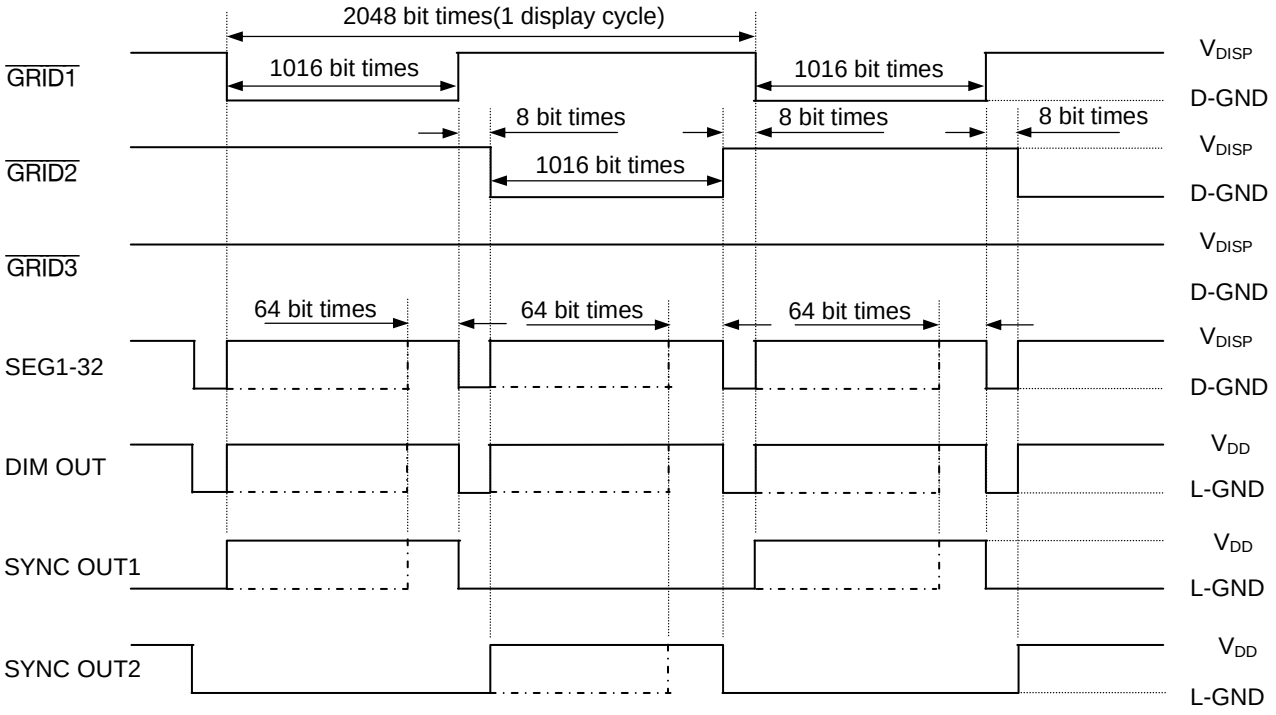


Reset Timing

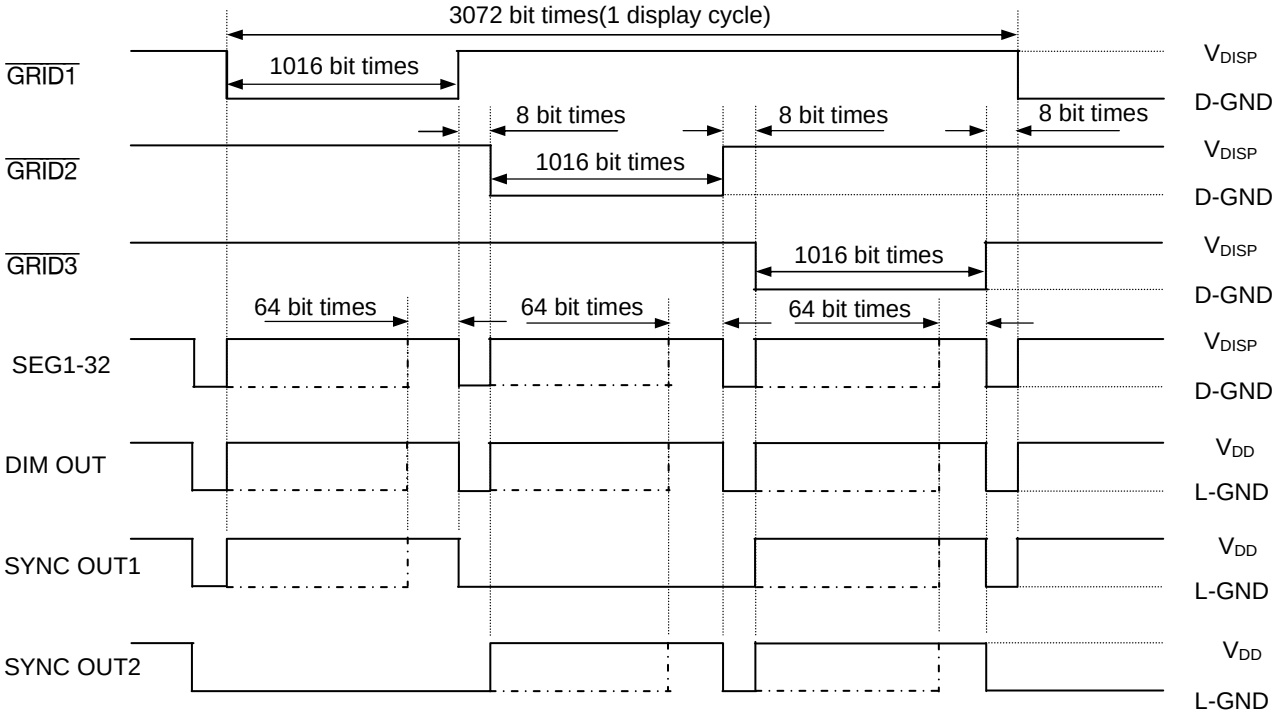


Driver Output Timing

Output Timing (Duplex Operation) *1bit time = 4/f_{osc}
Solid line : The dimming data is 1016/1024 at the master mode
Dotted line : The dimming data is 64/1024 at the master mode



Output Timing (Triplex Operation) *1bit time = 4/f_{osc}
Solid line : The dimming data is 1016/1024 at the master mode
Dotted line : The dimming data is 64/1024 at the master mode



FUNCTIONAL DESCRIPTION

Power-on Reset

When power is turned on, ML9212 is initialized by the internal power-on reset circuit.
The status of the internal circuit after initialization is as follows:

- The contents of the shift registers and latches are set to "0".
- The digital dimming duty cycle is set to "0".
- All segment outputs are set to Low level.
- $\overline{\text{GRID1}}$ outputs are set to Low level.
- $\overline{\text{GRID2}}$ to $\overline{3}$ outputs are set to High level.

Data Transfer Method

Data can be transferred between the rising edge and the next falling edge of chip select input.
The mode data, segment data and dimming data are written by a serial transfer method. The serial data is input to the shift register at the rising edge of a shift clock pulse.
The mode data (M0 to M2) must be transferred after the segment data and dimming data succeedingly.
When the chip select input falls, an internal LOAD signal is automatically generated and data is loaded to the latches.

Function Mode

Function mode is selected by the mode data (M0 to M2). The relation between function mode and mode data is as follows:

FUNCTION MODE	OPERATING MODE	FUNCTION DATA		
		M0	M1	M2
0	Segment Data for $\overline{\text{GRID1-3}}$ Input	0	0	0
1	Segment Data for $\overline{\text{GRID1}}$ Input	1	0	0
2	Segment Data for $\overline{\text{GRID2}}$ Input	0	1	0
3	Segment Data for $\overline{\text{GRID3}}$ Input	1	1	0
4	Digital Dimming Data Input	0	0	1

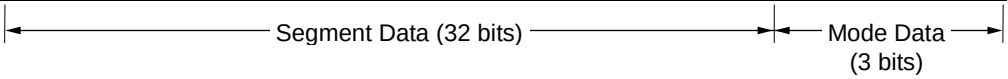
Segment Data Input [Function Mode: 0 to 3]

- ML9212 receives the segment data when function mode 0 to 3 are selected.
- The same segment data is transferred to the 3 segment data latches corresponding to $\overline{\text{GRID1}}$ to $\overline{3}$ at the same time when the function mode 0 is selected.
- The segment data is transferred to only one segment data latch corresponding to the specified GRID when the function mode is 1, 2 or 3 is selected.
- Segment output (SEG1 to 32) becomes High level (lightning) when the segment data (S1 to S32) is set to "1".

[Data Format]

Input Data : 35 bits
Segment Data : 32 bits
Mode Data : 3 bits

Bit	1	2	3	4	-------	29	30	31	32	33	34	35
Input DATA	S1	S2	S3	S4	-------	S29	S30	S31	S32	M0	M1	M2



[Bit correspondence between segment output and segment data]

SEG n	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Segment data	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
SEG n	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Segment data	S17	S18	S19	S20	S21	S22	S23	S24	S25	S26	S27	S28	S29	S30	S31	S32

Digital Dimming Data Input [Function Mode: 4]

- ML9212 receives the digital dimming data when function mode 4 is selected.
- The output duty changes in the range of 0/1024 (0%) to 1016/1024 (99.2%) for each grid.
- The 10-bit digital dimming data is input from LSB.

[Data Format]

Input Data : 13 bits
Digital Dimming Data : 10 bits
Mode Data : 3 bits

Bit	1	2	3	4	5	6	7	8	9	10	11	12	13
Input DATA	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	M0	M1	M2

LSB ← Digital Dimming Data (10 bits) → MSB ← Mode Data (3 bits) →

(LSB) Dimming Data (MSB)										Duty Cycle
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	
0	0	0	0	0	0	0	0	0	0	0/1024
1	0	0	0	0	0	0	0	0	0	1/1024
			⋮							⋮
1	1	1	0	1	1	1	1	1	1	1015/1024
0	0	0	1	1	1	1	1	1	1	1016/1024
1	0	0	1	1	1	1	1	1	1	1016/1024
			⋮							⋮
1	1	1	1	1	1	1	1	1	1	1016/1024

Master Mode

Master Mode is selected when M/$\overline{S}$ pin is set at High level. The master mode operation is as follows:

- The input levels of DIM IN, SYNC IN1 and SYNC IN2 are ignored, and these pins should be connected to L-GND or V_{DD}.
- The pulse width of $\overline{GRID1}$ to $\overline{3}$ and SEG1 to 32 are controlled by the internal digital dimming circuit.
- The segment Latch1 to 3 corresponding to $\overline{GRID1}$ to $\overline{3}$ are selected by the internal timing generator.

Slave Mode

Slave Mode is selected when M/$\overline{S}$ pin is set at Low level. The slave mode operation is as follows:

- The internal dimming circuit is ignored.
- The pulse width of SEG1 to 32 are controlled by the pulse width of DIM IN signal.
- The segment Latch1 to 3 corresponding to $\overline{GRID1}$ to $\overline{3}$ are selected by SYNC IN1 and SYNC IN2 signals.
- The output levels of $\overline{GRID1}$ to $\overline{3}$ are set at High level. The output levels of DIM OUT, SYNC OUT1 and SYNC OUT2 are set at Low level.

[Correspondence between SYNC IN1, 2 and Segment Latch1 to 3]

SYNC IN 1	SYNC IN 2	Segment Latch	GRID
0	0	No	No
1	0	Latch1	$\overline{GRID1}$
0	1	Latch2	$\overline{GRID2}$
1	1	Latch3	$\overline{GRID3}$

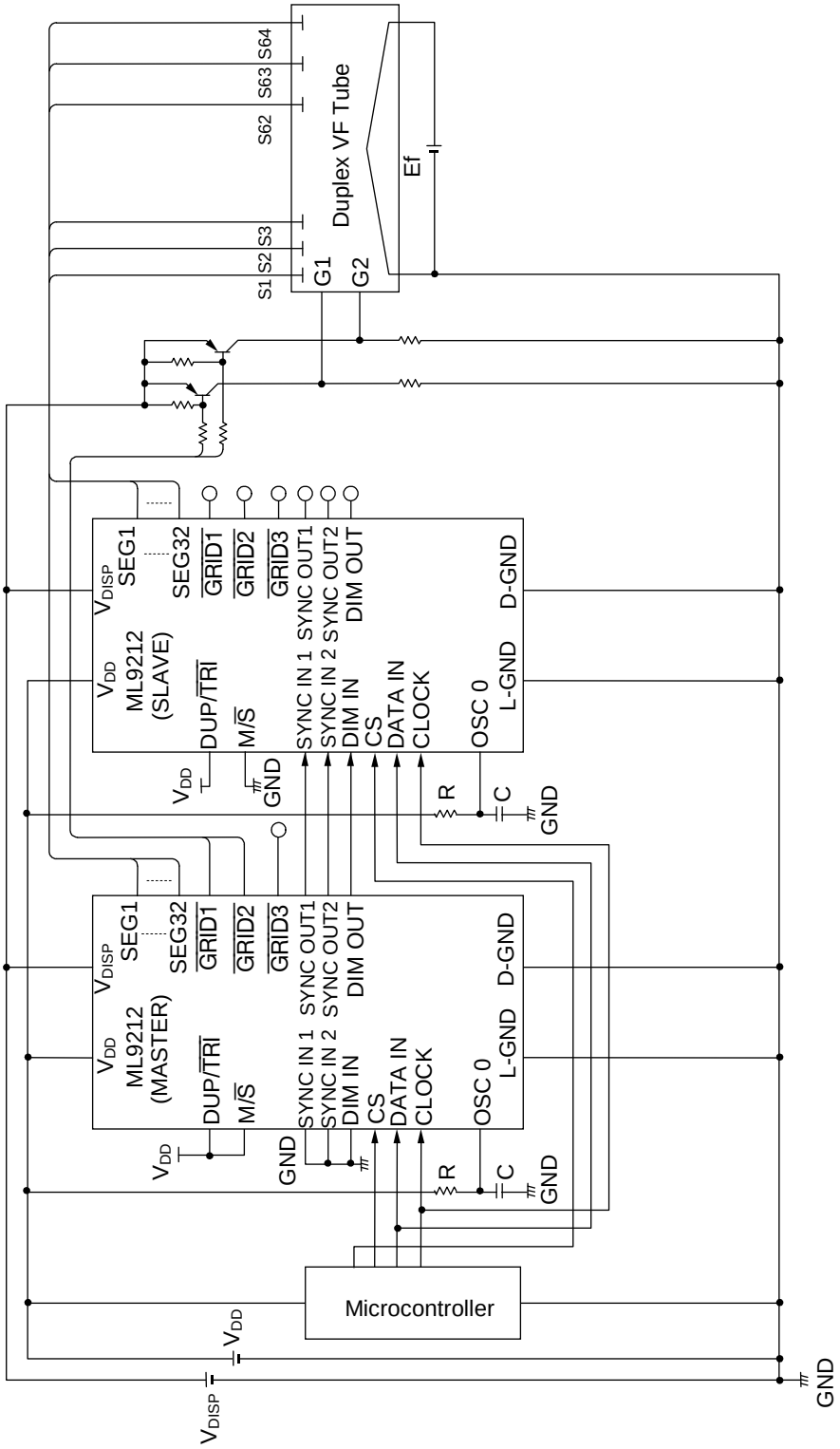
[Correspondence between DIM IN and SEG1 to 32]

DIM IN	SEG1 to 32
0	Low
1	High

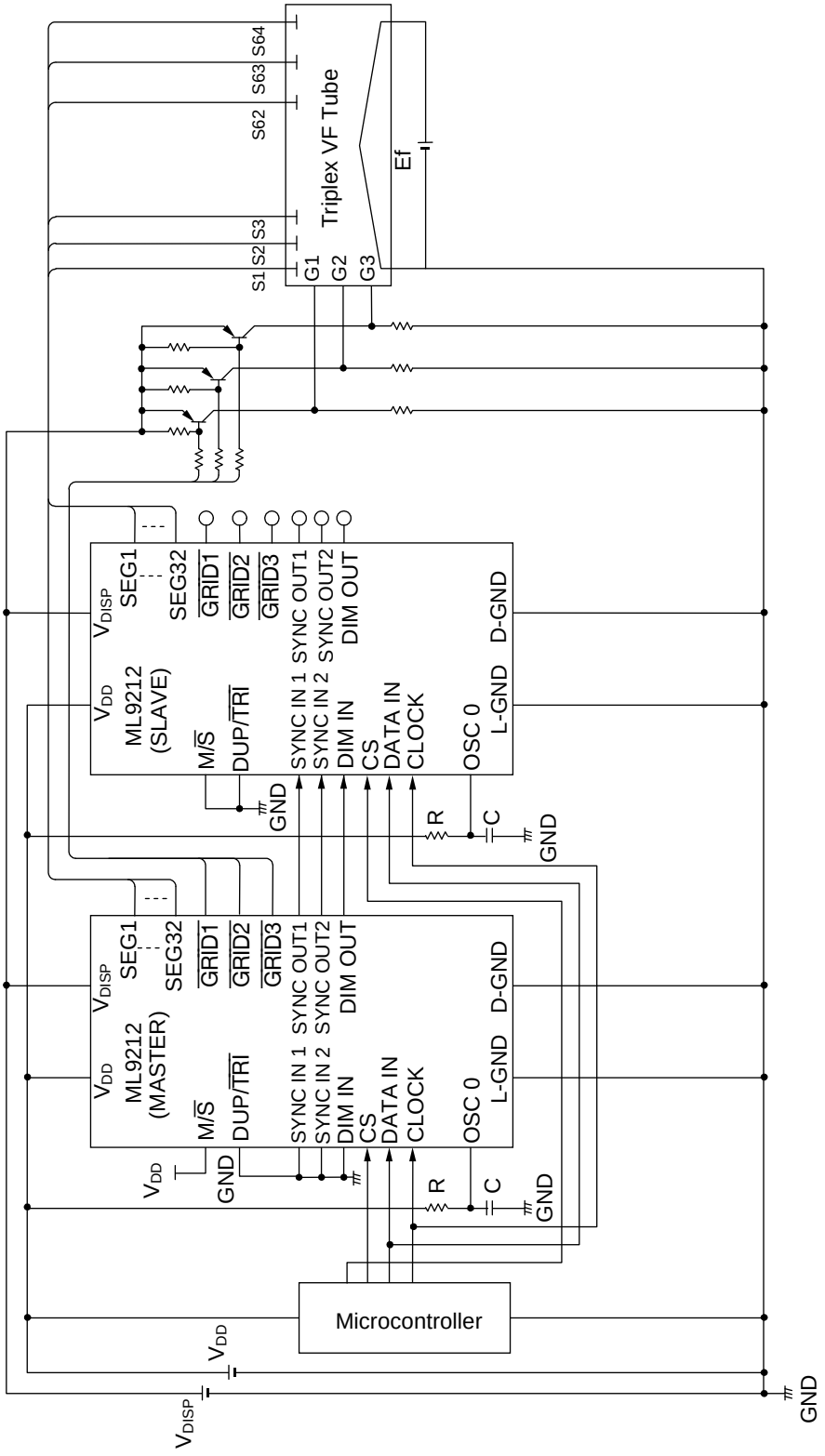
Note: Low: Lights OFF
High: Lights ON

APPLICATION CIRCUITS

1. Circuit for the duplex VFD tube with 128 segments (2 Grid × 64 Anode)

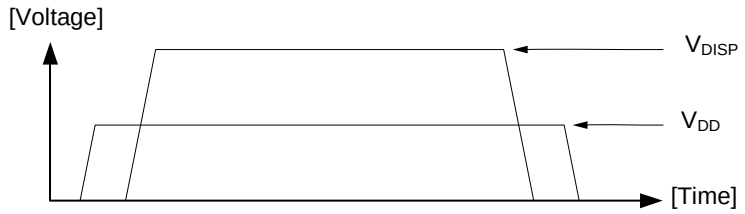


2. Circuit for the triplex VFD tube with 192 segments (3 Grid × 64 Anode)



NOTES ON TURNING POWER ON/OFF

- Connect L-GND and D-GND externally to be an equal potential voltage.
- To avoid wrong operations, turn on the driver power supply after turning on the logic power supply. Conversely, turn off the logic power supply after tuning off the driver power supply.



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9212-01	Nov., 26, 2002	–	–	Final edition 1

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