LAPIS Semiconductor

FEDL9209-01
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ML9209-xx

Vacuum fluorescent display tube controller driver

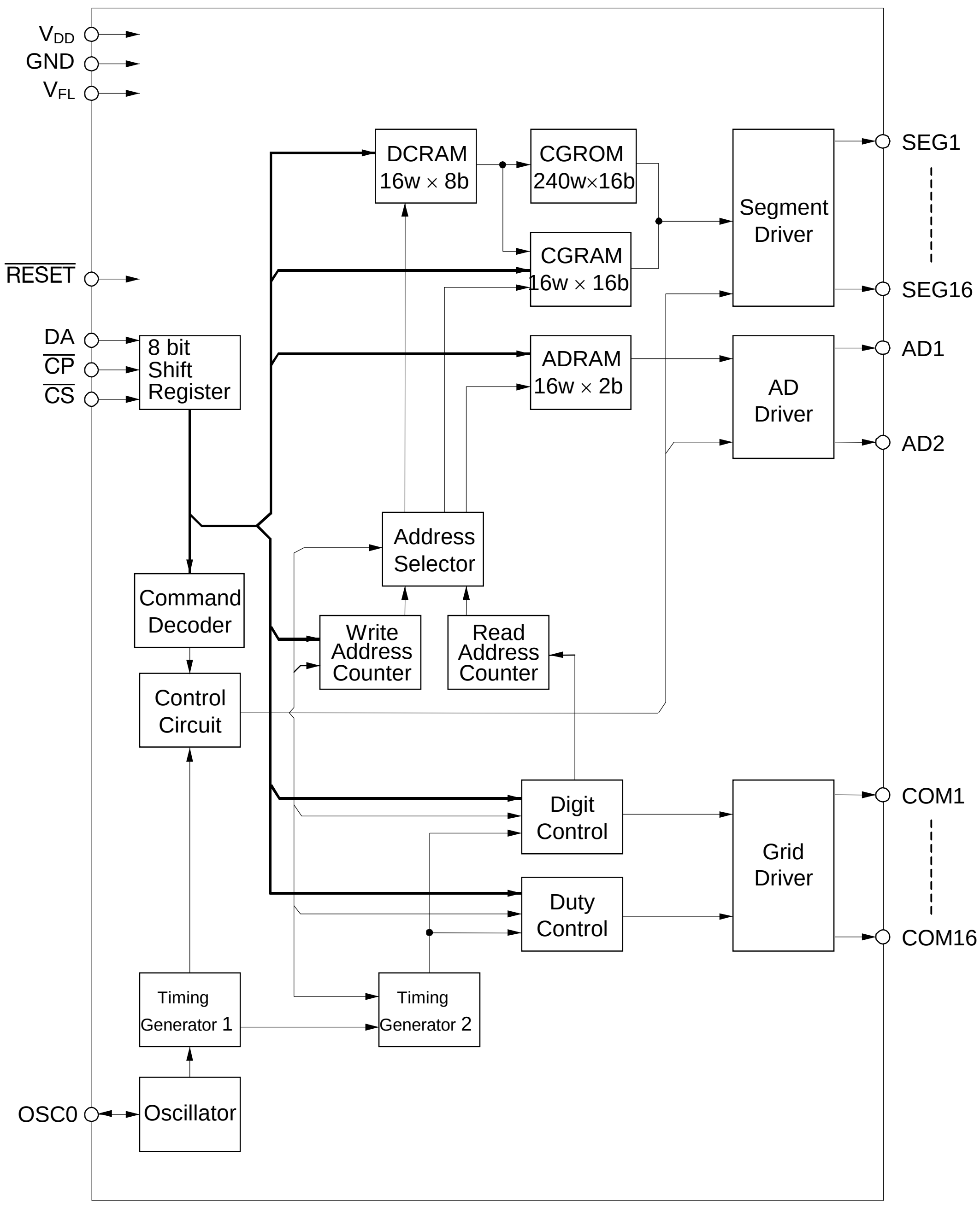
GENERAL DESCRIPTION

The ML9209-xx is an alphanumeric type vacuum fluorescent display (VFD) tube controller driver IC which can display alphanumeric characters, symbols, and bar charts.
Vacuum fluorescent display tube drive signals are generated by serial data sent from a micro-controller. A display system is easily realized by internal ROM and RAM for character display.
-01 is available as a general-purpose code.
Custom codes are provided on customer's request.

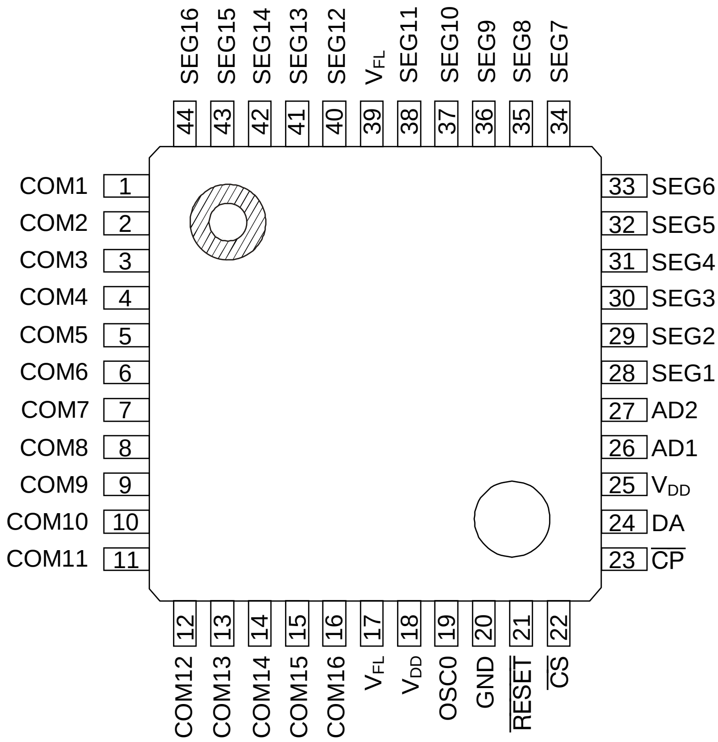
FEATURES

- Logic power supply and vacuum fluorescent display tube driving power supply (V_{DD})
  : 3.3 V±10% or 5.0 V±10%
- Vacuum fluorescent display tube driving power supply (V_{FL})
  : V_{DD} – 20 V to V_{DD} – 42 V
- VFD driver output current
  (VFD driver output can be connected directly to the VFD tube. No pull-down resistor is required.)
  - Segment driver (SEG1–16) : –6 mA ($V_{FL} = V_{DD} - 42$ V)
  - Segment driver (AD1, 2) : –15 mA ($V_{FL} = V_{DD} - 42$ V)
  - Grid driver (COM1–16) : –30 mA ($V_{FL} = V_{DD} - 42$ V)
- Content of display
  - CGROM : 16 segments 240 types (character data)
  - CGRAM : 16 segments 16 types (character data)
  - ADRAM : 16 (display digit)× 2 bits (symbol data)
  - DCRAM : 16 (display digit) × 8 bits (register for character data display)
- Display control function
  - Display digits : 1 to 16 digits
  - Display duty (brightness adjustment) : 16 stages
  - All display lights ON/OFF
- Four interfaces with microcontroller: DA, $\overline{CS}$, $\overline{CP}$, $\overline{RESET}$
- Instruction executable with 1 byte (excluding data write for each RAM)
- Built-in oscillation circuit (resistor & capacitor connected externally)
- Package options:
  44-pin plastic QFP (QFP44-P-910-0.80-2K) (ML9209-xxGA)

BLOCK DIAGRAM

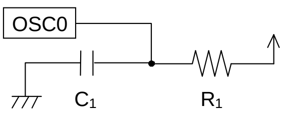


PIN CONFIGURATION (TOP VIEW)



44-Pin Plastic QFP

PIN DESCRIPTION

Pin	Symbol	Type	Connects to	Description
28–38, 40–44	SEG1–16	O	VFD tube anode electrode	VFD tube anode electrode drive output. Directly connected to the VFD tube and no pull-down resistor is required. $I_{OH} > -6$ mA
1–16	COM1–16	O	VFD tube grid electrode	VFD tube grid electrode drive output. Directly connected to the VFD tube and no pull-down resistor is required. $I_{OH} > -30$ mA
26, 27	AD1–2	O	VFD tube anode electrode	VFD tube anode electrode drive output. Directly connected to the VFD tube and no pull-down resistor is required. $I_{OH} > -15$ mA
18, 25	V_{DD}	—	Power supply	The voltage supply between V_{DD} and GND is for the power supply for the internal logic. The voltage supply between V_{DD} and V_{FL} is for the power supply for driving the VFD tube. Apply power to V_{DD} first, then to V_{FL}.
20	GND			
17,39	V_{FL}			
24	DA	I	Microcontroller	Serial data input pin (positive logic). Data is input from the LSB.
23	$\overline{CP}$	I	Microcontroller	Shift clock input pin. Serial data is shifted in on a rising edge of $\overline{CP}$.
22	$\overline{CS}$	I	Microcontroller	Chip select input pin. Serial data transfer is disabled when $\overline{CS}$ pin is “H” level.
21	$\overline{RESET}$	I	Microcontroller	Reset input. Setting this pin to “Low” initializes all the functions. Initial status is as follows. • Address of each RAM ....Address “00”H • Data of each RAM.....................Content is undefined • Display digit..............................16 digits • Brightness adjustment..............0/16 • All display lights ON or OFF......OFF mode • All outputs ....Low level
19	OSC0	I/O	C_1, R_1	Pin for RC oscillation. Resistors and capacitors are connected externally and constants vary depending on the V_{DD} voltage used. The target oscillation frequency is 2MHz.  (RC oscillator circuit) *Refer to the Application Circuit.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage (1)	V_{DD}	—	–0.3 to +6.5	V
Supply Voltage (2)	V_{FL}	—	V_{DD} – 45	V
Input Voltage	V_{IN}	—	–0.3 to V_{DD}+0.3	V
Power Dissipation	P_D	Ta ≥ 25°C	541	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C
Output Current	I_{O1}	COM1–16	–40 to 0.0	mA
	I_{O2}	AD1–2	–20 to 0.0	mA
	I_{O3}	SEG1–16	–10 to 0.0	mA

RECOMMENDED OPERATING CONDITIONS-1

• When the unit power supply voltage is 5.0 V (typ.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (1)	V_{DD}	—	4.5	5.0	5.5	V
Supply Voltage (2)	V_{FL}	—	V_{DD} –42	—	V_{DD}–20	V
High Level Input Voltage	V_{IH}	All input pins except OSC0	0.7 V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All input pins except OSC0	—	—	0.3 V_{DD}	V
$\overline{\text{CP}}$ frequency	f_C	—	—	—	2.0	MHz
Self-oscillation frequency	f_{OSC}	R_1 = 8.2 kΩ±5%, C_1 = 82 pF±5%	1.4	2.0	2.6	MHz
Frame Frequency	f_{FR}	DIGIT = 1 to16, R_1 = 8.2 kΩ±5%, C_1 = 82 pF±5%	170	244	318	Hz
Operating Temperature	T_{op}	—	–40	—	85	°C

RECOMMENDED OPERATING CONDITIONS-2

• When the unit power supply voltage is 3.3 V (typ.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (1)	V_{DD}	—	3.0	3.3	3.6	V
Supply Voltage (2)	V_{FL}	—	V_{DD}–42	—	V_{DD}–20	V
High Level Input Voltage	V_{IH}	All input pins except OSC0	0.8 V_{DD}	—	—	V
Low Level Input Voltage	V_{IL}	All input pins except OSC0	—	—	0.2 V_{DD}	V
$\overline{\text{CP}}$ frequency	f_C	—	—	—	2.0	MHz
Self-oscillation frequency	f_{OSC}	R_1 = 6.8 kΩ±5%, C_1 = 82 pF±5%	1.4	2.0	2.6	MHz
Frame Frequency	f_{FR}	DIGIT = 1 to 16, R_1 = 6.8 kΩ±5%, C_1 = 82 pF±5%	170	244	318	Hz
Operating Temperature	T_{op}	—	–40	—	85	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics-1

(V_{DD} = 5.0 V±10%, V_{FL} = V_{DD} – 42 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition		Min.	Max.	Unit
High Level Input Voltage	V_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—		0.7 V_{DD}	—	V
Low Level Input Voltage	V_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—		—	0.3 V_{DD}	V
High Level Input Current	I_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IH} = V_{DD}		–1.0	1.0	μA
Low Level Input Current	I_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IL} = 0.0 V		–1.0	1.0	μA
High Level Output Voltage	V_{OH1}	COM1–16	I_{OH1} = –30 mA		V_{DD} – 1.5	—	V
	V_{OH2}	AD1–2	I_{OH2} = –15 mA		V_{DD} – 1.5	—	V
	V_{OH3}	SEG1–16	I_{OH3} = –6 mA		V_{DD} – 1.5	—	V
Low Level Output Voltage	V_{OL1}	COM1–16 AD1–2 SEG1–16	—		—	V_{FL} + 1.0	V
Supply Current	I_{DD1}	V_{DD}	f_{OSC} = 2 MHz, no load	Duty = 15/16 Digit =1–16 All output lights ON	—	4	mA
	I_{DD2}			Duty = 0/16 Digit = 1–8 All output lights OFF	—	3	mA

DC Characteristics-2

(V_{DD} = 3.3 V±10%, V_{FL} = V_{DD} – 42 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Applied pin	Condition	Min.	Max.	Unit
High Level Input Voltage	V_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—	0.8 V_{DD}	—	V
Low Level Input Voltage	V_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	—	—	0.2 V_{DD}	V
High Level Input Current	I_{IH}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	$V_{IH} = V_{DD}$	–1.0	1.0	μA
Low Level Input Current	I_{IL}	$\overline{CS}$, $\overline{CP}$, DA, $\overline{RESET}$	V_{IL} = 0.0 V	–1.0	1.0	μA
High Level Output Voltage	V_{OH1}	COM1–16	I_{OH1} = –30 mA	V_{DD} – 1.5	—	V
	V_{OH2}	AD1–2	I_{OH2} = –15 mA	V_{DD} – 1.5	—	V
	V_{OH3}	SEG1–16	I_{OH3} = –6 mA	V_{DD} – 1.5	—	V
Low Level Output Voltage	V_{OL1}	COM1–16, AD1–2, SEG1–16	—	—	V_{FL} + 1.0	V
Supply Current	I_{DD1}	V_{DD}	f_{OSC} = 2 MHz, no load; Duty = 15/16, Digit =1–16, All output lights ON	—	3	mA
	I_{DD2}		f_{OSC} = 2 MHz, no load; Duty = 0/16, Digit = 1–8, All output lights OFF	—	2	mA

AC Characteristics-1

(V_{DD} = 5.0 V±10%, V_{FL} = V_{DD} – 42 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequency	f_C	—		—	2.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		250	—	ns
DA Setup Time	t_{DS}	—		250	—	ns
DA Hold Time	t_{DH}	—		250	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		250	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	R_1 = 8.2 kΩ±5%, C_1 = 82 pF±5%		16	—	μs
$\overline{CS}$ Wait Time	t_{CSW}	—		250	—	ns
Data Processing Time	t_{DOFF}	R_1 = 8.2 kΩ±5%, C_1 = 82 pF±5%		8	—	μs
$\overline{RESET}$ Pulse Width	t_{WRES}	—		250	—	ns
$\overline{RESET}$ Time	t_{RSON}	—		250	—	ns
DA Wait Time	t_{RSOFF}	—		250	—	ns
All Driver Output Slew Rate	t_R	C_l = 100 pF	t_R = 20 to 80%	—	2.0	μs
	t_F		t_F = 80 to 20%	—	2.0	μs

AC Characteristics-2

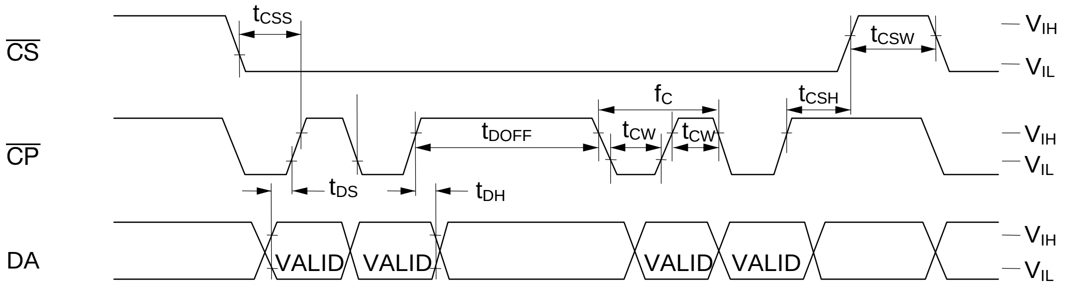
(V_{DD} = 3.3 V±10%, V_{FL} = V_{DD} – 42 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Max.	Unit
$\overline{CP}$ Frequency	f_C	—		—	2.0	MHz
$\overline{CP}$ Pulse Width	t_{CW}	—		250	—	ns
DA Setup Time	t_{DS}	—		250	—	ns
DA Hold Time	t_{DH}	—		250	—	ns
$\overline{CS}$ Setup Time	t_{CSS}	—		250	—	ns
$\overline{CS}$ Hold Time	t_{CSH}	R_1 = 6.8 kΩ±5%, C_1 = 82 pF±5%		16	—	μs
$\overline{CS}$ Wait Time	t_{CSW}	—		250	—	ns
Data Processing Time	t_{DOFF}	R_1 = 6.8 kΩ±5%, C_1 = 82 pF±5%		8	—	μs
$\overline{RESET}$ Pulse Width	t_{WRES}	—		250	—	ns
$\overline{RESET}$ Execution Time	t_{RSON}	—		250	—	ns
DA Wait Time	t_{RSOFF}	—		250	—	ns
All Driver Output Slew Rate	t_R	C_l = 100 pF	t_R = 20 to 80%	—	2.0	μs
	t_F		t_F = 80 to 20%	—	2.0	μs

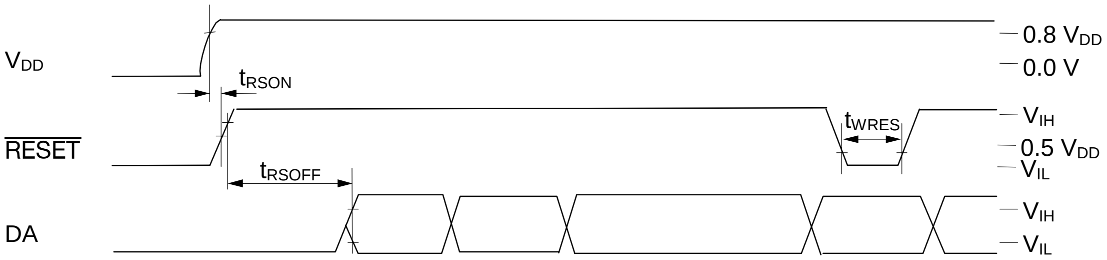
TIMING DIAGRAMS

1) Data Input Timing

Symbol	V_{DD} = 3.3 V ±10%	V_{DD} = 5.0 V ±10%
V_{IH}	0.8 V_{DD}	0.7 V_{DD}
V_{IL}	0.2 V_{DD}	0.3 V_{DD}

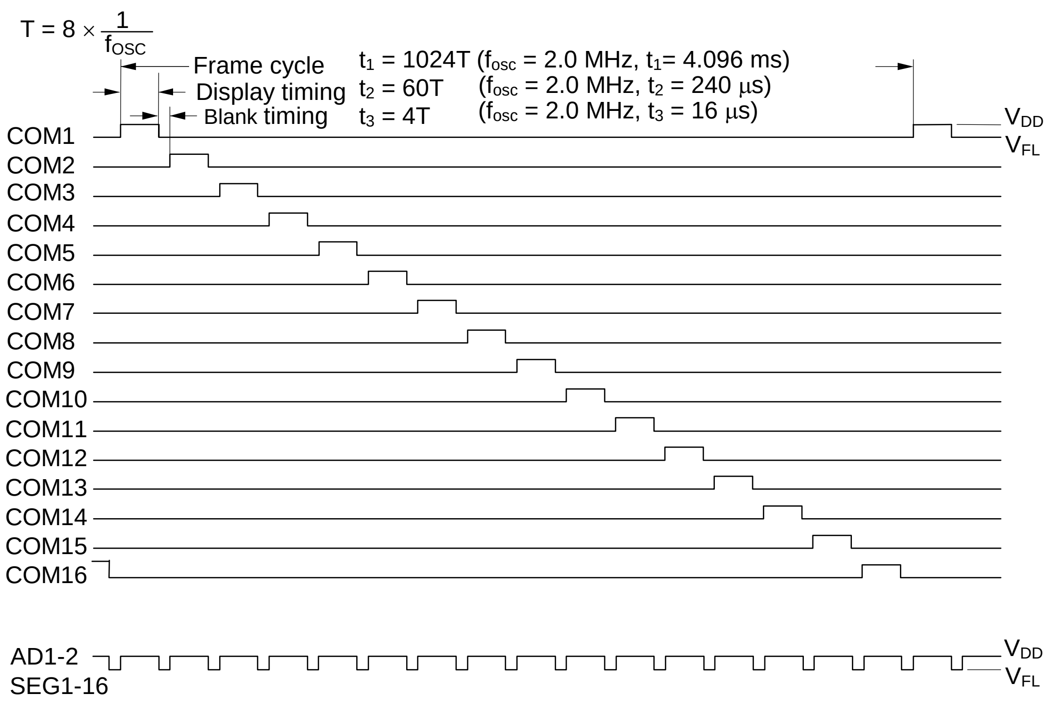


2) Data Input Timing



3) Output Timing

4) Digit Output Timing (16-Digit, 15/16-Duty)



FUNCTIONAL DESCRIPTION

Command List

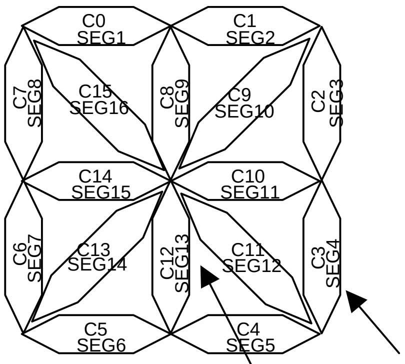
	Command	LSB		First byte					MSB	LSB		Second byte					MSB	
		B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
1	DCRAM data write	X0	X1	X2	X3	1	0	0	0	C0	C1	C2	C3	C4	C5	C6	C7	
2	CGRAM data write	X0	X1	X2	X3	0	1	0	0	C0	C1	C2	C3	C4	C5	C6	C7	2nd byte
										C8	C9	C10	C11	C12	C13	C14	C15	3rd byte
3	ADRAM data write	X0	X1	X2	X3	1	1	0	0	C0	C1	*	*	*	*	*	*	
5	Display duty set	D0	D1	D2	D3	1	0	1	0									
6	Number of digits set	K0	K1	K2	K3	0	1	1	0									
7	All display lights ON/OFF	L	H	*	*	1	1	1	0									
	Others (test mode)																	

* : Don’t care
Xn : Address setting for each RAM
Cn : Character code setting for each RAM
Dn : Display duty setting
Kn : Setting of the number of display digits
H : All display lights ON setting
L : All display lights OFF setting

When data is written to RAM (DCRAM, CGRAM, and ADRAM) continuously, addresses are internally incremented automatically. Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and subsequent bytes.

Note: The test mode is used for inspection before shipment. It is not a user function.

Positional Relationship Between SEGn and ADn (one digit)



C0–7: Corresponds to the 2nd byte of the CGRAM data write command.

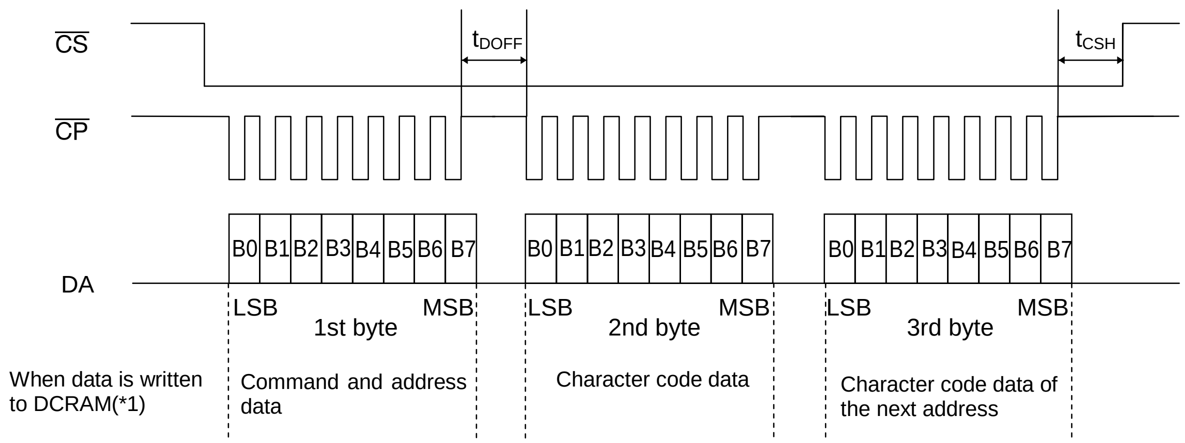
C8–15: Corresponds to the 3rd byte of the CGRAM data write command.

Data Transfer Method and Command Write Method

Display control command and data are written by an 8-bit serial transfer.
Write timing is shown in the figure below.

Setting the $\overline{\mathrm{CS}}$ pin to “Low” level enables a data transfer.
Data is 8 bits and is sequentially input into the DA pin from LSB (LSB first).
As shown in the figure below, data is read by the shift register at the rising edge of the shift clock, which is input into the $\overline{\mathrm{CP}}$ pin. If 8-bit data is input, internal load signals are automatically generated and data is written to each register and RAM.
Therefore it is not necessary to input load signals from the outside.

Setting the $\overline{\mathrm{CS}}$ pin to “High” disables data transfer. Data input from the point when the $\overline{\mathrm{CS}}$ pin changes from “High” to “Low” is recognized in 8-bit units.



*1 When data is written to RAM (DCRAM, CGRAM, ADRAM) continuously, addresses are internally incremented automatically. Therefore it is not necessary to specify the 1st byte to write RAM data for the 2nd and subsequent bytes.

Reset Function

Reset is executed when the $\overline{\mathrm{RESET}}$ pin is set to “L”, (when turning power on, for example) and initializes all functions.
Initial status is as follows.

- Address of each RAM.......................Address 00H
- Data of each RAM ....All contents are undefined.
- Number of display digits...................16 digits
- Brightness adjustment 0/16
- All display lights ON or OFF............OFF mode
- Segment output..................................All segment outputs go “Low.”
- AD output..All AD outputs go “Low.”

Be sure to execute the reset operation when turning power on and set again according to “Setting Flowchart” after reset.

Description of Commands and Functions

1. "DCRAM data write" command
   (Specifies the address of DCRAM and writes the character code of CGROM and CGRAM.)

DCRAM (Data Control RAM) has a 4-bit address to store character codes of CGROM and CGRAM.
A character code specified by DCRAM is converted to an alphanumeric character pattern via CGROM or CGRAM.
The DCRAM can store 16 characters worth of character codes.

[Command format]

	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
1st byte (1st)	X0	X1	X2	X3	1	0	0	0	: Setup and DCRAM address in the write mode of DCRAM data are specified. (Example: Specify DCRAM address 0H.)
2nd byte (2nd)	C0	C1	C2	C3	C4	C5	C6	C7	: Specify character code of CGROM and CGRAM. (It is written into DCRAM address 00H.)

To specify the character code of CGROM and CGRAM to the next address continuously, specify only character code as follows.
Since the address of DCRAM is automatically incremented, address specification is unnecessary.

	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
2nd byte (3rd)	C0	C1	C2	C3	C4	C5	C6	C7	: Specify character code of CGROM and CGRAM. (It is written into DCRAM address 1H.)
2nd byte (4th)	C0	C1	C2	C3	C4	C5	C6	C7	: Specify character code of CGROM and CGRAM. (It is written into DCRAM address 2H.)
⋮									
2nd byte (17th)	C0	C1	C2	C3	C4	C5	C6	C7	: Specify character code of CGROM and CGRAM. (It is written into DCRAM address FH.)
2nd byte (18th)	C0	C1	C2	C3	C4	C5	C6	C7	: Specify character code of CGROM and CGRAM. (It is rewritten into DCRAM address 0H.)

X0 (LSB) to X3 (MSB): DCRAM address (4 bits: 16 characters worth)
C0 (LSB) to C7 (MSB): Character code of CGROM and CGRAM (8 bits: 256 characters worth)

[Relationship between DCRAM addresses setup and COM positions]

HEX	X0	X1	X2	X3	COM position	HEX	X0	X1	X2	X3	COM position
0	0	0	0	0	COM1	8	0	0	0	1	COM9
1	1	0	0	0	COM2	9	1	0	0	1	COM10
2	0	1	0	0	COM3	A	0	1	0	1	COM11
3	1	1	1	0	COM4	B	1	1	0	1	COM12
4	0	0	1	0	COM5	C	0	0	1	1	COM13
5	1	0	1	0	COM6	D	1	0	1	1	COM14
6	0	1	1	0	COM7	E	0	1	1	1	COM15
7	1	1	1	0	COM8	F	1	1	1	1	COM16

2. "CGRAM data write" command
(Specifies the address of CGRAM and writes character pattern data.)

CGRAM (Character Generator RAM) has a 4-bit address to store alphanumeric character patterns.
A character pattern stored in CGRAM can be displayed by specifying the character code (address) by DCRAM.
The addresses of CGRAM are assigned to 00H to 0FH (All the other addresses are the CGROM addresses).
The CGRAM can store 16 types of character patterns.

[Command format]

	B0 (LSB)	B1	B2	B3	B4	B5	B6	B7 (MSB)	
1st byte (1st)	X0	X1	X2	X3	0	1	0	0	: Setup and CGRAM address in the write-in mode of CGRAM data are specified. (Example: Specify CGRAM address 00H.)
2nd byte (2nd)	C0	C1	C2	C3	C4	C5	C6	C7	: Specify 1st-column data. (It is written into CGRAM address 00H.)
3rd byte (3rd)	C8	C9	C10	C11	C12	C13	C14	C15	: Specify 2nd-column data. (It is written into CGRAM address 00H.)

To specify character pattern data continuously to the next address, specify only character pattern data as follows.
Since the address of CGRAM is automatically incremented, address specification is unnecessary.
Data from the 2nd to 6th byte (character pattern) is regarded as one data item taken together, so 250 ns is sufficient for t_{DOFF} time between bytes.

	B0 (LSB)	B1	B2	B3	B4	B5	B6	B7 (MSB)	
2nd byte (4th)	C0	C1	C2	C3	C4	C5	C6	C7	: Specify 1st-column data. (It is written into CGRAM address 01H.)
3rd byte (5th)	C8	C9	C10	C11	C12	C13	C14	C15	: Specify 2nd-column data. (It is written into CGRAM address 01H.)

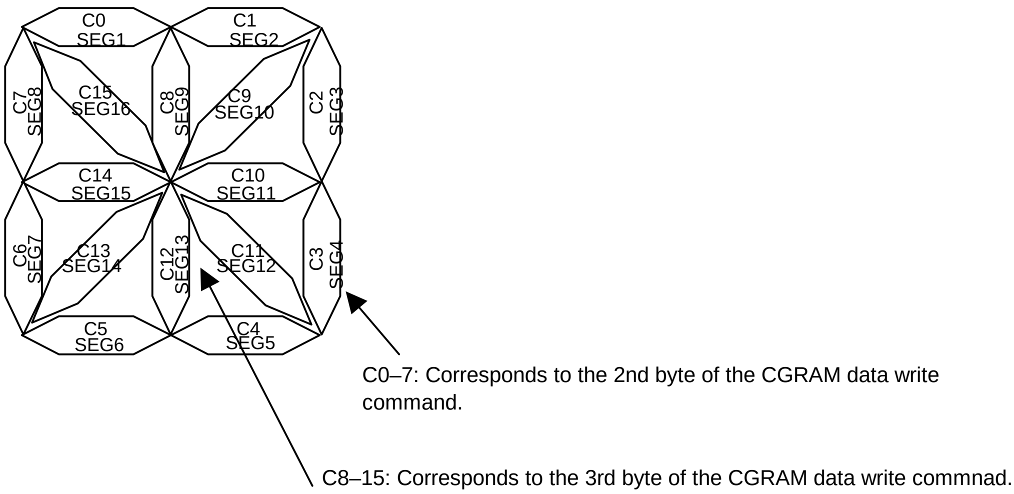
X0 (LSB) to X3 (MSB): CGRAM address (4 bits: 16 characters worth)
C0 (LSB) to C15 (MSB): Character data of CGRAM (16 bits: 16 outputs per digit)

[Positional relationship between CGRAM addresses setup and CGROM addresses]

HEX	X0	X1	X2	X3	CGROM address	HEX	X0	X1	X2	X3	CGROM address
0	0	0	0	0	RAM00	8	0	0	0	1	RAM08
1	1	0	0	0	RAM01	9	1	0	0	1	RAM09
2	0	1	0	0	RAM02	A	0	1	0	1	RAM0A
3	1	1	1	0	RAM03	B	1	1	0	1	RAM0B
4	0	0	1	0	RAM04	C	0	0	1	1	RAM0C
5	1	0	1	0	RAM05	D	1	0	1	1	RAM0D
6	0	1	1	0	RAM06	E	0	1	1	1	RAM0E
7	1	1	1	0	RAM07	F	1	1	1	1	RAM0F

Refer to the ROM Code Tables attached later in this document.

Positional Relationship Between CGROM and CGRAM outputs



*On CGROM

A CGROM (Character Generator ROM) has an 8-bit address to generate alphanumeric type matrix character patterns.

It has a capacity of 240 x 16 bits and can store 240 types of character patterns.

3. "ADRAM data write" command
   (Specifies the address of ADRAM and writes symbol data)

ADRAM (Additional Data RAM) has a 2-bit address to store symbol data.
Symbol data specified by ADRAM is directly output without CGROM and CGRAM.
(The ADRAM can store two types of symbol patterns for each digit.)
The terminal to which the contents of ADRAM are output can be used as a cursor.

[Command format]

	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
1st byte (1st)	X0	X1	X2	X3	1	1	0	0	: Setup and DCRAM address in the write-in mode of DCRAM data are specified. (Example: Specify ADRAM address 0H.)
	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
2nd byte (2nd)	C0	C1	*	*	*	*	*	*	: Specify symbol data. (Example: Specify ADRAM address 0H.)

To specify symbol data continuously to the next address, specify only symbol data as follows.
Since the address of ADRAM is automatically incremented, address specification is unnecessary.

	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
2nd byte (3rd)	C0	C1	*	*	*	*	*	*	: Specify symbol data. (It is written into ADRAM address 1H.)
	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
2nd byte (4th)	C0	C1	*	*	*	*	*	*	: Specify symbol data. (It is written into ADRAM address 2H.)
	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
2nd byte (17th)	C0	C1	*	*	*	*	*	*	: Specify symbol data. (It is written into ADRAM address FH.)
	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
2nd byte (18th)	C0	C1	*	*	*	*	*	*	: Specify symbol data. (It is rewritten into ADRAM address 0H.)

X0 (LSB) to X3 (MSB) : ADRAM address (4 bits: 16 characters worth)
C0 (LSB) to C1 (MSB) : Symbol data (2 bits: 2 symbols per digit)
* : Don't care

[Relationship between ADRAM addresses setup and COM positions]

HEX	X0	X1	X2	X3	COM positions	HEX	X0	X1	X2	X3	COM positions
0	0	0	0	0	COM1	8	0	0	0	1	COM9
1	1	0	0	0	COM2	9	1	0	0	1	COM10
2	0	1	0	0	COM3	A	0	1	0	1	COM11
3	1	1	1	0	COM4	B	1	1	0	1	COM12
4	0	0	1	0	COM5	C	0	0	1	1	COM13
5	1	0	1	0	COM6	D	1	0	1	1	COM14
6	0	1	1	0	COM7	E	0	1	1	1	COM15
7	1	1	1	0	COM8	F	1	1	1	1	COM16

5. "Display duty set" command
   (Writes display duty value into the duty cycle register.)

For display duty, brightness can be adjusted in 16 stages using 4-bit data.
When power is turned on or when the $\overline{\text{RESET}}$ signal is input, the duty cycle register value is "0". Always execute this command before turning the display on, then set a desired duty value.

[Command format]

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7
1st byte	D0	D1	D2	D3	1	0	1	0

: setup and duty value in display duty specification mode are specified.

D0 (LSB) to D3 (MSB) : Display duty data (4 bits: 16 stages worth)

[Relation between setup data and controlled COM duty]

HEX	D0	D1	D2	D3	COM duty	HEX	D0	D1	D2	D3	COM duty
0	0	0	0	0	0/16	0	0	0	0	1	8/16
1	1	0	0	0	1/16	1	1	0	0	1	9/16
2	0	1	0	0	2/16	2	0	1	0	1	10/16
3	1	1	0	0	3/16	3	1	1	0	1	11/16
4	0	0	1	0	4/16	4	0	0	1	1	12/16
5	1	0	1	0	5/16	5	1	0	1	1	13/16
6	0	1	1	0	6/16	6	0	1	1	1	14/16
7	1	1	1	0	7/16	7	1	1	1	1	15/16

* The state when power is turned on or when the $\overline{\text{RESET}}$ signal is input.

6. “Number of display digits set” command
(Writes the number of display digits into the number-of-display-digits register.)

For the number of display digits, 1 to 16 digits can be specified using 4-bit data.
When power is turned on or when a $\overline{\text{RESET}}$ signal is input, the number-of-display-digits register value is “0”. Always execute this command before turning the display on, then set a desired value.

[Command format]

	B0 (LSB)	B1	B2	B3	B4	B5	B6	B7 (MSB)	
1st byte	K0	K1	K2	K3	0	1	1	0	: Setup in display digits specification mode and digits value is specified.

K0 (LSB) to K3 (MSB) : Data of the number of display digits (4 bits: 16 digits worth)

[Relation between data to be set and the number of digits of COM to be controlled]

HEX	D0	D1	D2	D3	No. of digits of COM	HEX	D0	D1	D2	D3	No. of digits of COM
0*	0	0	0	0	COM1–16	0	0	0	0	1	COM1–18
1	1	0	0	0	COM1	1	1	0	0	1	COM1–9
2	0	1	0	0	COM1–2	2	0	1	0	1	COM1–10
3	1	1	0	0	COM1–3	3	1	1	0	1	COM1–11
4	0	0	1	0	COM1–4	4	0	0	1	1	COM1–12
5	1	0	1	0	COM1–5	5	1	0	1	1	COM1–13
6	0	1	1	0	COM1–6	6	0	1	1	1	COM1–14
7	1	1	1	0	COM1–7	7	1	1	1	1	COM1–15

* The state when power is turned on or when the $\overline{\text{RESET}}$ signal is input.

7. “All display lights ON” and “All display lights OFF” commands
   (Turns the entire display ON and OFF, respectively.)

All display lights ON is used primarily for display testing.
All display lights OFF is primarily used for display blink and to prevent false display upon power-on.

[Command format]

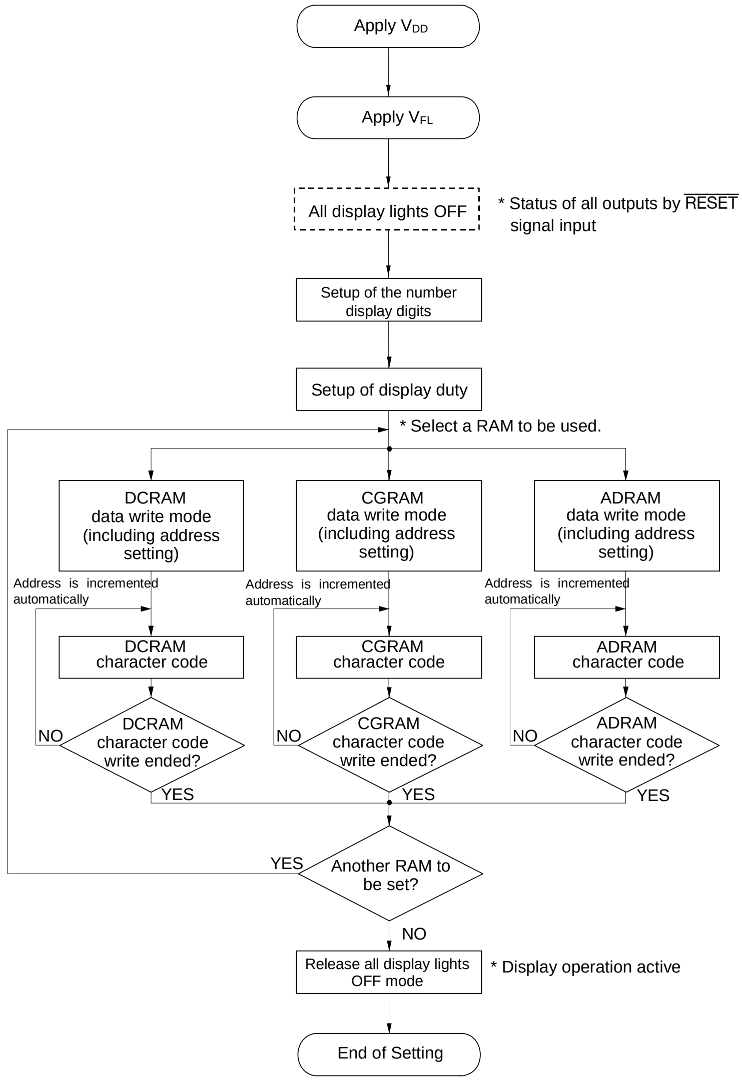
	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte	L	H	*	*	1	1	1	0	: Select all display lights ON or OFF and specify their operation.

L: All display lights OFF
H: All display lights ON
* : Don’t Care

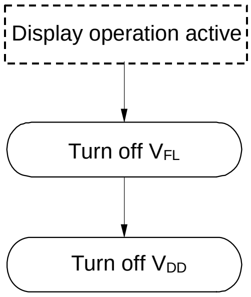
[Data to be setup and display state of SEG and AD]

L	H	Display state of SEG and AD	
0	0	Normal display	
1	0	Sets all outputs to Low	* The state when power is turned on or when $\overline{\text{RESET}}$ signal is input
0	1	Sets all outputs to High	
1	1	Sets all outputs to High	* Priority is given to the All display lights ON command.

Setting Flowchart
(Power applying included)

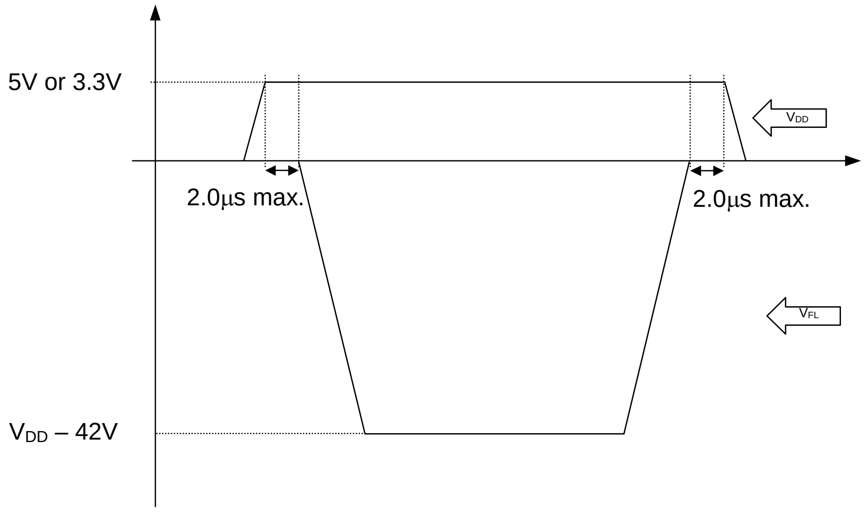


Power-off Flowchart

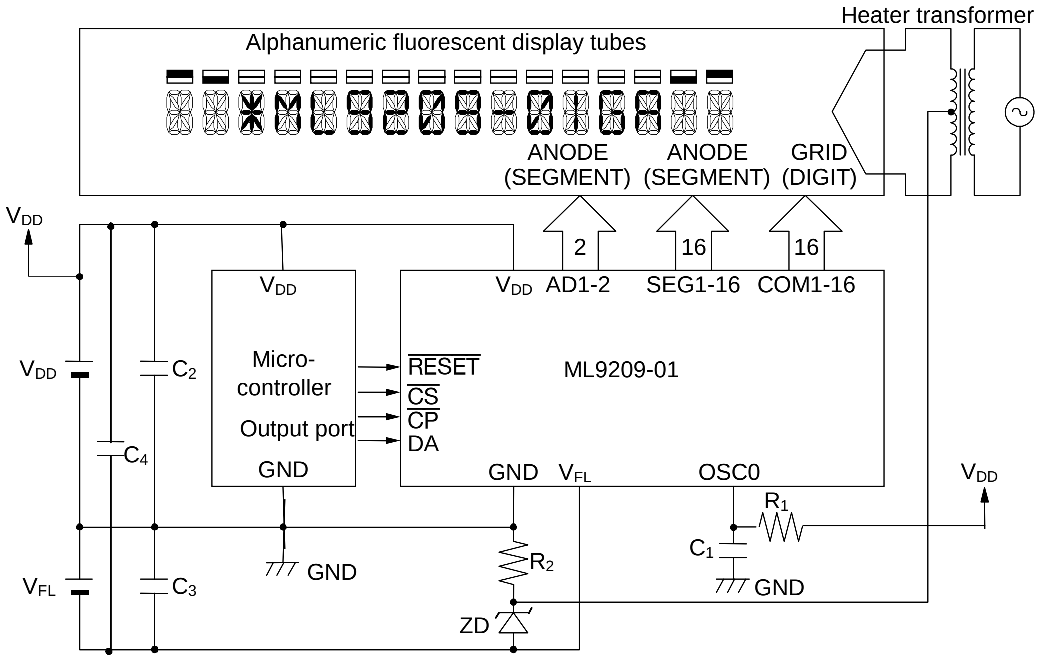


NOTE ON APPLYING POWER

To prevent the IC from malfunctioning, turn on the logic power supply first, and then turn on the driver power supply when applying power. Also, for power-off, turn off the driver power supply first, then turn off the logic power supply.



APPLICATION CIRCUIT



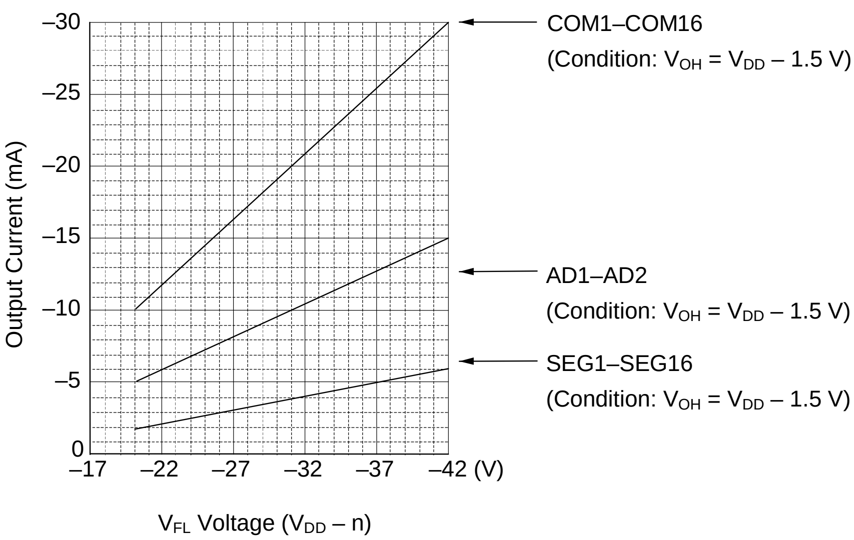
Notes:

1. The V_{DD} voltage depends on the power supply voltage of the microcontroller used. Adjust the value of the constants R_1 and C_1 to the power supply voltage used.

2. The V_{FL} voltage depends on the vacuum fluorescent display tube used. Adjust the value of the constants R_2 and ZD to the voltage used.

Reference data

Shown below is a chart showing the V_{FL} voltage vs. output current of each driver.
Care must be taken that the entire power consumption will not exceed the power dissipation.

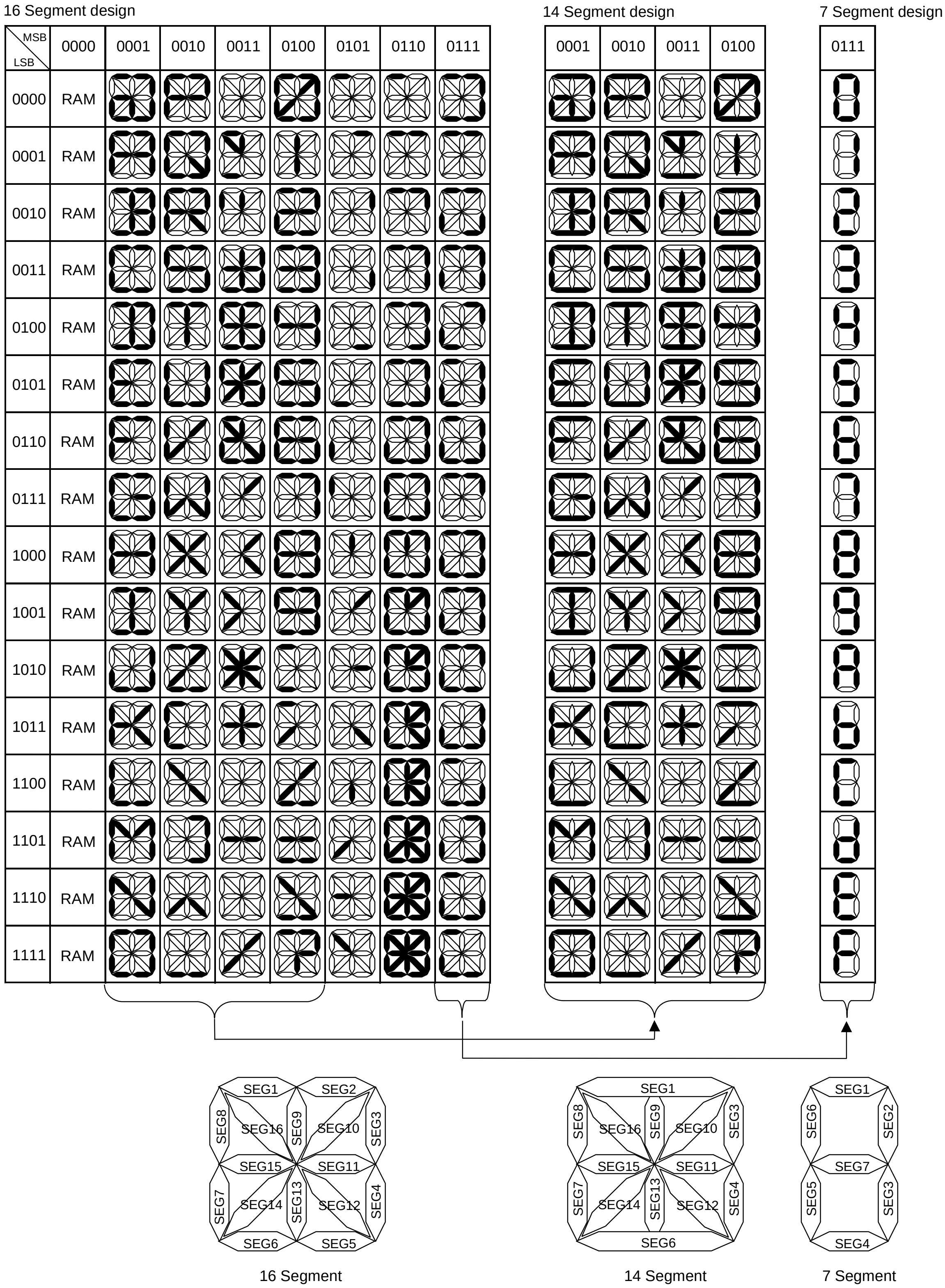


V_{FL} Voltage vs. Output Current of Each Driver

ML9209-01 ROM CODE

*ROM CODE_A is the character set for SEGA1 to SEGA16.
*00000000b(00h) to 00001111b(0Fh) are the CGRAM_A addresses

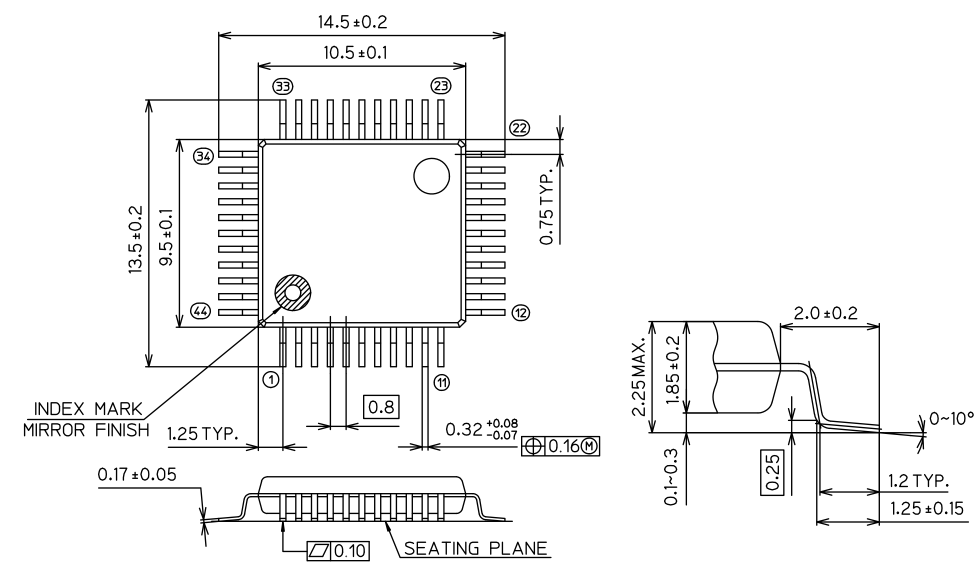
MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM															
0001	RAM															
0010	RAM															
0011	RAM															
0100	RAM															
0101	RAM															
0110	RAM															
0111	RAM															
1000	RAM															
1001	RAM															
1010	RAM															
1011	RAM															
1100	RAM															
1101	RAM															
1110	RAM															
1111	RAM															


16 Segment design
14 Segment design
7 Segment design
MSB
LSB
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
RAM
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG8
SEG9
SEG10
SEG11
SEG12
SEG13
SEG14
SEG15
SEG16
16 Segment
14 Segment
7 Segment

PACKAGE DIMENSIONS

(Unit: mm)

QFP44-P-910-0.80-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Sn/Pb
Package weight (g)	0.41 TYP.
Rev. No./Last Revised	5/Nov. 20, 2002

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9209-01	Oct. 20, 2004	—	—	Final edition 1

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