FEDL7029-03
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OKI Semiconductor

ML7029

Multifunction ADPCM CODEC

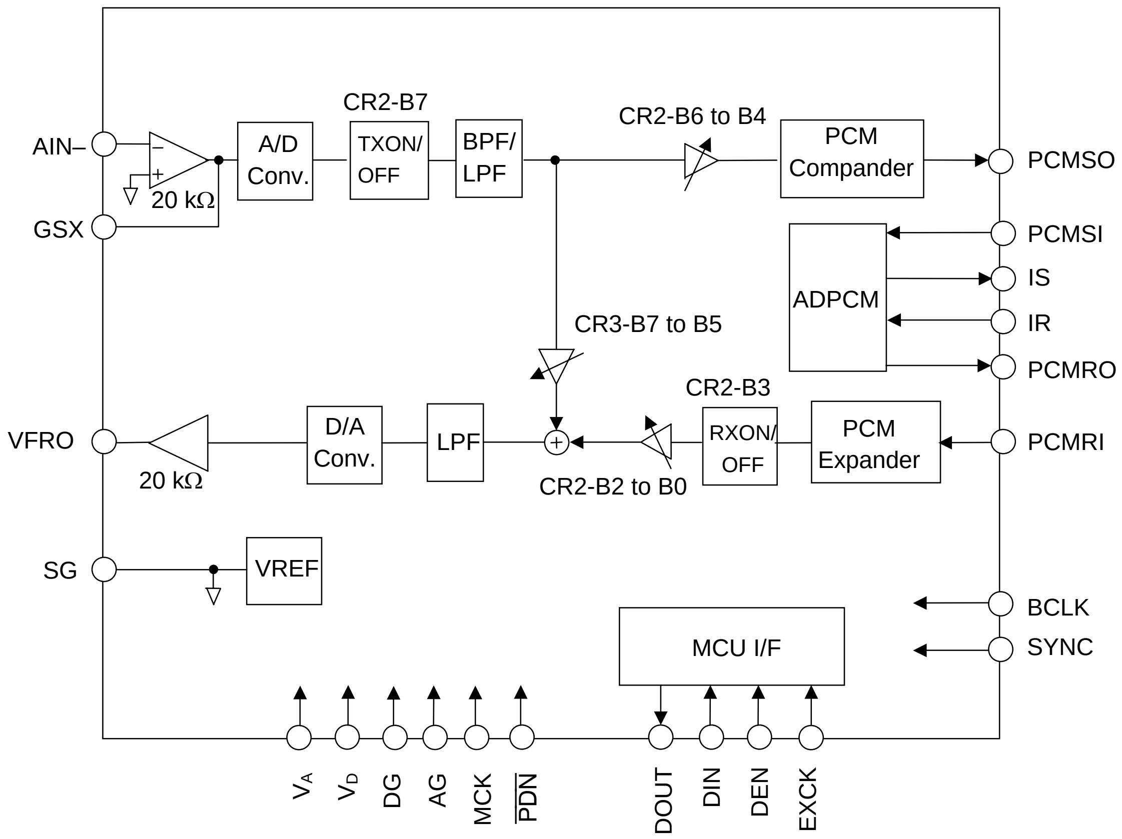
GENERAL DESCRIPTION

The ML7029 is a single channel ADPCM CODEC IC which performs mutual transcoding between the analog voice band signal and 32 kbps ADPCM serial data.

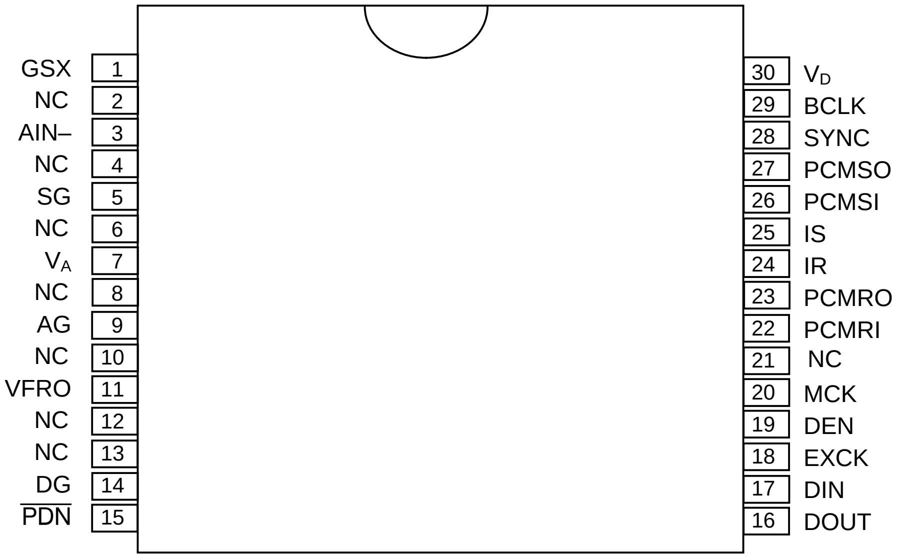
FEATURES

- Single 3 V Power Supply Operation (V_{DD}: 2.7 to 3.6 V)
- ADPCM Algorithm: ITU-T G.726 (32 kbps, 24 kbps, 16 kbps)
- Full-Duplex Transmit/Receive Operation
- Transmit/Receive Synchronous Mode Only
- PCM Data Format: μ-law
- Serial PCM/ADPCM Transmission Data Rate: 64 kbps to 2048 kbps (when SYNC = 8 kHz)
- Low Power Consumption
  - Operating Mode: 18 mW Typ. (V_{DD} = 3.0 V, SYNC = 8 kHz)
  - Power-Down Mode: 0.03 mW Typ. (V_{DD} = 3.0 V, SYNC = 8 kHz)
- Sampling Frequency: 6 kHz to 21 kHz selectable (However, there are limitations to 16 kHz or higher frequencies)
- Master Clock Frequency: Sampling frequency × 1296
  When SYNC = 8 kHz: 10.368 MHz
- Transmit/Receive Mute, Transmit/Receive Programmable Gain Control
- Side Tone Path with Programmable Attenuation (8-Step Level Adjustment)
- Serial MCU Interface Control
- Package:
  30-pin plastic SSOP (SSOP30-P-56-0.65-K) (ML7029)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No Connection

30-Pin Plastic SSOP

PIN FUNCTIONAL DESCRIPTIONS

AIN–, GEX

Transmit analog input and transmit level adjustment.
AIN– is connected to the inverting input of the transmit amplifier. GSX is connected to the transmit amplifier output. During power-down mode, the GSX output is a high impedance state.

VFRO

Receive analog output. During power-down mode, the VFRO output is in a high impedance state.

SG

Analog signal ground.
The output voltage of this pin is approximately 1.4 V. Put 10 μF plus 0.1 μF (ceramic type) bypass capacitors between this pin and AG. During power-down, this output voltage is 0 V. This pin should be used via a buffer if used externally.

AG

Analog ground.

DG

Digital ground.
This ground is separated from the analog signal ground pin (AG). The DG pin must be kept as close as possible to AG on the PCB.

Va

Analog +3 V power supply.

V_D

Digital +3 V power supply.
This power supply is separated from the analog signal power supply pin (V_A). The V_D pin must be kept as close as possible to V_A on the PCB.

$\overline{\text{PDN}}$

Power-down and reset control input.
A “0” level makes the IC enter a power-down state. At the same time, all control register data are reset to the initial state. Set this pin to “1” during normal operating mode. The power-down state is controlled by a logical OR with CR0-B5 of the control register. When using $\overline{\text{PDN}}$ for power-down and reset control, set CR0-B5 to digital “0”. The reset width (a “L” level period) should be 200 ns or more.
Be sure to reset the control registers by executing this power down to keep this pin to digital “0”level for 200 ns or longer after the power is turned on and V_{DD} exceeds 2.7 V.

MCK
Master clock input.
The frequency is 1296 times the SYNC signal. For example, it is 10.368 MHz when the SYNC signal is 8 kHz.
The master clock signal may be asynchronous with BCLK and SYNC.

PCMSO
Transmit PCM data output.
PCM is output from MSB in synchronization with the rising edge of BCLK and XSYNC.
Refer to Figure 1. During power-down, the PCMSO output is at “L” level.

PCMSI
Transmit PCM data input.
This signal is converted to the transmit ADPCM data, PCM is shifted in synchronization with the falling edge of BCLK. Normally, this pin is connected to PCMSO. Refer to Figure 1.

PCMRO
Receive PCM data output.
PCM is the output signal after ADPCM decoder processing. This signal is output serially from MSB in synchronization with the rising edge of BCLK and RSYNC. Refer to Figure 1.
During power-down, the PCMRO output is at “L” level.

PCMRI
Receive PCM data input.
PCM is shifted on the rising edge of the BCLK and input from MSB. Normally, this pin is connected to PCMRO.
Refer to Figure 1.

IS
Transmit ADPCM signal output.
After having encoded PCM with ADPCM, the signal is output from MSB in synchronization with the rising edge of BCLK and XSYNC. Refer to Figure 1. This pin is at “H” level during power-down.

IR
Receive ADPCM signal input.
This input signal is shifted serially on the falling edge of BCLK and SYNC and input from MSB. Refer to Figure 1.

BCLK
Shift clock input for the PCM and ADPCM data.
The frequency is set in the range of 8 to 256 times the SYNC frequency. Refer to Figure 1.

SYMC
Sampling input for the PCM and ADPCM data. The frequency is 8 kHz or 11.025 kHz and is selected by the control register data CR3-B1.
Synchronize this signal with BCLK signal. SYNC is used to indicate the MSB of the PCM data stream. Refer to Figure 1.

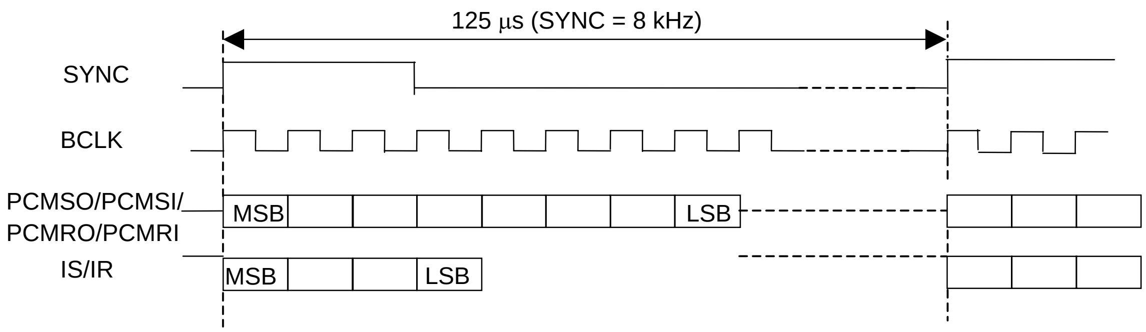


Figure 1 PCM and ADPCM Interface Basic Timing

DEN, EXCK, DIN, DOUT

Serial control ports for MCU interface.

Reading and writing data are performed by an external MCU through these pins. The 8-byte cotrol registers (CR0 to 7) are provided on the device.

DEN is the “Enable” control signal input, EXCK is the data shift clock input, DIN is the address and data input, and DOUT is the data output.

Figures 2-1 and 2-2 show the input/output timing diagram. During power-down, the DOUT output is in a high impedance state.

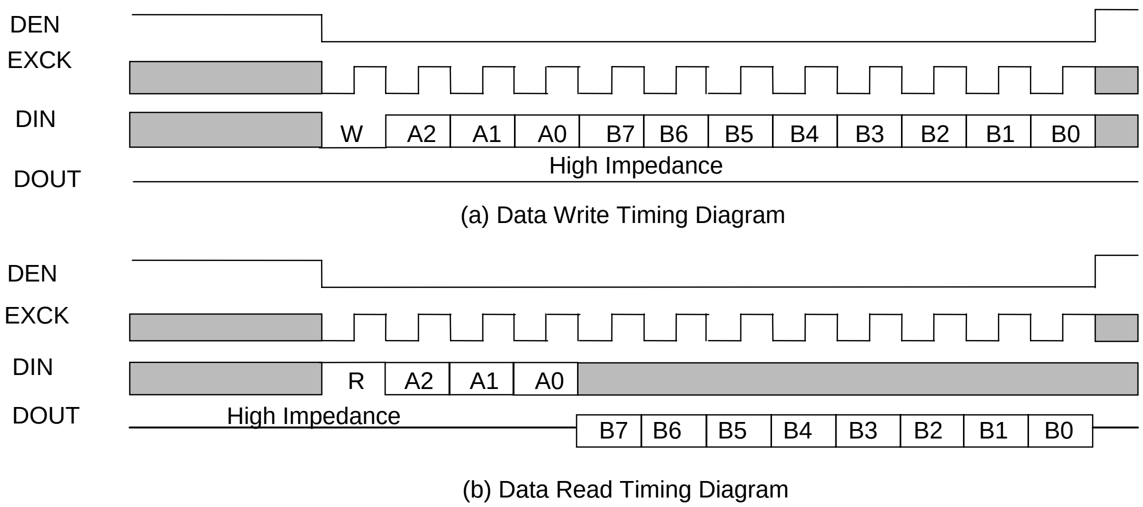


Figure 2-1 MCU Interface Input/Output Timing (DIN = 12 bits)

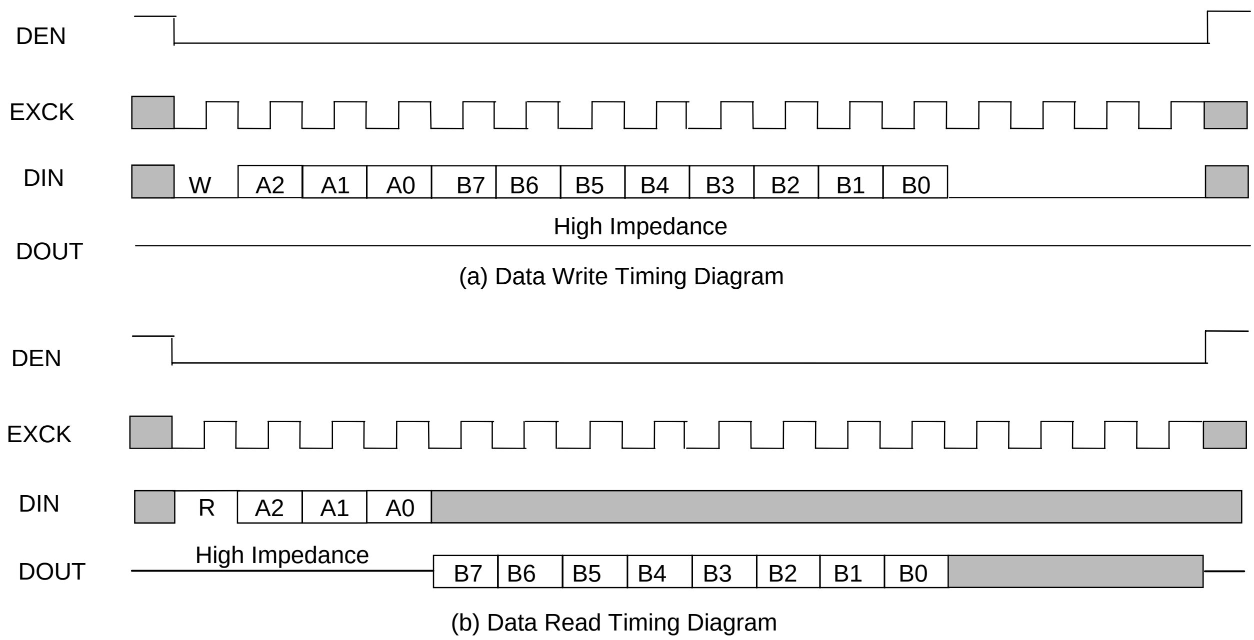


Figure 2-2 MCU Interface Input/Output Timing (DIN = 16 bits)

Table 1 shows the register map.

Table 1 Control Register Map

Name	Address			Control and Detect Data								R/W
	A2	A1	A0	B7	B6	B5	B4	B3	B2	B1	B0	
CR0	0	0	0	—	—	PDN ALL	—	—	—	—	—	R/W
CR1	0	0	1	MODE 1	MODE 0	TX RESET	RX RESET	TX MUTE	RX MUTE	—	RX PAD	R/W
CR2	0	1	0	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0	R/W
CR3	0	1	1	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	—	—	—	HPF 8k/11k	HPF ON/OFF	R/W

R/W : Read/Write enable

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–.3 to +5.0	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD}+0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{stg}	—	–55 to +150	°C

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed	+2.7	3.0	+3.6	V
Operating Temperature Range	Ta	—	–25	+25	+70	°C
Digital Input High Voltage	V_{IH}	Digital Input Pins	0.45 × V_{DD}	—	V_{DD}	V
Digital Input Low Voltage	V_{IL}	Digital Input Pins	0	—	0.16 × V_{DD}	V
Master Clock Frequency	f_{MCK1}	MCK	7.776	10.368	20.736	MHz
Master Clock Frequency Accuracy	f_{MCK2}	MCK	–0.01%	SYNC × 1296	+0.01%	MHz
Bit Clock Duty	f_{BCK}	BCLK	SYNC × 8	—	SYNC × 256	kHz
Sampling Frequency (*1)	f_{SYNC}	SYNC	6.0	8.0	16	kHz
Master Clock Duty Ratio	D_{MCK}	MCK (≤20.736 MHz)	30	50	70	%
Clock Duty Ratio	D_{CLK}	BCLK, EXCK	30	50	70	%
Digital Input Rise Time	t_{ir}	Digital Input Pins	—	—	50	ns
Digital Input Fall Time	t_{if}	Digital Input Pins	—	—	50	ns
PCM Sync Signal Setting Time (Continuous BCLK)	t_{BS}	BCLK ↔ SYNC (see Fig. 3-1)	100	—	—	ns
PCM Sync Signal Setting Time (Burst Mode Clock)	t_{SB}	BCLK ↔ SYNC (see Fig. 3-2)	0	—	20	μs
SYNC Signal Width (Continuous BCLK)	t_{WS}	SYNC (see Fig. 3-1)	1BCLK	—	SYNC –1 BCLK	μs
SYNC Signal Width (Burst Mode Clock)	t_{WSB}	SYNC (see Fig. 3-2)	1BCLK	—	Burst Clock –1	μs
PCM, ADPCM Setup Time	t_{DS}	—	100	—	—	ns
PCM, ADPCM Hold Time	t_{DH}	—	100	—	—	ns
Digital Output Load	C_{DL}	Digital Output Pins	—	—	100	pF
Bypass Capacitors for SG	C_{SG}	SG to AG	10+0.1	—	—	μF

*1: Refer to the Appendix.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 to 3.6 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating Mode No Signal	—	6.0	12	mA
(V_{DD} = 3.0 V, SYNC = 8 kHz)	I_{DD2}	Power Down Mode (Input pins are fixed)	—	0.01	0.1	mA
Input Leakage Current	I_{IH}	$V_I = V_{DD}$	—	—	2.0	µA
	I_{IL}	V_I = 0 V	—	—	0.5	µA
Output High Voltage	V_{OH}	I_{OH} = 4 mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = –4 mA	—	—	0.4	V
Input Capacitance	C_{IN}	—	—	5	—	pF

Analog Interface Characteristics

(V_{DD}= 2.7 to 3.6 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{IN}	AIN–	—	10	—	MΩ
Output Load Resistance	R_L	GSX, VFRO	20	—	—	kΩ
Output Load Capacitance	C_L	GSX, VFRO	—	—	100	pF
Output Amplitude (*2)	V_{O1}	GSX, VFRO (R_L = 20 kΩ)	—	—	1.3	V_{PP}
Offset Voltage	V_{OF}	GSX, VFRO	–100	—	+100	mV
SG Output Voltage	V_{SG}	SG	—	1.4	—	V
SG Output Resistance	R_{SG}	SG	—	40	—	kΩ
SG Warm-up Time	T_{SG}	SG↔AG 10+0.1µF (Rise time to max. 90% level)	—	700	—	ms

*2: –7.7 dBm (600Ω) = 0 dBm0, +3.17 dBm0 = 1.3 V_{PP}

AC Characteristics

(V_{DD} = 2.7 to 3.6 V, Ta = –25 to +70°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
		Freg. (Hz)	Level (dBm0)				
Transmit Frequency Response SYNC = 8 kHz BPF	LB8T1	60	0	30	—	—	dB
	LB8T2	300		–0.5	—	1.5	dB
	LB8T3	1015		Reference			dB
	LB8T4	3400		–0.5	—	1.0	dB
	LB8T5	3970		12	—	—	dB
Transmit Frequency Response SYNC = 11.025 kHz BPF	LB11T1	60	0	30	—	—	dB
	LB11T2	300		–0.5	—	1.5	dB
	LB11T3	1400		Reference			dB
	LB11T4	4690		–0.5	—	1.0	dB
	LB11T5	5470		12	—	—	dB
Transmit Frequency Response SYNC = 8 kHz LPF	LL8T1	300	0	–0.5	—	0.5	dB
	LL8T2	1015		Reference			dB
	LL8T3	3400		–0.5	—	1.0	dB
	LL8T4	3970		12	—	—	dB
Transmit Frequency Response SYNC = 11.025 kHz LPF	LL11T1	300	0	–0.5	—	0.5	dB
	LL11T2	1400		Reference			dB
	LL11T3	4690		–0.5	—	1.0	dB
	LL11T4	5470		12	—	—	dB
Receive Frequency Response SYNC = 8 kHz LPF	LL8R1	300	0	–0.5	—	0.5	dB
	LL8R2	1015		Reference			dB
	LL8R3	3400		–0.5	—	1.0	dB
	LL8R4	3970		12	—	—	dB
Receive Frequency Response SYNC = 11.025 kHz LPF	LL11R1	300	0	–0.5	—	0.5	dB
	LL11R2	1400		Reference			dB
	LL11R3	4690		–0.5	—	1.0	dB
	LL11R4	5470		12	—	—	dB
Transmit S/N Ratio SYNC = 8 kHz (*3)	SD8T1	f = 1015 Hz	3	35	—	—	dB
	SD8T2		–40	28	—	—	dB
Receive S/N Ratio SYNC = 8 kHz (*3)	SD8R1	f = 1015 Hz	3	35	—	—	dB
	SD8R2		–40	28	—	—	dB
Transmit S/N Ratio SYNC = 16 kHz (*3)	SD16T1	f = 1015 Hz	3	35	—	—	dB
	SD16T2		–40	28	—	—	dB
Receive S/N Ratio SYNC = 16 kHz (*3)	SD16R1	f = 1015 Hz	3	35	—	—	dB
	SD16R2		–40	28	—	—	dB
Idle Channel Noise SYNC = 8 kHz (*3)	N_{IDLT}	—	AIN– = SG	—	—	–68	dBm0pP
	N_{IDLR}		(*4)	—	—	–72	dBm0pP
Idle Channel Noise SYNC = 16 kHz (*3)	N_{IDLT}	—	AIN– = SG	—	—	–68	dBm0pP
	N_{IDLR}		(*4)	—	—	–72	dBm0pP
Absolute Signal Amplitude (*5)	A_{VT}	1015 Hz(GSX) SYNC = 8 kHz	0	0.285	0.320	0.359	Vrms
	A_{VR}	1015 Hz(VFRO) SYNC = 8 kHz	0	0.285	0.320	0.359	Vrms

*3: Use the P-message weighted filter
*4: PCMRI input code “11111111” (µ-law)
*5: 0.320 Vrms = 0 dBm0 = –7.7 dBm (600Ω)

Digital Interface

(V_{DD} = 2.7 to 3.6 V, Ta = –20 to +70°C)

Parameter	Symbol	Condition	Reference	Min.	Typ.	Max.	Unit
Digital Input/Output Setting Time	t_{SDX}, t_{SDR}	1LSTTL+100 pF	Fig. 3-1 Fig. 3-2	0	—	200	ns
	t_{XD1}, t_{RD1}			0	—	200	ns
	t_{XD2}, t_{RD2}			0	—	200	ns
	t_{XD3}, t_{RD3}			0	—	200	ns
Serial Port Digital Input/Output Setting Time	t_1	C_L= 50 pF	Fig. 4-1 Fig. 4-2	50	—	—	ns
	t_2			50	—	—	ns
	t_3			50	—	—	ns
	t_4			50	—	—	ns
	t_5			100	—	—	ns
	t_6			50	—	—	ns
	t_7			50	—	—	ns
	t_8			0	—	50	ns
	t_9			50	—	—	ns
	t_{10}			50	—	—	ns
	t_{11}			0	—	50	ns
Shift Clock Frequency	f_{EXCK}	EXCK	EXCK	—	—	10	MHz

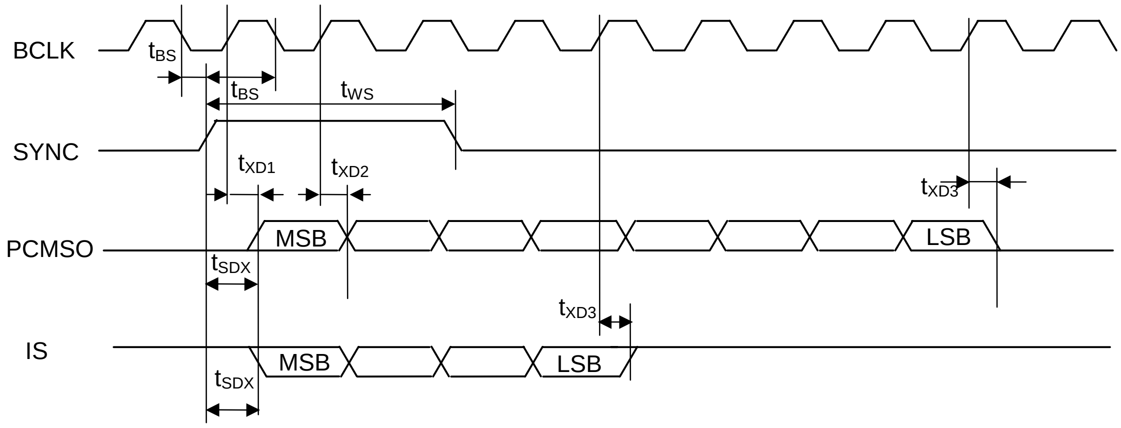
AC Characteristics (Programmable Gain Stages)

(V_{DD} = 2.7 to 3.6 V, Ta = -25 to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Gain Accuracy	D_G	All stages, to programmed value SYNC = 8 kHz	–1	0	+1	dB

TIMING DIAGRAM

Transmit Side PCM/ADPCM Data Interface



Receive Side PCM/ADPCM Data Interface

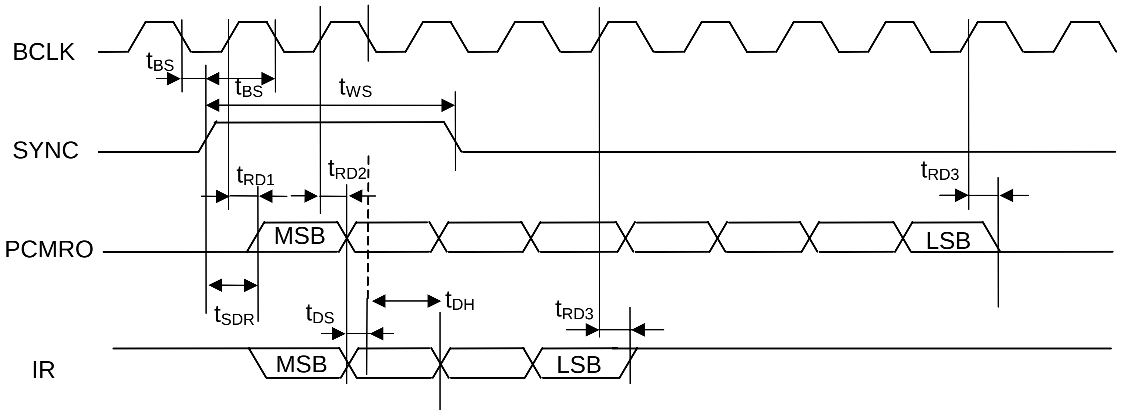
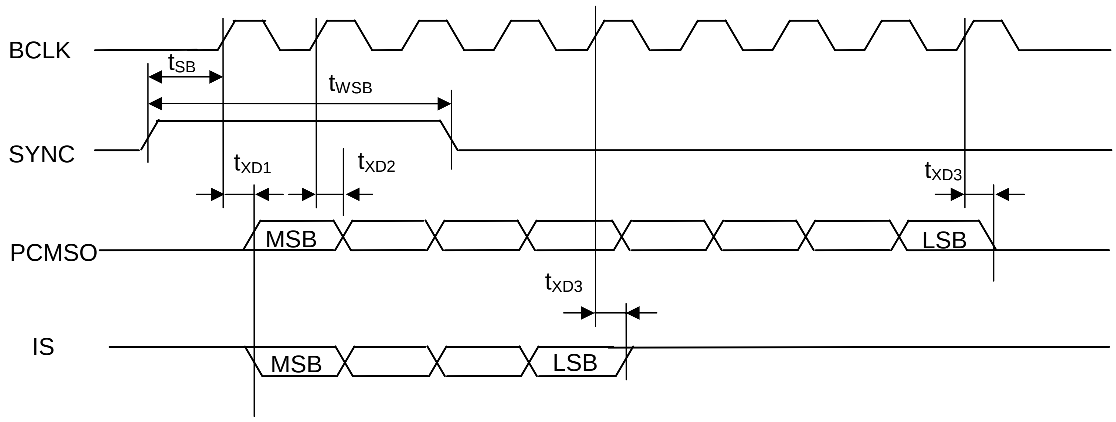


Figure 3-1 PCM/ADPCM Data Interface (Continuous BCLK)

Transmit Side PCM/ADPCM Data Interface



Receive Side PCM/ADPCM Data Interface

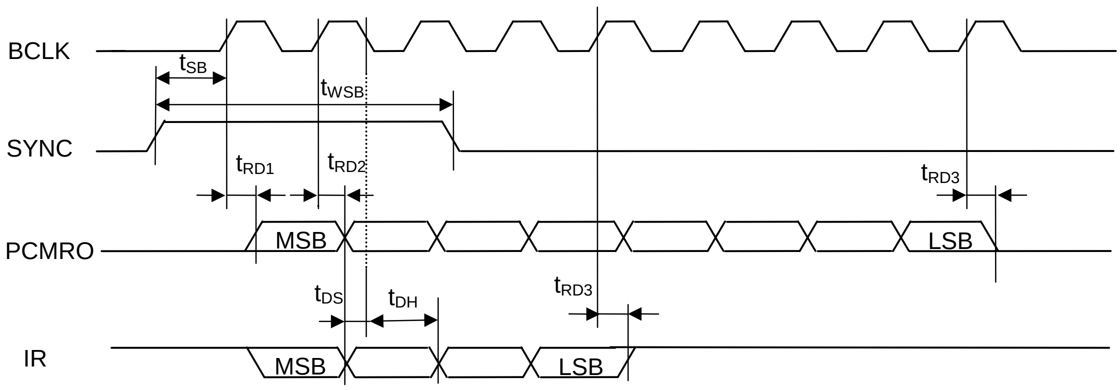


Figure 3-2 PCM/ADPCM Data Interface (Burst Mode Clock)

Serial Port Data Transfer for MCU Interface

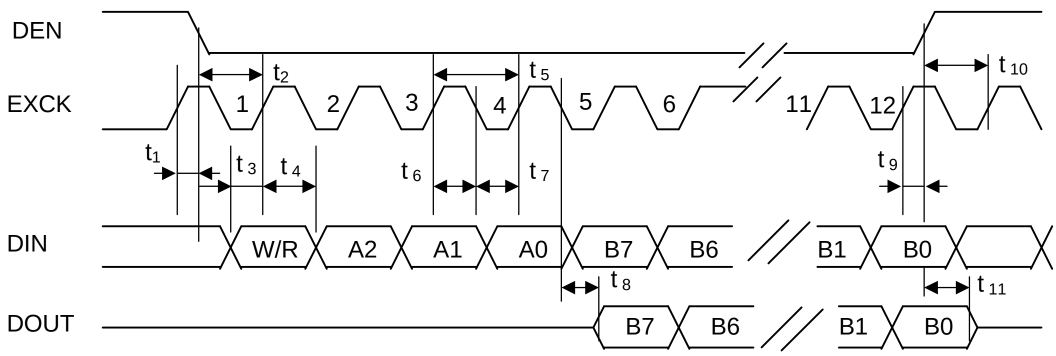


Figure 4-1 Serial Control Port Interface (DIN = 12 bits)

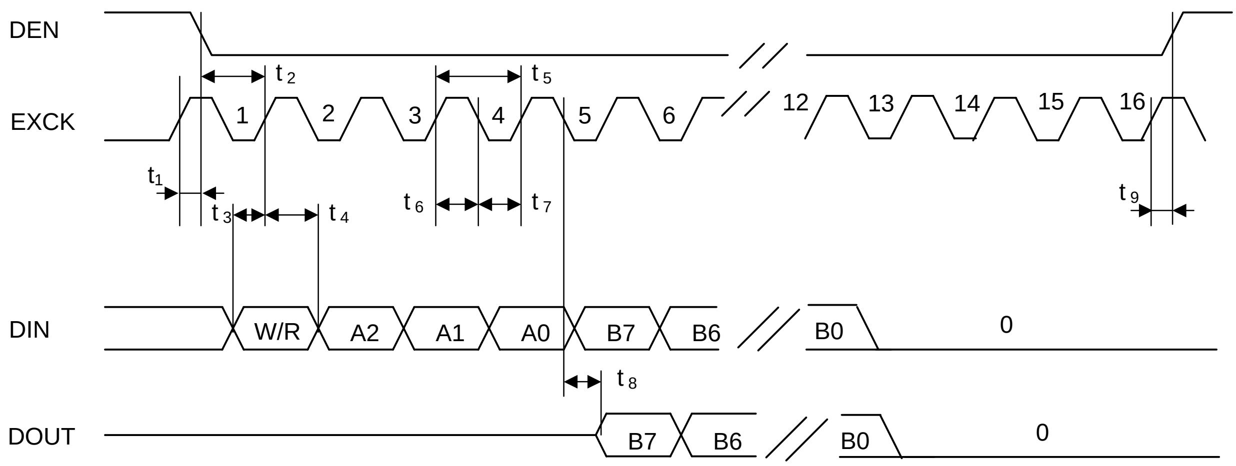


Figure 4-2 Serial Control Port Interface (DIN = 16 bits)

FUNCTIONAL DESCRIPTION

Control Registers

(1) CR0 (Basic operating mode setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR0	—	—	PDN ALL	—	—	—	—	—
Initial Value	*	*	0	*	*	*	*	*

Note: Initial Value: Reset state by $\overline{\text{PDN}}$ (*: Don’t care)

B7, B6, B4 to B0: Not used (These pins are used to test the device. They should be set to “0” during normal operation.)

B5: Power-down (entire system); 0/Power-on, 1/Power-down
0 Red with the inverted external power-down signals.
When using this data, set the $\overline{\text{RDN}}$ pin to “1”.

(2) CR1 (ADPCM operating mode setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR1	MODE1	MODE0	TX RESET	RX RESET	TX MUTE	RX MUTE	—	RX PAD
Initial Value	0	0	0	0	0	0	*	0

B7, B6: ADPCM data compression algorithm select (output bit select);
(0, 0): 4-bit output (32 kbps)
(0, 1): 8-bit output (64 kbps)
(1, 0): 3-bit output (24 kbps)
(1, 1): 2-bit output (16 kbps)
Data rates in parentheses: when SYNC = 8 kHz

B5: ADPCM of transmit reset (specified by G.726); 1/Reset*
B4: ADPCM of receive reset (specified by G.726); 1/ Reset*
B3: ADPCM transmit data mute; 1/Mute
B2: ADPCM receive data mute; 1/Mute
B1: Not used (This pin is used to test the device. It should be set to “0” during normal operation.
B0: Receive side PAD; 1/inserted in the receive side voice path, 12 dB loss
0/no PAD

* The reset width should be $1/f_{sample}$ μs or more.
The transmit and receive sides cannnot be reset separately.
They must be reset at the same time.

(3) CR2 (PCM CODEC operating mode setting and transmit/receive gain adjustment)

	B7	B6	B5	B4	B3	B2	B1	B0
CR2	TX ON/OFF	TX GAIN2	TX GAIN1	TX GAIN0	RX ON/OFF	RX GAIN2	RX GAIN1	RX GAIN0
Initial Value	0	0	1	1	0	0	1	1

B7: Transmit PCM signal ON/OFF; 0/ON, 1/OFF

B6, B5, B4: Transmit signal gain adjustment, refer to Table 2.

B3: Receive PCM signal ON/OFF; 0/ON, 1/OFF

B2, B1, B0: Receive signal gain adjustment, refer to Table 2.

Table 2 Transmit/Receive Gain Setting (when SYNC = 8 kHz)

B6	B5	B4	Transmit Gain	B2	B1	B0	Receive Gain
0	0	0	–6 dB	0	0	0	–6 dB
0	0	1	–4 dB	0	0	1	–4 dB
0	1	0	–2 dB	0	1	0	–2 dB
0	1	1	0 dB	0	1	1	0 dB
1	0	0	+2 dB	1	0	0	+2 dB
1	0	1	+4 dB	1	0	1	+4 dB
1	1	0	+6 dB	1	1	0	+6 dB
1	1	1	+8 dB	1	1	1	+8 dB

(4) CR3 (Side tone gain setting)

	B7	B6	B5	B4	B3	B2	B1	B0
CR3	Side Tone GAIN2	Side Tone GAIN1	Side Tone GAIN0	—	—	—	HPF 8k/11k	HPF ON/OFF
Initial Value	0	0	0	*	*	*	0	0

B7, B6, B5: Side tone path gain setting. Refer to Table 3.

B4 to B2: Not used (These pins are used to test the device. They should be set to "0" during normal operation.)

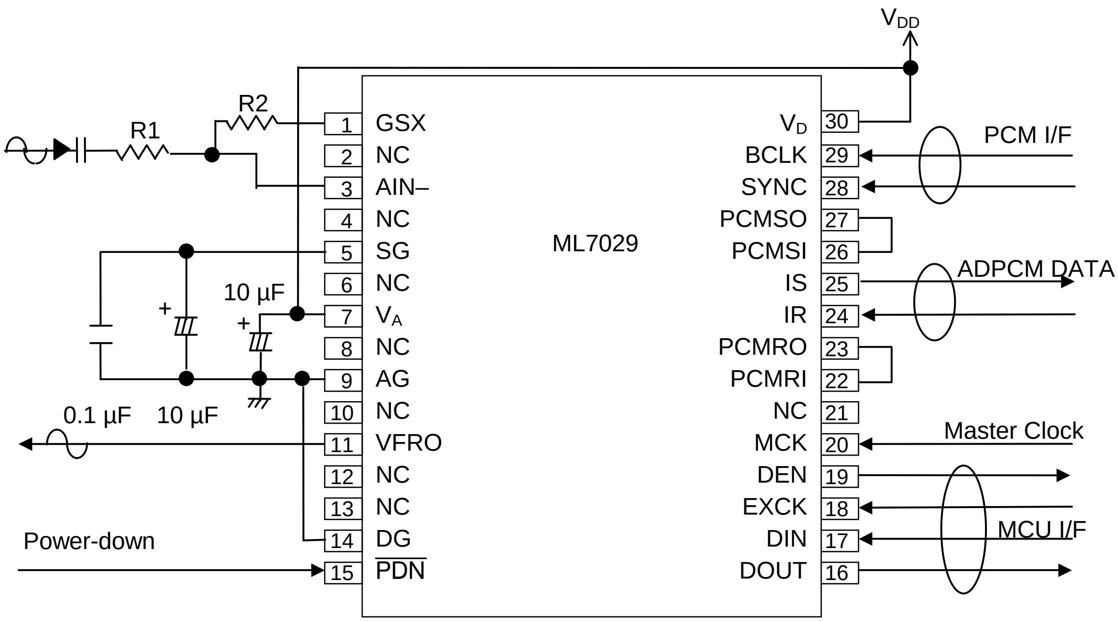
Table 3 Side Tone Pash Gain Setting (when SYNC = 8 kHz)

B7	B6	B5	Side Tone Path Gain
0	0	0	OFF
0	0	1	–21 dB
0	1	0	–19 dB
0	1	1	–17 dB
1	0	0	–15 dB
1	0	1	–13 dB
1	1	0	–11 dB
1	1	1	–9 dB

B1: Transmit HPF cut-off frequency select;
0/The cut-off frequency of the transmit HPF is the sampling frequency × 0.0275.
When SYNC = 8 kHz: 220 Hz, when SYNC = 11.025 kHz: 300 Hz.
The transmit frequency characteristics are not guaranteed when selecting SYNC = 11.025 kHz.
1/The cut-off frequency of the transmit HPF is the sampling frequency × 0.0200.
When SYNC = 8 kHz: 160 Hz, when SYNC = 11.025 kHz: 220 Hz.
The transmit frequency characteristics are not guaranteed when selecting SYNC = 8 kHz.
B0: Transmit HPF ON/OFF; 0/ON, 1/OFF

For the frequency characteristics, refer to Figures 9 to 12 in the Reference Data.

APPLICATION CIRCUIT



APPLICATION INFORMATION

Burst Mode Clock

This device can be operated by a burst mode clock (see below).

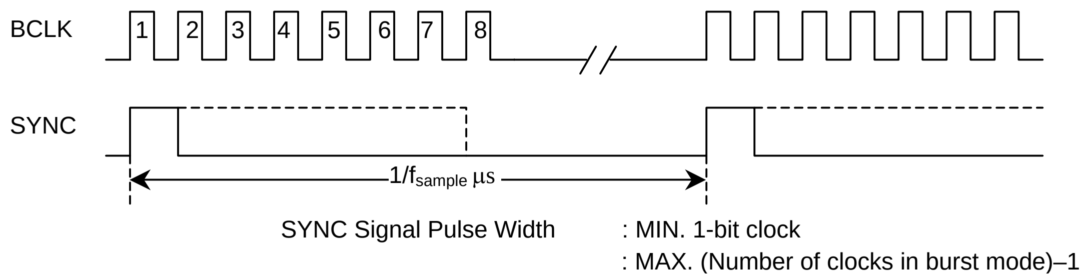


Figure 5 Example of Burst Mode Clock

Relationship between SYNC and BLCK

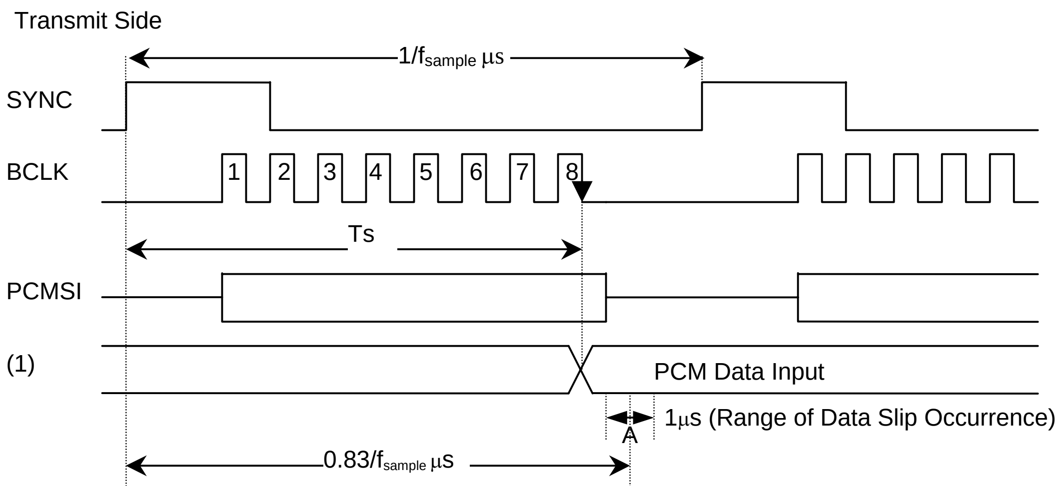


Figure 6

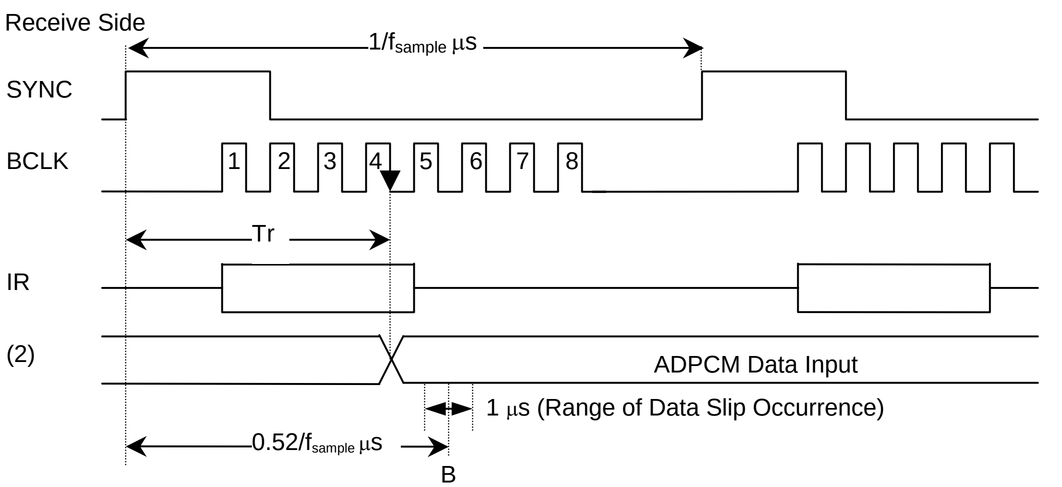
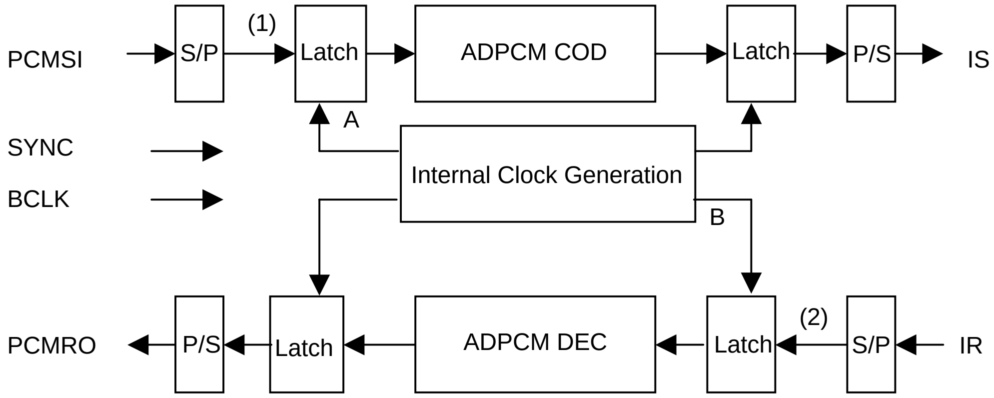


Figure 7



(1): PCM data serial to parallel conversion output
(2): ADPCM data serial to parallel conversion output
A: (1) Data internal latch timing
B: (2) Data internal latch timing

Figure 8

In this device, internal operating timing is generated according to the SYNC signal (see Figure 8). Therefore, a data slip may occur in the following timing when the PCM and ADPCM data is input.

1. When the PCM signal (PCMSI) is captured
   If TS: PCM signal output (1) after serial/parallel conversion and A: internal latch timing in Figure 6 overlap, a data slip occurs.

2. When the ADPCM signal (IR) is captured
   If Tr: ADPCM signal output (2) after serial/parallel conversion and B: internal latch timing in Figure 7 overlap, a data slip occurs.

The data slip occurs at the timing of 1 and 2 above. Therefore, taking internal clock jitters and IC internal delay into consideration, the timing of SYNC and BCLK signals should not be set up in the range of about 1 μs from the timing A and B.

REFERENCE DATA

Transmit Frequency Characteristics

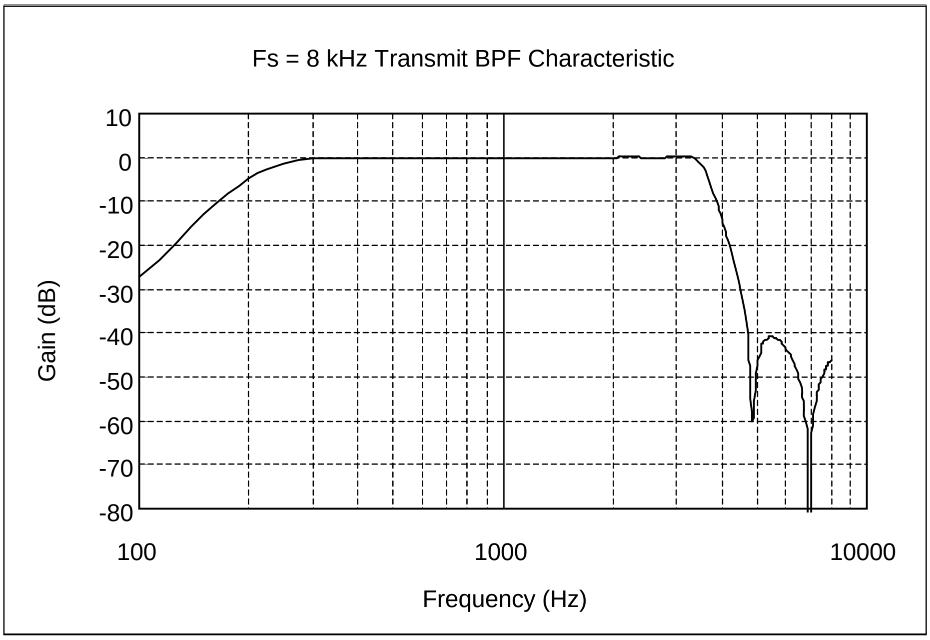


Figure 9 Transmit Bandpass Filter Characteristic (Fs = 8 kHz, CR3-B1, B0 = (0, 0))

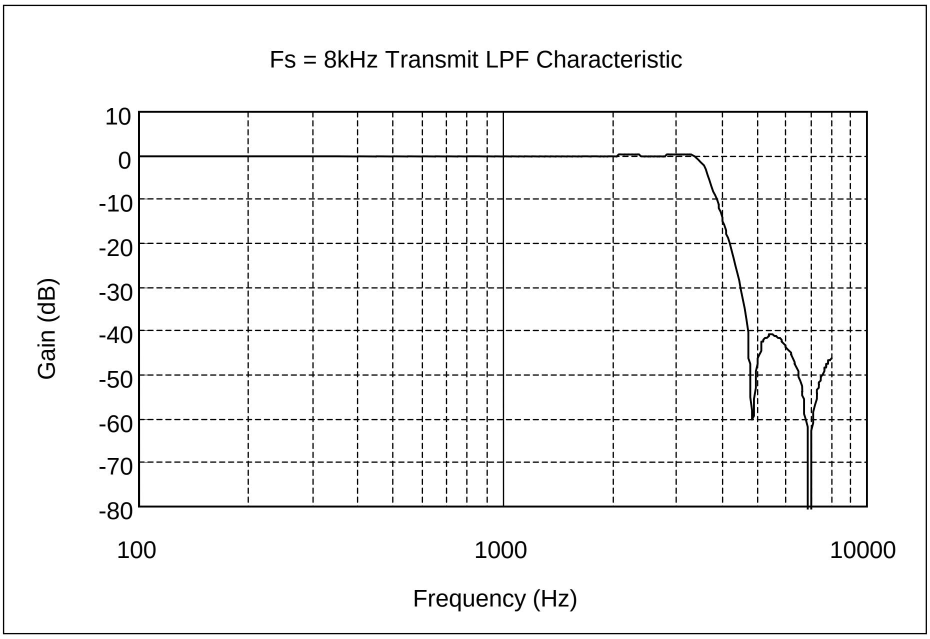


Figure 10 Transmit Lowpass Filter Characteristic (Fs = 8 kHz, CR3-B1, B0 = (0, 1))

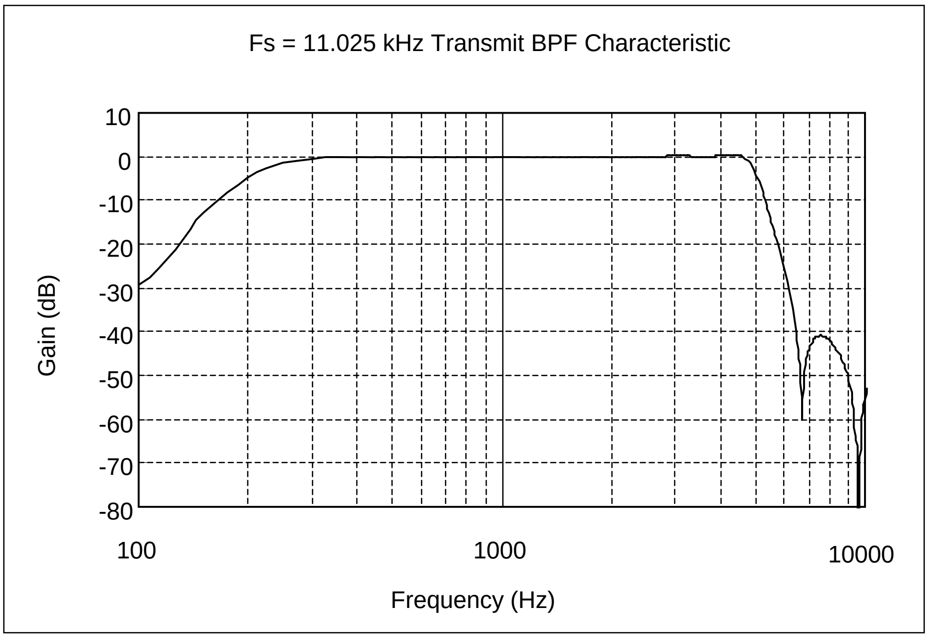


Figure 11 Transmit Bandpass Filter Characteristic (Fs = 11.025 kHz, CR3-B1, B0 = (1, 0))

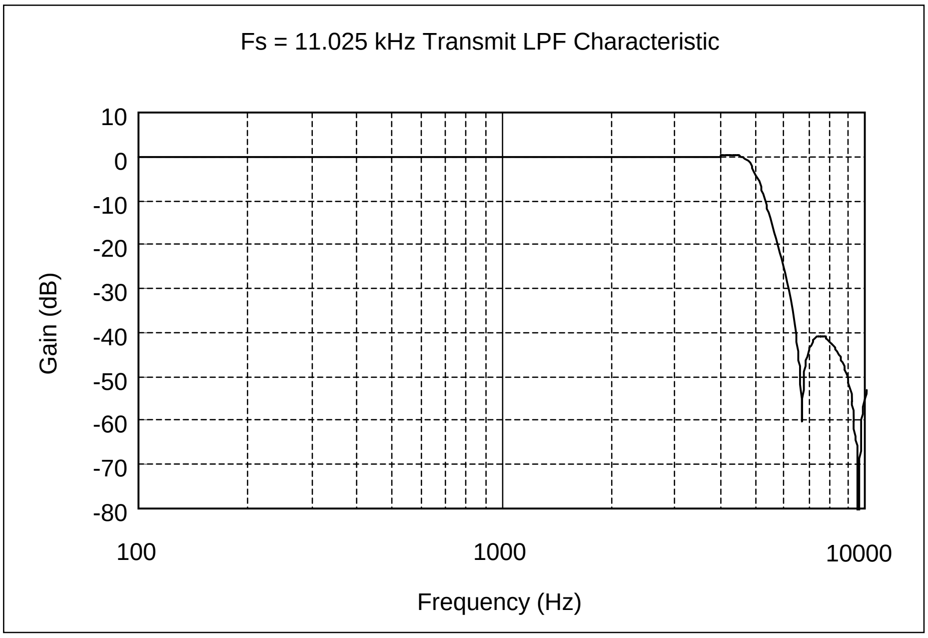


Figure 12 Transmit Lowpass Filter Characteristic (Fs = 11.025 kHz, CR3-B1, B0 = (1, 1))

Receive Frequency Characteristics

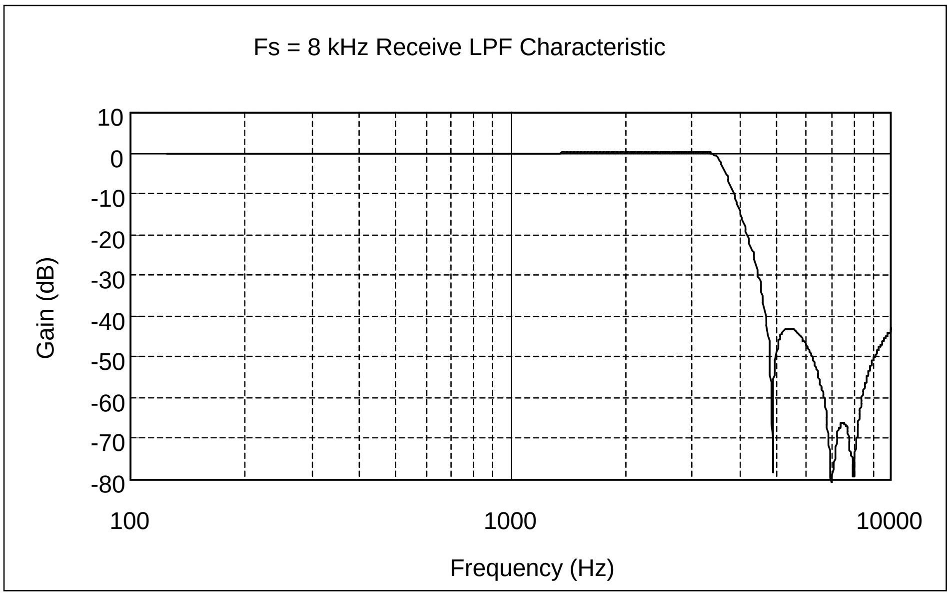


Figure 13 Receive Lowpass Filter Characteristic (Fs = 8 kHz, CR3-B1, B0 = (0, *))

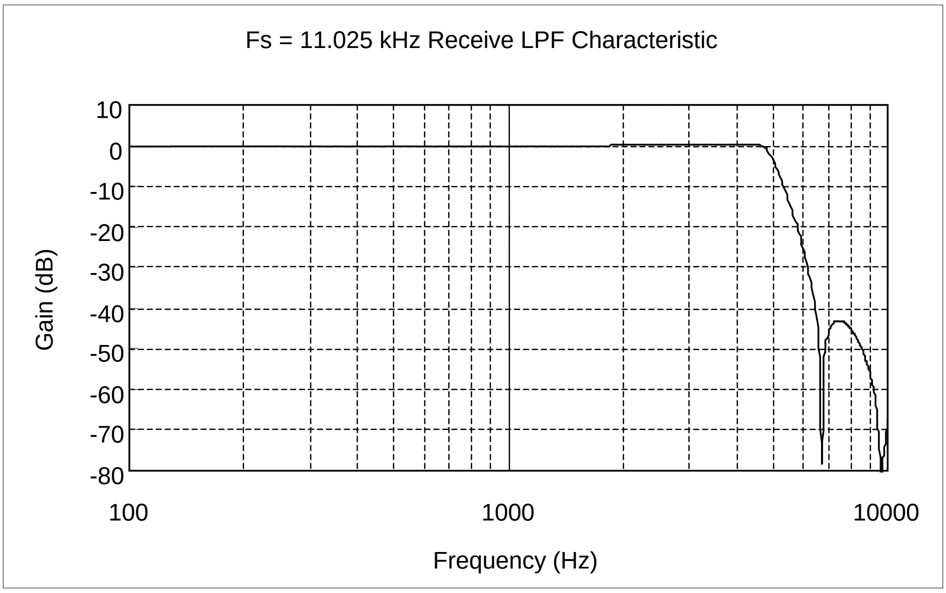


Figure 14 Receive Lowpass Filter Characteristic (Fs = 11.025 kHz, CR3-B1, B0 = (1, *))

APPENDIX

When the Sampling Frequency is 16 kHz or Higher:

This device enables the operation at 16 kHz or higher sampling frequencies under conditions below. However, be aware that the AC characteristics are not guaranteed under these conditions.

Operating Conditions at Sampling Frequency = 19 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed	3.0	—	3.6	V
Operating Temperature Range	Ta	—	–25	—	+50	°C
Digital Input High Voltage	V_{IH}	Digital input pin	0.95 × V_{DD}	—	V_{DD}	V
Digital Input Low Voltage	V_{IL}	Digital input pin	0		0.05 × V_{DD}	V
Master Clock Frequency	f_{MCK1}	MCK	—	24.624	—	MHz
Master Clock Frequency Accuracy	f_{MCK2}	MCK	–0.01%	SYNC × 1296	+0.01	MHz
Sampling Frequency	f_{SYNC}	SYNC	—	19	—	kHz
Master Clock Duty Ratio	D_{MCK}	—	40	—	70	%
Transmit S/N Ratio (at 3 dBm0 input)	SD19T1	—	—	46.2	—	dB
Transmit S/N Ratio (at –40 dBm0 input)	SD19T2	—	—	24.8	—	dB
Receive S/N Ratio (at 3 dBm0 input)	SD19R1	—	—	45.4	—	dB
Receive S/N Ratio (at –40 dBm0 input)	SD19R2	—	—	38.0	—	dB

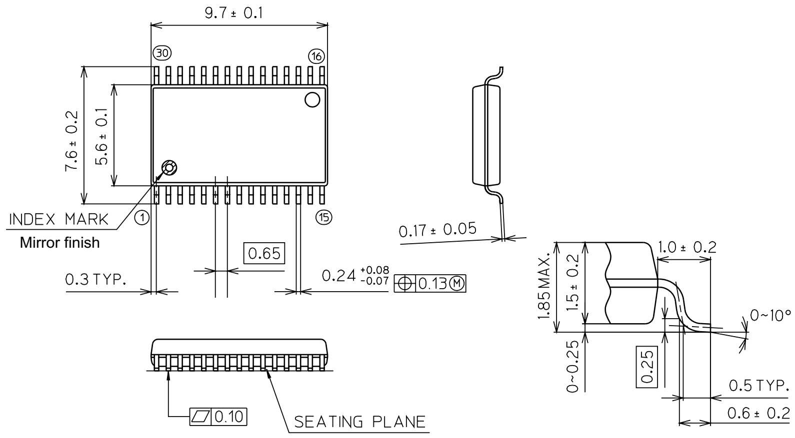
Operating Conditions at Sampling Frequency = 21 kHz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed	3.3	—	3.6	V
Operating Temperature Range	Ta	—	–25	—	+50	°C
Digital Input High Voltage	V_{IH}	Digital input pin	0.95 × V_{DD}	—	V_{DD}	V
Digital Input Low Voltage	V_{IL}	Digital input pin	0		0.05 × V_{DD}	V
Master Clock Frequency	f_{MCK1}	MCK	—	27.216	—	MHz
Master Clock Frequency Accuracy	f_{MCK2}	MCK	–0.01%	SYNC × 1296	+0.01	MHz
Sampling Frequency	f_{SYNC}	SYNC	—	21	—	kHz
Master Clock Duty Ratio	D_{MCK}	—	40	—	70	%
Transmit S/N Ratio (at 3 dBm0 input)	SD19T1	—	—	46.1	—	dB
Transmit S/N Ratio (at –40 dBm0 input)	SD19T2	—	—	20.2	—	dB
Receive S/N Ratio (at 3 dBm0 input)	SD19R1	—	—	44.8	—	dB
Receive S/N Ratio (at –40 dBm0 input)	SD19R2	—	—	37.8	—	dB

PACKAGE DIMENSIONS

(Unit: mm)

SSOP30-P-56-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.19 TYP.
Rev. No./Last Revised	5/Dec. 5, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7029-02	Nov. 2001	–	–	Final edition 2
FEDL7029-03	Feb.18, 2004	–	–	Final edition 3
		9	9	Changed “Symbol” of Setup Time and Hold Time for PCM/ ADPCM.

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