FEDL630Q791-01
Issue Date: 10/22/2014

ML630Q791

32-bit Microcontroller for Sensor Control

GENERAL DESCRIPTION

The ML630Q791 is a high-performance low power 32-bit microcontroller optimized for the control of various sensor ICs. Equipped with a 32-bit CPU core Cortex®-M0, it implements a 128 KB flash memory, 16 KB RAM, rich interfaces used to control various sensors, and host interface with the 512-byte communication register in a very compact package. The ML630Q791 can efficiently control the power consumption of the whole system by separating the sensor control function from the application processor, and its high performance permits sensor-fusion using accelerometers, magnetic field sensors and gyro sensors, which makes it an ideal sensor control microcontroller for smart phones.

FEATURES

● CPU
- — 32-bit RISC CPU (ARM® Cortex®-M0)
- — Thumb®/Thumb®-2 instruction supported
- — Serial Wire Debug (SWD) port support

● Internal memory
- — 128 KB FLASH ROM (32K x 32-bit)
- — 16 KB SRAM (4K x 32-bit)

● Interrupt controller
- — Non-maskable interrupt: 1 source
- — Maskable interrupt: 21 sources

Internal sources: 14 (Timer: 8, PWM: 1, I2C: 2, HOSTIF: 1, Arithmetic circuit: 1, UART: 1)
External sources: 7

● Timer / Counter
- — 8-bit auto-reload timer x 8channels
- — 16-bit pulse width modulation(PWM) x 1channel
- — Watchdog timer (WDT) x 1channel

● Serial interface
- — I2C interface with master function x 2channels (including 8-bit, 32-stage FIFO)
- — UART interface x 1channel (two-wire, full duplex communication, including 8-bit, 32-stage FIFO)

● Host interface
- — Serial interface with slave function (SPI/I2C selectable) x 1channel
- — Interrupt to a host processor
- — 512Byte FIFO RAM

● General-purpose I/O port
- — 7-bit input/output port x 1channel
- — External Interrupt function

● Arithmetic circuit
- — Root and Division operations support

● Flash Programming Function
- — Hardware remap function support
- — ISP(In System Programming) support

ROHM SEMICONDUCTOR

ARM CORTEX Processor Technology

● Operation mode and power management function
- — CPU operation mode
  Supports high- and low-speed clock operation.
- — Sleep mode
  Stops clock of CPU.
- — SleepDeep mode
  Stops clock of CPU and all peripheral blocks.

● Input clock
- — 32.768 kHz (External clock input)

● Power supply voltage
- — V_{DD} : 1.7V to 1.9V
- — Digital core section : 1.35V to 1.65V (supplied by the internal voltage regulator)

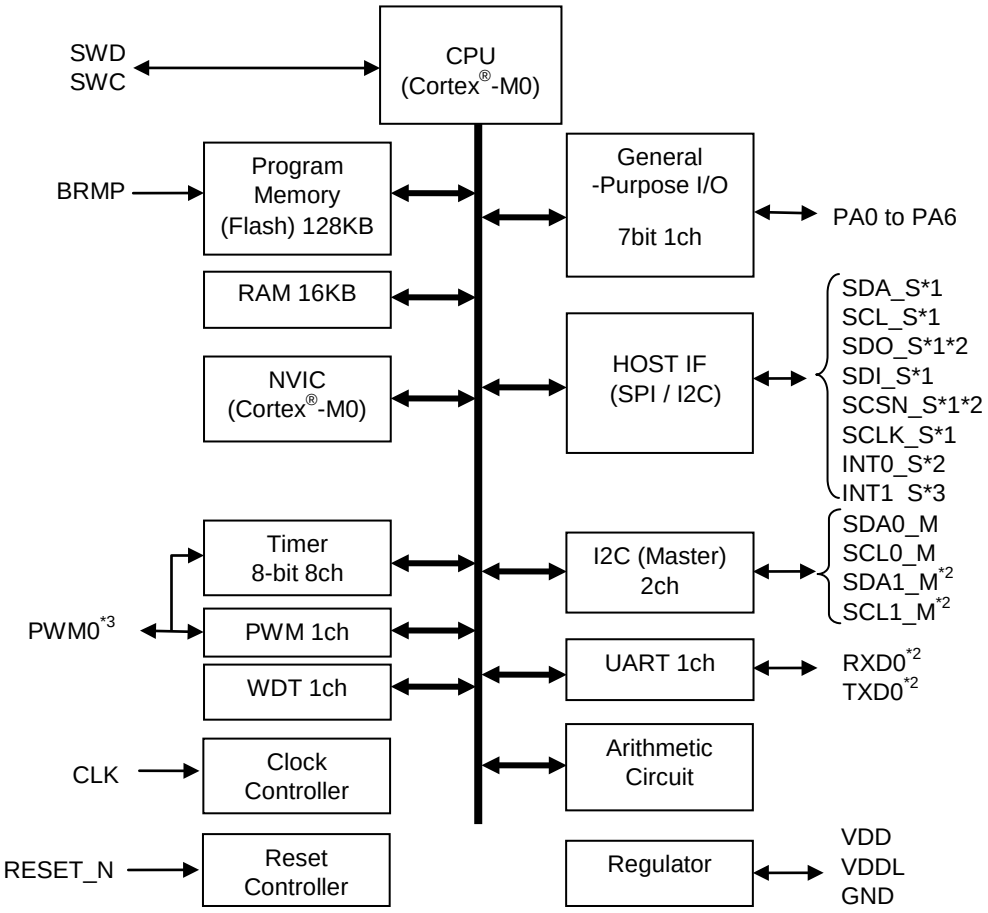
● Power consumption
- — High-speed operation (32MHz) : 5.0mA
- — SleepDeep mode : 2.5uA

● Operating frequency
- — High-speed clock: 32 MHz (generated by internal FLL from input clock)
- — Low-speed clock: 32.768 kHz

● Operating temperature
- — -40°C to 85°C

● Package
- — 20-pin WL-CSP 0.4mm pitch (2.1 mm x 1.8 mm)

BLOCK DIAGRAM



*1 Selectable I2C or SPI interface
*2 Secondary function
*3 Tertiary function

PIN CONFIGURATION

PA4	PA5	SDA0_M	SCL0_M	5
PA3	PA2	BRMP	VPP	4
GND	PA0	SWD	SWC	3
VDDL	PA1	SDA_S	CLK	2
VDD	RESET_N	PA6	SCL_S	1
D	C	B	A	

20-pin WL-CSP Package
(Bottom View)

PIN FUNCTION

Pin List

PIN No.	Primary Function				Secondary Function			Tertiary Function		
	Symbol	I/O	Reset State	Function	Symbol	I/O	Function	Symbol	I/O	Function
D3	GND	—	—	Power Supply	—	—	—	—	—	—
D1	VDD	—	—	Power Supply	—	—	—	—	—	—
D2	VDDL	—	—	Power Supply	—	—	—	—	—	—
A2	CLK	I	HZ	SYSTEM	—	—	—	—	—	—
B4	BRMP	I	PD	SYSTEM	—	—	—	—	—	—
A3	SWC	I	PU	DEBUG I/F	—	—	—	—	—	—
B3	SWD	IO	PU	DEBUG I/F	—	—	—	—	—	—
C1	RESET_N	I	PU	SYSTEM	—	—	—	—	—	—
A1	SCL_S*1 SCLK_S	I I	HZ	HSTIF	—	—	—	—	—	—
B2	SDA_S*1 SDIO_S SDI_S	IO IO I	HZ	HSTIF	—	—	—	—	—	—
D5	PA4	IO	HZ	GPIO	SCS_S	I	HSTIF	—	—	—
C5	PA5	IO	HZ	GPIO	SDO_S	O	HSTIF	—	—	—
B5	SDA0_M	IO	HZ	I2C0	—	—	—	—	—	—
A5	SCL0_M	O	HZ	I2C0	—	—	—	—	—	—
C4	PA2	IO	HZ	GPIO	RXD0	I	UART	—	—	—
D4	PA3	IO	HZ	GPIO	TXD0	O	UART	—	—	—
C3	PA0	IO	HZ	GPIO	SDA1_M	IO	I2C1	PWM0	IO	PWM
C2	PA1	IO	HZ	GPIO	SCL1_M	O	I2C1	INT1_S	O	HSTIF
B1	PA6	IO	HZ	GPIO	INT0_S	O	HSTIF	—	—	—
A4	VPP	—	—	TEST	—	—	—	—	—	—

*1 The used pin is determined by the HSTIF setting.

Pin Description

Power Supply

Pin name	I/O	Description	Polarity
GND	—	IO/core GND	—
VDD	—	IO power supply	—
VDDL	—	Core power supply (generated by internal regulator)	—

SYSTEM

Pin name	I/O	Description	Polarity
CLK	I	External clock input (32.768kHz)	—
BRMP	I	Remap control input (for firmware update) Based on the BRMP pin setting at the time of the reset release, Bank0 is remapped.	—
RESET_N	I	System reset input	Negative

DEBUG Interface

Pin name	I/O	Description	Polarity
SWC	I	Serial clock of Serial Wire Debug Port	—
SWD	IO	Serial I/O data of Serial Wire Debug Port	—

Host Interface(HSTIF)

Pin name	I/O	Description	Polarity
SCL_S*2	I	SCL of I2C slave interface	—
SDA_S*2	IO	SDA of I2C slave interface	—
SCLK_ S	I	SCLK of SPI slave interface	—
SDIO_S	IO	SDI and SDO of SPI slave interface in 3-wired mode	—
SDI_S	I	SDI of SPI slave interface in 4-wired mode	—
SCS_S	I	SCS of SPI slave interface	*1
SDO_S	O	SDO of SPI slave interface in 4-wired mode	—
INT0_S	O	Interrupt0 output for host interface	Negative
INT1_S	O	Interrupt1 output for host interface	Negative

*1 The polarity can be set by the software.
*2 3.6V tolerant in case of I^2C interface.

I2C master interface

Pin name	I/O	Description	Polarity
SDA0_M*	IO	SDA of I2C0 master interface	—
SCL0_M*	O	SCL of I2C0 master interface	—
SDA1_M*	IO	SDA of I2C1 master interface	—
SCL1_M*	O	SCL of I2C1 master interface	—

* 3.6V tolerant.

UART

Pin name	I/O	Description	Polarity
RXD0	I	UART receive data	—
TXD0	O	UART transmit data	—

PWM

Pin name	I/O	Description	Polarity
PWM0	IO	Output: PWM interface Input: PWM and timer clock input	—

GPIO

Pin name	I/O	Description	Polarity
PA0 to PA6	IO	GPIO (External interrupt function available)	—

TEST

Pin name	I/O	Description	Polarity
VPP	—	FLASH test pin	—

TERMINATION OF UNUSED PINS

Pin	Recommended pin handling
VPP	Open
BRMP	Open
SWC	Connect a pull-up resistor. (Recommended)
SWD	Connect a pull-up resistor. (Recommended)
SCL_S	Connect a pull-down resistor.
SDA_S	Connect a pull-down resistor.
PA0 to PA6	Open (Note)
SDA0_M, SCL0_M	Connect a pull-up resistor.

[Note:]
It is recommended to set the unused input ports and input/output ports to the input mode with pull-down/pull-up resistor or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

HOST INTERFACE

The ML630Q791 controls various sensors via the host interface. The host interface provides selectable I2C/SPI interface and interrupt signals to the host processor, and includes an register address space and an 512Byte FIFO.

Register Map

Address		Name	Symbol	R/W	Size	Initial Value
Write	Read					
0x00	0x80	Configuration register	CFG	R/W	8	0x00
0x01	0x81	reserved	—	—	—	—
0x02	0x82	interrupt mask register 0	INTMSK0	R/W	8	0xFF
0x03	0x83	interrupt mask register 1	INTMSK1	R/W	8	0xFF
0x04~ 0x08	0x84~ 0x88	reserved	—	—	—	—
—	0x89	Operation status register	STATUS	R/—	8	0xFE
—	0x8A	Error code register 0	ERROR0	R/—	8	0x00
—	0x8B	Error code register 1	ERROR1	R/—	8	0x00
—	0x8C	interrupt request register 0	INTREQ0	R/—	8	0x00
—	0x8D	interrupt request register 1	INTREQ1	R/—	8	0x00
0x0E~ 0x0F	0x8E~ 0x8F	reserved	—	—	—	—
0x10	0x90	FIFO register	FIFO	R/W	8	0xXX
0x11~ 0x1F	0x91~ 0x9F	reserved	—	—	—	—
0x20	0xA0	Parameter register 0F	PRMF	R/W	8	0x00
0x21	0xA1	Parameter register 0E	PRME	R/W	8	0x00
0x22	0xA2	Parameter register 0D	PRMD	R/W	8	0x00
0x23	0xA3	Parameter register 0C	PRMC	R/W	8	0x00
0x24	0xA4	Parameter register 0B	PRMB	R/W	8	0x00
0x25	0xA5	Parameter register 0A	PRMA	R/W	8	0x00
0x26	0xA6	Parameter register 09	PRM9	R/W	8	0x00
0x27	0xA7	Parameter register 08	PRM8	R/W	8	0x00
0x28	0xA8	Parameter register 07	PRM7	R/W	8	0x00
0x29	0xA9	Parameter register 06	PRM6	R/W	8	0x00
0x2A	0xAA	Parameter register 05	PRM5	R/W	8	0x00
0x2B	0xAB	Parameter register 04	PRM4	R/W	8	0x00
0x2C	0xAC	Parameter register 03	PRM3	R/W	8	0x00
0x2D	0xAD	Parameter register 02	PRM2	R/W	8	0x00
0x2E	0xAE	Parameter register 01	PRM1	R/W	8	0x00
0x2F	0xAF	Parameter register 00	PRM0	R/W	8	0x00
0x30	0xB0	Command register 0	CMD0	R/W	8	0x00
0x31	0xB1	Command register 1	CMD1	R/W	8	0x00
0x32	0xB2	Command entry register	ENT	R/W	8	0x00
0x33~ 0x3F	0xB3~ 0xBF	reserved	—	—	—	—
—	0xC0	Result register 00	RSLT00	R/—	32	0x00
—	0xC1	Result register 01	RSLT01	R/—	32	0x00
—	0xC2	Result register 02	RSLT02	R/—	32	0x00
—	0xC3	Result register 03	RSLT03	R/—	32	0x00
—	0xC4	Result register 04	RSLT04	R/—	32	0x00
—	0xC5	Result register 05	RSLT05	R/—	32	0x00
—	0xC6	Result register 06	RSLT06	R/—	32	0x00
—	0xC7	Result register 07	RSLT07	R/—	32	0x00
—	0xC8	Result register 08	RSLT08	R/—	32	0x00
—	0xC9	Result register 09	RSLT09	R/—	32	0x00

Address		Name	Symbol	R/W	Size	Initial Value
Write	Read					
—	0xCA	Result register 0A	RSLT0A	R/—	32	0x00
—	0xCB	Result register 0B	RSLT0B	R/—	32	0x00
—	0xCC	Result register 0C	RSLT0C	R/—	32	0x00
—	0xCD	Result register 0D	RSLT0D	R/—	32	0x00
—	0xCE	Result register 0E	RSLT0E	R/—	32	0x00
—	0xCF	Result register 0F	RSLT0F	R/—	32	0x00
—	0xD0	Result register 10	RSLT10	R/—	32	0x00
—	0xD1	Result register 11	RSLT11	R/—	32	0x00
—	0xD2	Result register 12	RSLT12	R/—	32	0x00
—	0xD3	Result register 13	RSLT13	R/—	32	0x00
—	0xD4	Result register 14	RSLT14	R/—	32	0x00
—	0xD5	Result register 15	RSLT15	R/—	32	0x00
—	0xD6	Result register 16	RSLT16	R/—	32	0x00
—	0xD7	Result register 17	RSLT17	R/—	32	0x00
—	0xD8	Result register 18	RSLT18	R/—	32	0x00
—	0xD9	Result register 19	RSLT19	R/—	32	0x00
—	0xDA	Result register 1A	RSLT1A	R/—	32	0x00
—	0xDB	Result register 1B	RSLT1B	R/—	32	0x00
—	0xDC	Result register 1C	RSLT1C	R/—	32	0x00
—	0xDD	Result register 1D	RSLT1D	R/—	32	0x00
—	0xDE	Result register 1E	RSLT1E	R/—	32	0x00
—	0xDF	Result register 1F	RSLT1F	R/—	32	0x00
—	0xE0	Result register 20	RSLT20	R/—	32	0x00
—	0xE1	Result register 21	RSLT21	R/—	32	0x00
—	0xE2	Result register 22	RSLT22	R/—	32	0x00
—	0xE3	Result register 23	RSLT23	R/—	32	0x00
—	0xE4	Result register 24	RSLT24	R/—	32	0x00
—	0xE5	Result register 25	RSLT25	R/—	32	0x00
—	0xE6	Result register 26	RSLT26	R/—	32	0x00
—	0xE7	Result register 27	RSLT27	R/—	32	0x00
—	0xE8	Result register 28	RSLT28	R/—	32	0x00
—	0xE9	Result register 29	RSLT29	R/—	32	0x00
—	0xEA	Result register 2A	RSLT2A	R/—	32	0x00
—	0xEB	Result register 2B	RSLT2B	R/—	32	0x00
—	0xEC	Result register 2C	RSLT2C	R/—	32	0x00
—	0xED	Result register 2D	RSLT2D	R/—	32	0x00
—	0xEE	Result register 2E	RSLT2E	R/—	32	0x00
—	0xEF	Result register 2F	RSLT2F	R/—	32	0x00
—	0xF0	Result register 30	RSLT30	R/—	32	0x00
—	0xF1	Result register 31	RSLT31	R/—	32	0x00
—	0xF2	Result register 32	RSLT32	R/—	32	0x00
—	0xF3	Result register 33	RSLT33	R/—	32	0x00
—	0xF4	Result register 34	RSLT34	R/—	32	0x00
—	0xF5	Result register 35	RSLT35	R/—	32	0x00
—	0xF6	Result register 36	RSLT36	R/—	32	0x00
—	0xF7	Result register 37	RSLT37	R/—	32	0x00
—	0xF8	Result register 38	RSLT38	R/—	32	0x00
—	0xF9	Result register 39	RSLT39	R/—	32	0x00
—	0xFA	Result register 3A	RSLT3A	R/—	32	0x00
—	0xFB	Result register 3B	RSLT3B	R/—	32	0x00
—	0xFC	Result register 3C	RSLT3C	R/—	32	0x00
—	0xFD	Result register 3D	RSLT3D	R/—	32	0x00
—	0xFE	Result register 3E	RSLT3E	R/—	32	0x00
—	0xFF	Result register 3F	RSLT3F	R/—	32	0x00

Configuration Register CFG

	7	6	5	4	3	2	1	0
CFG	REGMD	—	INTPW[1:0]		INT1EN	INTLVL	—	—
R/W	R/W	—	R/W	R/W	R/W	R/W	—	—
Initial Value	0	0	0	0	0	0	0	0

REGMD:

This bit shows the register access mode of the serial interface (SPI/I2C). When set to "0", the internal address is incremented by 1 each time a 1-byte data is transmitted/received. When set to "1", the address is fixed to the same address.

INTPW[1:0]:

This bit indicates the pulse width setting when the interrupt signal is a pulse signal.

If the pulse width is set to 500[ns] or longer, an interrupt pulse may not be output depending on the timing when the CPU writes to the interrupt request register.

In this case, use the level output as the interrupt signal instead of the pulse output.

INTPW[1:0]	Description
00	250[ns] (4 MHz cycle) (initial value)
01	500[ns] (2 MHz cycle)
10	1000[ns] (1 MHz cycle)
11	2000[ns] (500 kHz cycle)

INT1EN:

Controls the INT1_S interrupt signal.

INT1EN	Description
0	INT1_S pin is merged with INT0_S to be output (initial value)
1	INT1_S pin is enabled

INTLVL:

Sets the interrupt level. Set to "0" for pulse output, or set to "1" for level output.

Interrupt Mask Register INTMSK *n* (*n* = 0, 1)

	7	6	5	4	3	2	1	0
INTMSK0	MSK0 [7]	MSK0 [6]	MSK0 [5]	MSK0 [4]	MSK0 [3]	MSK0 [2]	MSK0 [1]	MSK0 [0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	1	1	1	1	1	1	1	1

	7	6	5	4	3	2	1	0
INTMSK1	MSK1 [7]	MSK1 [6]	MSK1 [5]	MSK1 [4]	MSK1 [3]	MSK1 [2]	MSK1 [1]	MSK1 [0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	1	1	1	1	1	1	1	1

MSK0[7:0]:

Masks the interrupt notification to the host processor by the interrupt request register (INTREQ0). Set to "1" to mask the interrupt notification by REQ0[n] bit of INTREQ0.Set to "0" not to mask the interrupt notification.

MSK1[7:0]:

Masks the interrupt notification to the host processor by the interrupt request register (INTREQ1). Set to "1" to mask the interrupt notification by REQ1[n] bit of INTREQ1.Set to "0" not to mask the interrupt notification.

Operation Status Register STATUS

	7	6	5	4	3	2	1	0
STATUS	ST[7]	ST[6]	ST[5]	ST[4]	ST[3]	ST[2]	ST[1]	ST[0]
R/W	R/—	R/—	R/—	R/—	R/—	R/—	R/—	R/—
Initial Value	0	0	0	0	0	0	0	0

ST[7:0]:
Indicates the status of sensor measurement.

Error Code Register ERROR *n* (*n* = 0, 1)

	7	6	5	4	3	2	1	0
ERROR*n*	ER*n* [7]	ER*n* [6]	ER*n* [5]	ER*n* [4]	ER*n* [3]	ER*n* [2]	ER*n* [1]	ER*n* [0]
R/W	R/—	R/—	R/—	R/—	R/—	R/—	R/—	R/—
Initial Value	0	0	0	0	0	0	0	0

ER *n*[7:0]:
Indicates the interrupt source to the host processor. Each bit of this register is cleared by being read by the host processor.

Interrupt Request Register INTREQ*n* (*n* = 0, 1)

	7	6	5	4	3	2	1	0
INTREQ*n*	REQ*n* [7]	REQ*n* [6]	REQ*n* [5]	REQ*n* [4]	REQ*n* [3]	REQ*n* [2]	REQ*n* [1]	REQ*n* [0]
R/W	R/—	R/—	R/—	R/—	R/—	R/—	R/—	R/—
Initial Value	0	0	0	0	0	0	0	0

REQ*n*[7:0]:
Indicates the interrupt source to the host processor. Each bit of this register is cleared by being read by the host processor.

FIFO Register FIFO

	7	6	5	4	3	2	1	0
FIFO	FIFO [7]	FIFO [6]	FIFO [5]	FIFO [4]	FIFO [3]	FIFO [2]	FIFO [1]	FIFO [0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	x	x	x	x	x	x	x	x

FIFO [7:0]:
This register indicates the command processing results.This register is FIFO structure and read the data of given size.
When doing firmware update, the data with max 512 Byte unit input is available.

Parameter Register PRM*n* (*n* = 00 to 0F)

	7	6	5	4	3	2	1	0
PRM*n*	PRM*n*[7]	PRM*n* [6]	PRM*n* [5]	PRM*n* [4]	PRM*n* [3]	PRM*n* [2]	PRM*n* [1]	PRM*n* [0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

PRM*n*[7:0]:
This register sets the parameters of commands.

Command Register CMD*n* (*n* = 0, 1)

	7	6	5	4	3	2	1	0
CMD*n*	CMD*n*[7]	CMD*n*[6]	CMD*n*[5]	CMD*n*[4]	CMD*n*[3]	CMD*n*[2]	CMD*n*[1]	CMDn[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

CMD*n*[7:0]:
This register sets the measurement conditions of sensors and inputs commands such as measurement start/stop.

Command Entry Register ENT

	7	6	5	4	3	2	1	0
ENT	—	—	—	—	—	—	—	ENT
R/W	—	—	—	—	—	—	—	R/W
Initial Value	0	0	0	0	0	0	0	0

ENT:
After a command is set, set this bit "1" to notify the CPU of the command. When the CPU receives the command, this bit is cleared.

Result Register RSLT *n* (*n* = 00 to 3F)

	7	6	5	4	3	2	1	0
RSLT*n*	RSLT*n*[7]	RSLT*n* [6]	RSLT*n* [5]	RSLT*n* [4]	RSLT*n* [3]	RSLT*n* [2]	RSLT*n* [1]	RSLT*n* [0]
R/W	R/—	R/—	R/—	R/—	R/—	R/—	R/—	R/—
Initial Value	0	0	0	0	0	0	0	0

RSLT*n*[7:0]:
This register indicates the command processing results.

ABSOLUTE MAXIMUM RATINGS

(GND=0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage (Digital I/O)	V_{DD}	Ta=25°C	-0.3 to 4.6	V
Power supply voltage (Digital CORE)	V_{DDL}	Ta=25°C	-0.3 to 1.8	V
Input voltage	V_{IN}	Ta=25°C	-0.3 to 4.6	V
Output voltage	V_{OUT}	Ta=25°C	-0.3 to 4.6	V
Output current	I_{OUT}	Ta=25°C	-10 to 10	mA
Power dissipation	PD	Ta=25°C	0.8	W
Storage temperature	T_{STG}	—	-55 to 150	°C

RECOMMENDED OPERATION CONDITIONS

(GND=0V)

(GND=0V)

Parameter	Symbol	Condition	Range	Unit
Ambient temperature	T_a	—	-40 to 85	°C
Power supply voltage	V_{DD}	—	1.7 to 1.9	V
Input voltage	V_{IN0}	—	0 to V_{DD}	V
	V_{IN1}	*1	0 to 3.6	V
Input clock frequency	f_{CLK}	—	32.768±1%	kHz
VDDL pin external capacitance	C_L	—	2.2±50%	µF

*1 SCL_S, SDA_S, SDA0_M, SCL0_M, PA0, PA1 using as I^2C bus interface.

OPERATING CONDITIONS OF FLASH MEMORY

(GND=0V)

Parameter	Symbol	Condition	Range	Unit
Ambient temperature	Ta	—	-40 to 85	°C
Power supply voltage	V_{DD}	—	1.7 to 1.9	V
Rewrite count	C_{EP}	—	1000	times
Data retention	Y_{DR}	—	10	years

ELECTRICAL CHARACTERISTICS

DC Characteristics (1/2)

(V_{DD}=1.7 to 1.9V, GND=0V, Ta=-40 to 85°C)

Parameter	Symbol	Condition	Standard value			Unit
			Min.	Typ.	Max.	
Power consumption (Sleep)	IDD2	CPU stop *1	—	2.5	120	μA
Power consumption (Low-speed operation)	IDD3	CPU 32.768kHz operation *1	—	0.5	0.7	mA
Power consumption (High-speed operation)	IDD4	CPU 32MHz operation	—	5.0	6.5	mA
Power consumption (At reset)	IDD-R	RESETN pin is Low	—	0.4	0.6	mA

*1 operate with the low-speed clock and stop the high-speed clock (FLL). Peripherals except HostIF are initial state.

DC Characteristics (2/2)

(V_{DD}=1.7 to 1.9V, GND=0V, Ta=-40 to 85°C)

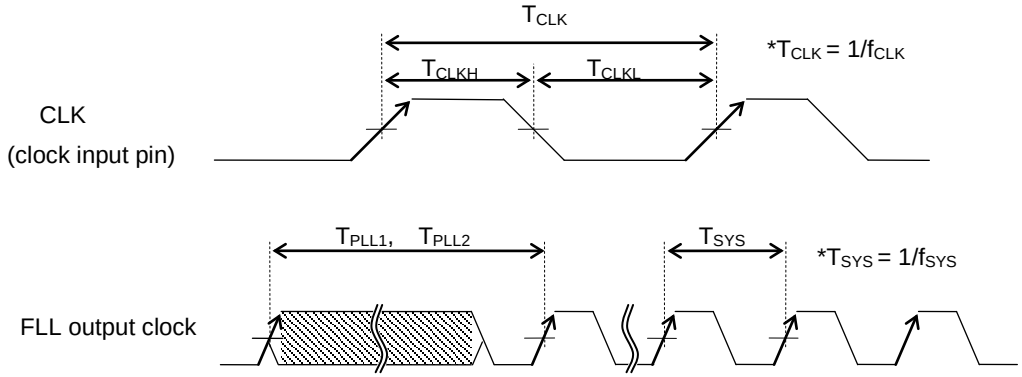
Parameter	Symbol	Condition	Standard value			Unit
			Min.	Typ.	Max.	
Output voltage 1	VOH1	—	—	—	—	V
(SDA0_M, SCL0_M PA0[*1], PA1[*1] SCL_S[*2], SDA_S[*2])	VOL1	IOL = 3mA	—	—	V_{DD} x 0.2	
Output voltage 2	VOH2	IOH = -2mA	V_{DD} - 0.45	—	—	V
(Other pins)	VOL2	IOL = 2mA	—	—	0.45	
Output leakage	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	1	μA
	IOOL	VOL = 0V (in high-impedance state)	-1	—	—	
input current 1	IIH1Z	VIH = V_{DD}	—	—	1	μA
	IIL1Z	VIL = GND	-1	—	—	
	IIH1	VIH = V_{DD} (pull-down)	2	—	200	
	IIL1	VIL = GND (pull-up)	-200	—	-2	
Input voltage	VIH1	—	V_{DD} x 0.7	—	—	V
	VIL1	—	—	—	V_{DD} x 0.3	

*1 Output voltage 1 shows the characteristic in case the secondary pin function (I2C) is selected.
*2 Output voltage 1 shows the characteristic in case I2C is selected for host interface.

AC Characteristics (Clock)

(V_{DD}=1.7 to 1.9V,GND= 0V, Ta=-40 to 85°C)

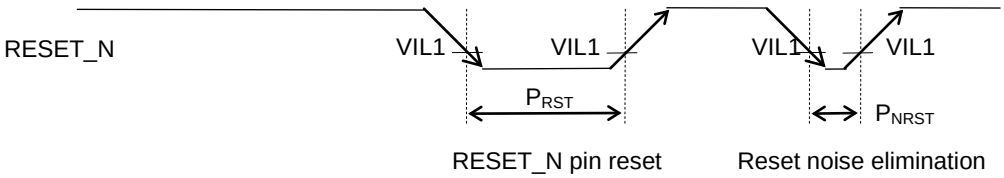
Parameter	Symbol	Condition	Standard value			Unit
			Min.	Typ.	Max.	
Input clock frequency	f_{CLK}	—	Typ. -1%	32.768	Typ. +1%	kHz
Input clock High pulse width	T_{CLKH}	—	Typ. -1%	15.259	Typ. +1%	µs
Input clock Low pulse width	T_{CLKL}	—	Typ. -1%	15.259	Typ. +1%	µs
System clock frequency	f_{SYS}	f_{CLK} = 32.768kHz	Typ -5%	32	Typ +5%	MHz
FLL activation time (Normal activation)	T_{FLL1}	f_{CLK} = 32.768kHz	—	—	1	ms
FLL activation time (Fast activation)	T_{FLL2}	f_{CLK} = 32.768kHz	—	75	—	µs



AC Characteristics (Reset)

(V_{DD}=1.7 to 1.9V, GND= 0V, Ta=-40 to 85°C)

Parameter	Symbol	Condition	Standard value			Unit
			Min.	Typ.	Max.	
Reset pulse width	P_{RST}	—	400	—	—	µs
Reset noise elimination pulse width	P_{NRST}	—	—	—	0.1	

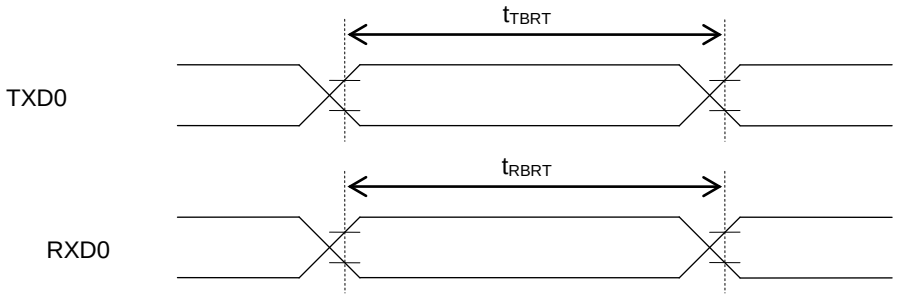


AC Characteristics (UART)

(V_{DD}=1.7 to 1.9V, GND=0V, Ta=-40 to 85°C)

Parameter	Symbol	Condition	Standard value			Unit
			Min.	Typ.	Max.	
Transferring baud-rate	t_{TBRT}	—	—	BRT*[1]	—	s
Receiving baud-rate	t_{RBRT}	—	BRT*[1] -3%	BRT*[1]	BRT*[1] +3%	s

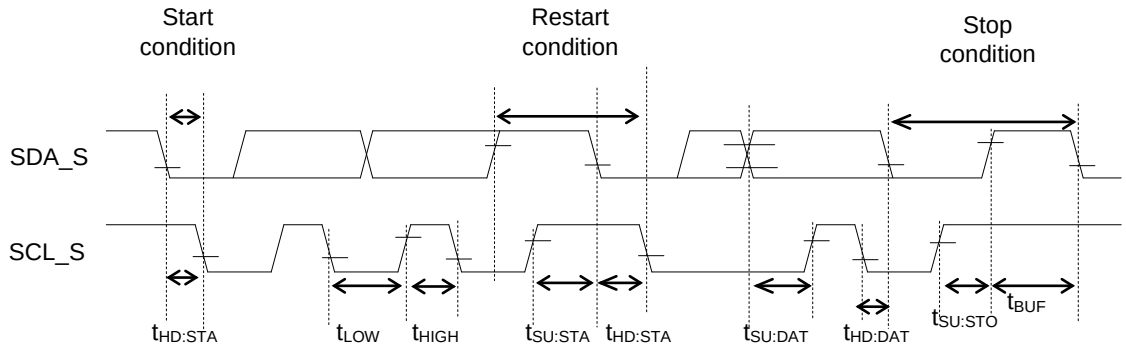
*1 Baud rate period (including the error of the clock frequency selected) set with the UART0 baud rate register (UA0BRTL,H) and the UART0 mode register 0 (UA0MOD0).



AC Characteristics (Host Interface: I2C Slave Interface)

(V_{DD}=1.7 to 1.9V, GND=0V, Ta= -40 to 85°C)

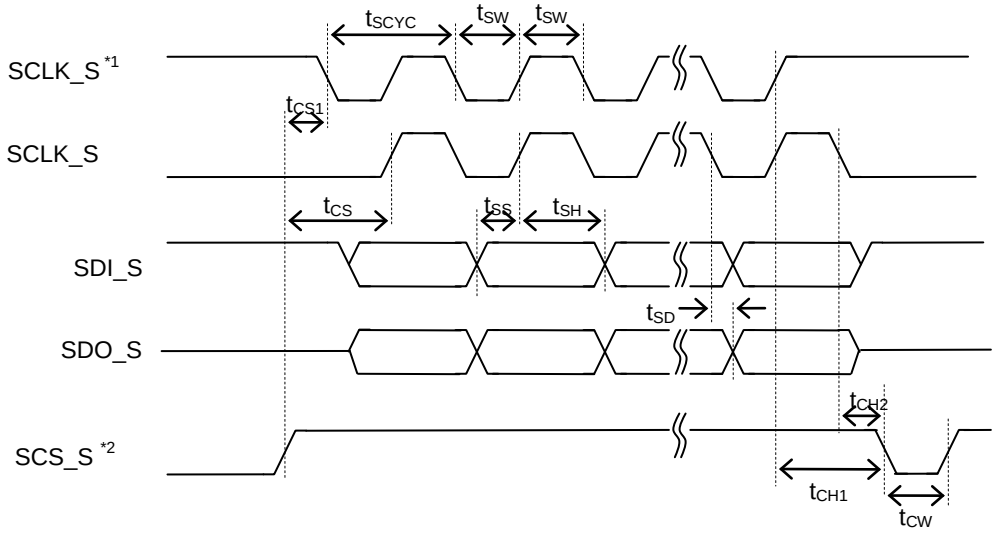
Parameter	Symbol	Condition	Standard value			Unit
			Min.	Typ.	Max.	
SCL_S clock frequency	f_{SCL}	—	—	—	400	kHz
SCL_S hold time (start/restartcondition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL_S "L" level time	t_{LOW}	—	1.3	—	—	µs
SCL_S "H" level time	t_{HIGH}	—	0.6	—	—	µs
SCL_S setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA_S hold time	$t_{HD:DAT}$	—	0	—	—	ns
SDA_S setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA_S setup time (P: Stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus free time	t_{BUF}	—	1.3	—	—	µs



AC Characteristics (Host Interface: SPI Slave Interface)

(V_{DD}=1.7 to 1.9V, GND=0V, Ta= -40 to 85°C)

Parameter	Symbol	Condition	Standard value			Unit
			Min.	Typ.	Max.	
SCLK_S input cycle	t_{SCYC}	—	250	—	—	ns
SCLK_S input pulse width	t_{SW}	—	120	—	—	ns
SCS_S setup time	t_{CS1}	—	80	—	—	ns
	t_{CS2}	—	80	—	—	ns
SCS_S hold time	t_{CH1}	—	80	—	—	ns
	t_{CH2}	—	80	—	—	ns
SCS_S input pulse width	t_{CW}	—	90	—	—	ns
SDO_S output delay time	t_{SD}	—	—	—	100	ns
SDI_S input setup time	t_{SS}	—	60	—	—	ns
SDI_S input hold time	t_{SH}	—	60	—	—	ns



*1 As for SPI, if Host keeps SCLK high while communication is standby, there are cases when this LSI cannot enter SleepDeep mode until SCS_S becomes non-active.
*2 Either “High active” or “Low active” can be selected for polarity of SCS_S.

AC Characteristics (I2C Master Interface: Standard Mode 100 kHz)

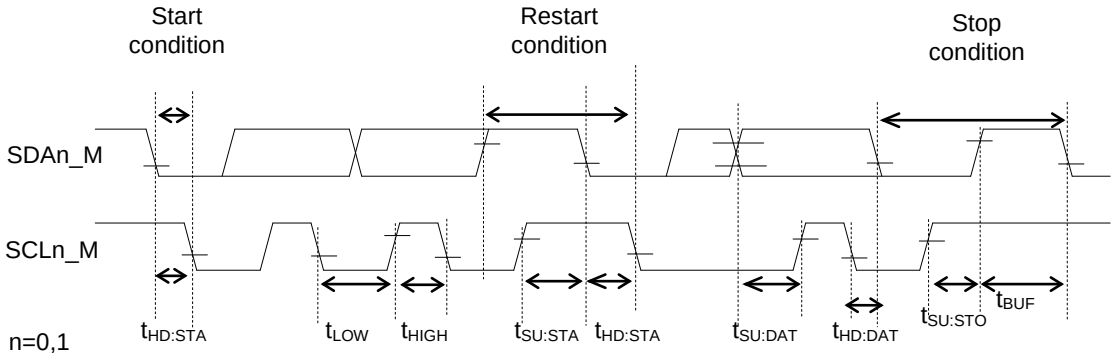
(V_{DD}=1.7 to 1.9V, GND=0V, Ta= -40 to 85°C)

Parameter	Symbol	Condition	Standard value			Unit
			Min.	Typ.	Max.	
SCLn_M clock frequency	f_{SCL}	—	—	—	100	kHz
SCLn_M hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCLn_M "L" level time	t_{LOW}	—	4.7	—	—	µs
SCLn_M "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCLn_M setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDAn_M hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDAn_M setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDAn_M setup time (P: Stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus free time	t_{BUF}	—	4.7	—	—	µs

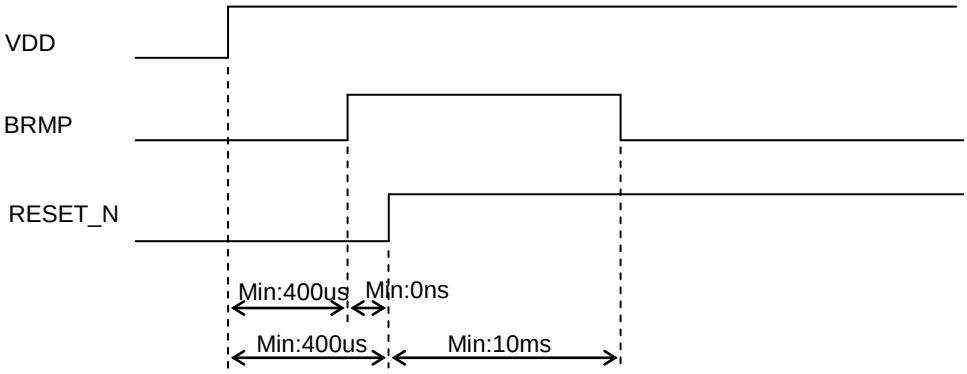
AC Characteristics (I2C Master Interface: Fast Mode 400 kHz)

(V_{DD}=1.7 to 1.9V, GND=0V, Ta= -40 to 85°C)

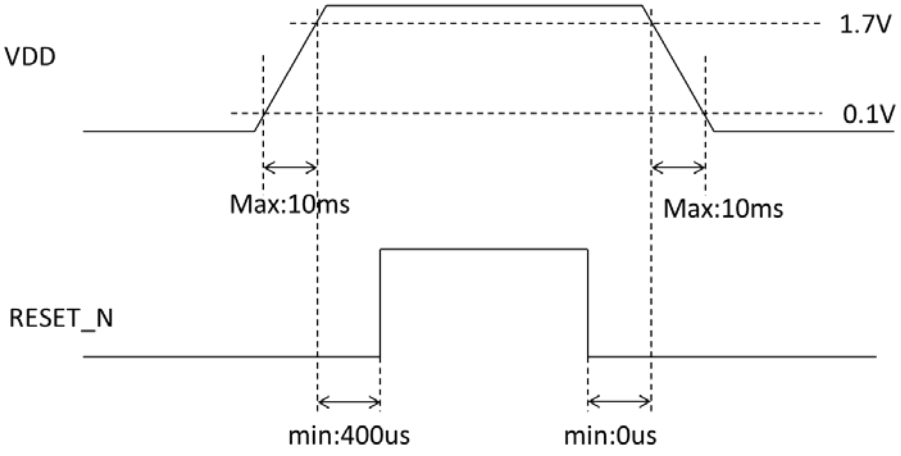
Parameter	Symbol	Condition	Standard value			Unit
			Min.	Typ.	Max.	
SCLn_M clock frequency	fSCL	—	—	—	400	kHz
SCLn_M hold time (start/restart condition)	tHD:STA	—	0.6	—	—	µs
SCLn_M "L" level time	tLOW	—	1.3	—	—	µs
SCLn_M "H" level time	tHIGH	—	0.6	—	—	µs
SCLn_M setup time (restart condition)	tSU:STA	—	0.6	—	—	µs
SDAn_M hold time	tHD:DAT	—	0	—	—	µs
SDAn_M setup time	tSU:DAT	—	0.1	—	—	µs
SDAn_M setup time (P: Stop condition)	tSU:STO	—	0.6	—	—	µs
Bus free time	tBUF	—	1.3	—	—	µs



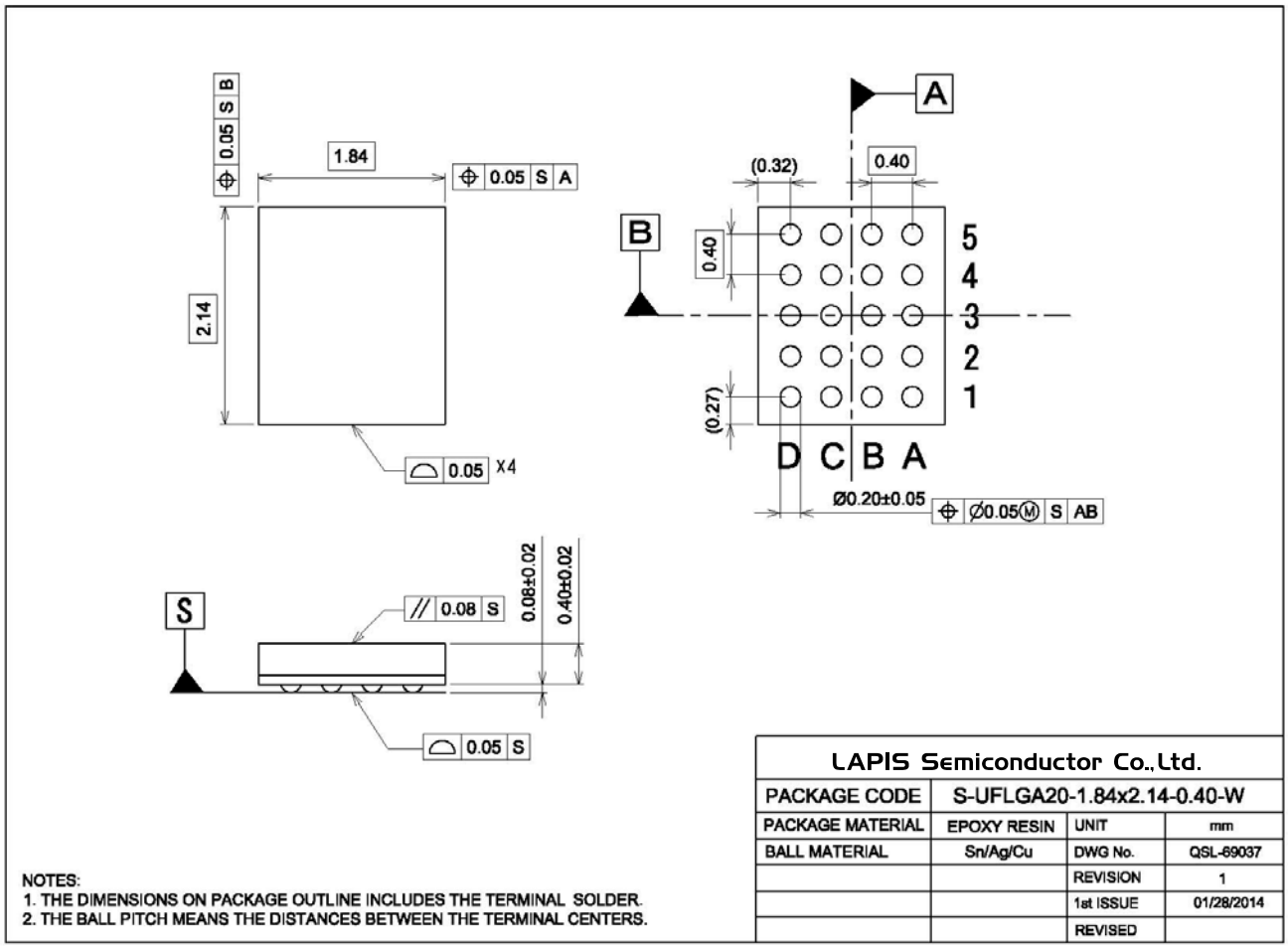
AC Characteristics (Firmware update)



Power-on/Power-off



PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Issue Date	Page		Description
		Previous Edition	Current Edition	
PEDL630Q791-01	2014.5.15	-	-	Preliminary Edition issued
FEDL630Q791-01	2014.10.22	-	-	Final Edition issued

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