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ML610Q794G

Sensor Control Hub 8-bit Microcontroller

■ General Description

The ML610Q794G is a high-performance 8-bit low power microcontroller optimized for sensor hub applications that integrates LAPIS Semiconductor's original high-performance 8-bit CPU core, with a 16-bit multiplier/divider co-processor, 64 KByte flash memory, 4 KByte RAM, multiple interfaces for various sensors and host interfaces with 8KByte logging RAM in 48pin TQFP package. The ML610Q794G is an ideal sensor hub microcontroller for personal healthcare equipments, wearable devices, and sensor nodes that all require power efficient control and data collection from multiple sensors.

■ Features

- CPU
  - —8-bit RISC CPU (CPU name: uX-U8/100)
  - —16-bit length instruction system
  - —Minimum instruction execution time
    - 30.5 us (32.768 kHz system clock)
    - 0.25 us (4.096 MHz system clock)
  - —Built-in co-processor for multiplication, division, and multiply-accumulate operations
    - Multiplication (Input: 16-bit x 16-bit, Output: 32-bit)
    - Division (Input: 32-bit/16-bit, Output: 32-bit)
    - Multiply-accumulate (Input: 16-bit x 16-bit + 32-bit, Output: 32-bit)

- Internal memory
  - —64KByte Flash ROM (32KWord x 16-bits)
  - —4KByte SRAM (4KWord x 8-bits)

- Interrupt controller
  - —Non-maskable interrupt: 1 source
  - —Maskable interrupt: 29 sources
    - Number of internal sources: 13 (Timer: 6, ADC: 1, HOST I/F: 1, Arithmetic unit: 1, UART: 1, SPI: 1, SIO: 1, I2C: 1)
    - Number of external sources: 16

- Timer
  - —8-bit auto-reload timer x 6ch (These timers can be used as 16-bit auto-reload timer x 3ch)
  - —Watchdog timer (WDT) x 1ch

- Serial interface
  - —SPI interface with master function x 1ch
  - —I2C interface with master function x 1ch
  - —UART interface (two-wire, full duplex communication with 16-bit FIFO) x 1ch
  - —SIO interface (two-wire, half-duplex communication) x 1ch

- Host interface
  - —Serial interface with slave function (SPI or I2Cis selectable) x 1ch
  - —Outputs a host processor interrupt x 1ch (secondary function of general-purpose I/O port)
  - —8-KByte RAM for data logging data

● General-purpose I/O port
—8-bit input/output port x 2ch
—5-bit input/output port x 1ch

● A/D converter
—12-bit successive approximation type A/D converter x 2ch

● Coprocessor
—Square Root operation (Input: 18 bit, Output: 19 bit)

● Power consumption control function
- CPU operation mode
  Supports steps from high to low frequency operation
- HALT mode
  Supports HALT mode for stopping CPU only
  Returning from the HALT mode : 77usec

● Input clock
- 32.768 kHz Crystal or Oscillator Input

● Power supply voltage
-Analog section: 2.5V to 3.6V
-Digital I/O section: 2.5V to 3.6V
-Digital core section: supplied by the internal voltage regulator

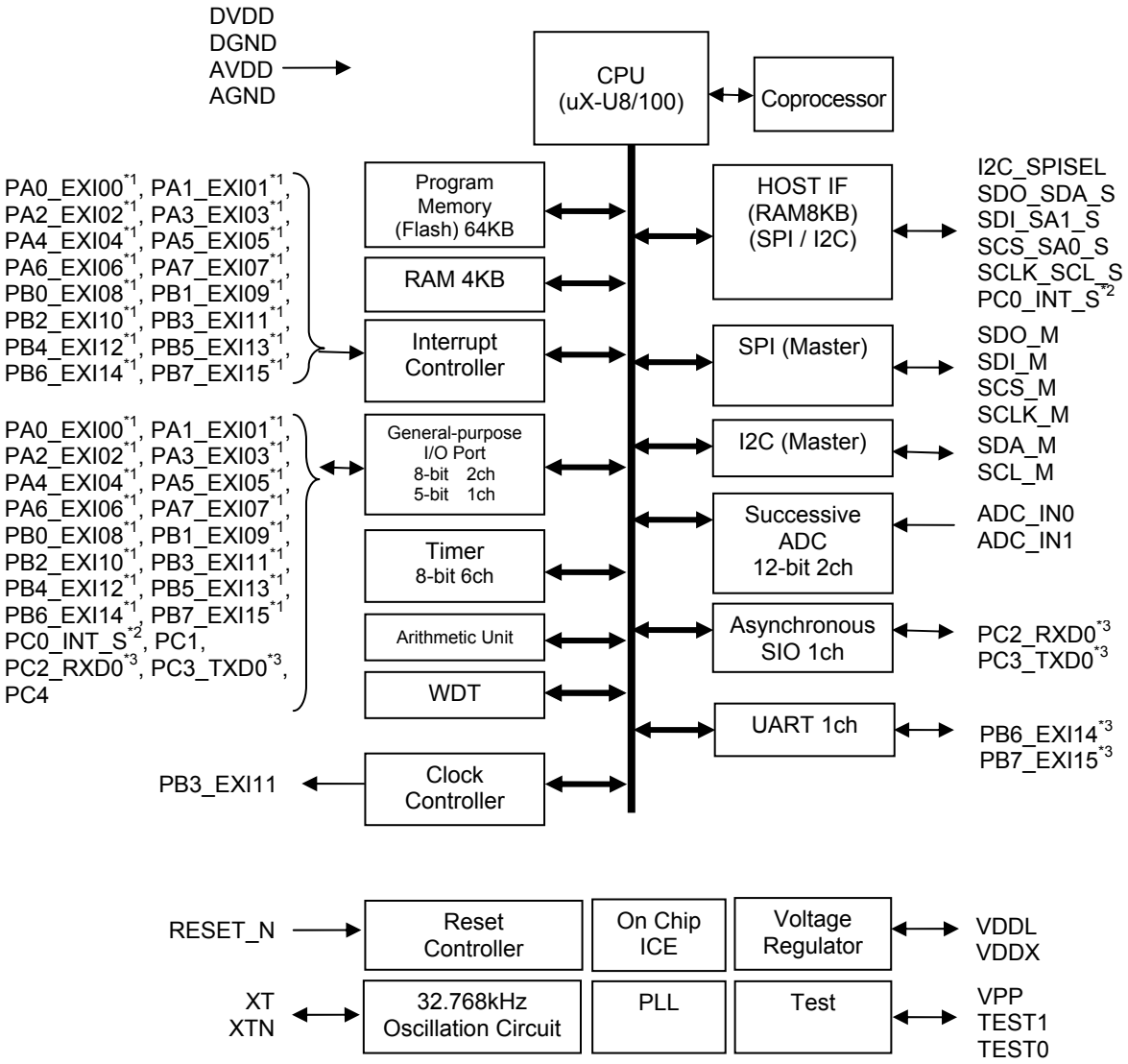
● Power consumption
—High-speed operation (4.096MHz): 1.0mA
—HALT Mode: 1.1uA

● Operating frequency
—High-speed clock: 4.096 MHz
—Low-speed clock: 32.768kHz

● Operating temperature
—Ambient temperature: -30°C to +85°C (FLASH erase/programming -30°C to +60°C)

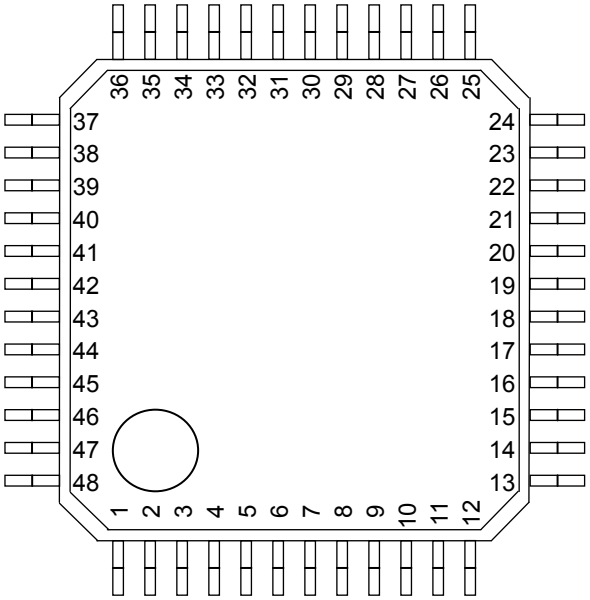
● Package
—48-pin QFP (TQFP48-0707-0.50)

■ Block Diagram



*1 Shared by the interrupt pins and the general-purpose I/O port
*2 Shared by the interrupt output pin of the host interface and the general-purpose I/O port
*3 Shared by the UART/Asynchronous SIO transmit/receive pins and the general-purpose I/O port

■ Pin Configuration (Top View)



48pin QFP (TQFP48-0707-0.50) Pin Layout

■ List of Pins

PIN No.	Symbol	Input/output	Polarity	Function
38	AGND	—	—	Analog GND
39	AVDD	—	—	Analog power supply
36	DGND	—	—	Digital IO/core GND
35	DVDD	—	—	Digital I/O power supply
34	VDDL	—	—	Digital core power supply (generated by internal regulator)
37	VDDX	—	—	Voltage regulator output for 32.768kHz crystal
48	I2C_SPISEL	I	—	Selects the interface with a host processor I2C interface when I2C_SPISEL=1 SPI interface when I2C_SPISEL=0
3	SDO_SDA_S	IO	—	SDA of I2C slave interface when I2C_SPISEL = 1
		O	—	SDO of SPI slave interface when I2C_SPISEL = 0 (This pin becomes Hi-Z except during not output any data.)
17	SDI_SA1_S	I	—	I2C slave address when I2C_SPISEL = 1
		I	—	SDI of SPI slave interface when I2C_SPISEL = 0
5	SCS_SA0_S	I	—	I2C slave address when I2C_SPISEL = 1
		I	Positive	SCS of SPI slave interface when I2C_SPISEL = 0
4	SCLK_SCL_S	I	—	SCL of I2C slave interface when I2C_SPISEL = 1
		I	—	SCLK of SPI slave interface when I2C_SPISEL = 0
32	SDA_M	IO	—	SDA of I2C master interface
33	SCL_M	O	—	SCL of I2C master interface
6	SDO_M	O	—	SDO of SPI master interface
19	SDI_M	I	—	SDI of SPI master interface
7	SCS_M	O	Positive	SCS of SPI master interface
8	SCLK_M	O	—	SCLK of SPI master interface
40	ADC_IN1	I	—	Successive ADC input 1
41	ADC_IN0	I	—	Successive ADC input 0
10	PC0_INT_S	IO	—	Primary function: GPIO
		O	Negative	Secondary function: Interrupt output for host interface
2	PC1	IO	—	GPIO
11	PC2_RXD0	IO	—	Primary function: GPIO
		I	—	Secondary function: RXD of Asynchronous SIO
12	PC3_TXD0	IO	—	Primary function: GPIO
		O	—	Secondary function: TXD of Asynchronous SIO
18	PC4	IO	—	GPIO
16	PA0_EXI00	IO	—	GPIO/external interrupt input
31	PA1_EXI01	IO	—	GPIO/external interrupt input
20	PA2_EXI02	IO	—	GPIO/external interrupt input
30	PA3_EXI03	IO	—	GPIO/external interrupt input
21	PA4_EXI04	IO	—	GPIO/external interrupt input
29	PA5_EXI05	IO	—	GPIO/external interrupt input
28	PA6_EXI06	IO	—	GPIO/external interrupt input
27	PA7_EXI07	IO	—	GPIO/external interrupt input
26	PB0_EXI08	IO	—	GPIO/external interrupt input
25	PB1_EXI09	IO	—	GPIO/external interrupt input
22	PB2_EXI10	IO	—	GPIO/external interrupt input
23	PB3_EXI11	IO	—	GPIO/external interrupt input

		O	—	32.768kHz clock for output
13	PB4_EXI12	IO	—	GPIO/external interrupt input
14	PB5_EXI13	IO	—	GPIO/external interrupt input
15	PB6_EXI14	IO	—	Primary function: GPIO/external interrupt input
		I	—	Secondary function: UART data receiving
9	PB7_EXI15	IO	—	Primary function: GPIO/external interrupt input
		O	—	Secondary function: UART data transmitting
1	RESET_N	I	Negative	System reset input
47	XT	I	—	Oscillation pin for 32.768kHz crystal
46	XTN	IO	—	Oscillation pin for 32.768kHz crystal
43	HXT	—	—	Test pin(open)
42	HXTN	—	—	Test pin(open)
24	VPP	—	—	Test pin(open)
44	TEST1	I	—	Test pin
45	TEST0	I	—	Test pin/remap pin (for firmware update)

■ Termination of Unused Pins

Pin	Recommended pin termination
VPP	open
HXT, HXTN	open
TEST0	open
TEST1	open
RESET_N	open, or connect a pull-up resistor
PA0~PA7	open *1
PB0~PB7	open *1
PC0~PC4	open *1
ADC_IN0~1	open
SDA_M, SCL_M	open
SDO_M, SCS_M, SCLK_M	open
SDI_M	Please connect a pull-down resistor
SCLK_SCL_S, SCS_SA0_S, SDI_SA1_S, SDO_SDA_S	Please apply low level to I2C_SPISEL pin, and connect a pull-down resistor to each of these pins

[Note]

*1 The current consumption may become excessively large if unused input ports and input/output ports are left open with setting high impedance input. It is recommended to set those unused ports to “input mode with a pull-down resistor”, “input mode with a pull-up resistor”, or “output mode” by setting the port control registers.

■ Host Interface

A Host Processor has access to multiple sensors through the Host Interface on the ML610Q794G. The host interface supports I2C or SPI (selectable), output of interrupt signal to a host processor and an 8-KByte FIFO, and can be configured by the followings register map.

- Register Map

Address		Name	Symbol (Byte)	R/W	Size	Initial Value
Write	Read					
00H	80H	Configuration register	CFG	R/W	8	00H
01H	81H	Sensor interrupt mask register 0	INTMSK0	R/W	8	FFH
02H	82H	Sensor interrupt mask register 1	INTMSK1	R/W	8	FFH
03H ~ 07H	83H ~ 87H	reserved	—	—	—	—
08H	88H	Operation status register	STATUS	R/—	8	FEH
09H	89H	Sensor interrupt request register 0	INTREQ0	R/—	8	00H
0AH	8AH	Sensor interrupt request register 1	INTREQ1	R/—	8	00H
0BH	8BH	Error code register 0	ERROR0	R/—	8	00H
0CH	8CH	Error code register 1	ERROR1	R/—	8	00H
0DH~ 0FH	8DH~ 8FH	reserved	—	—	—	—
10H	90H	Command register 0	CMD0	R/W	8	00H
11H	91H	Command register 1	CMD1	R/W	8	00H
12H	92H	Parameter register 0	PRM0	R/W	8	00H
13H	93H	Parameter register 1	PRM1	R/W	8	00H
14H	94H	Parameter register 2	PRM2	R/W	8	00H
15H	95H	Parameter register 3	PRM3	R/W	8	00H
16H	96H	Parameter register 4	PRM4	R/W	8	00H
17H	97H	Parameter register 5	PRM5	R/W	8	00H
18H	98H	Parameter register 6	PRM6	R/W	8	00H
19H	99H	Parameter register 7	PRM7	R/W	8	00H
1AH	9AH	Parameter register 8	PRM8	R/W	8	00H
1BH	9BH	Parameter register 9	PRM9	R/W	8	00H
1CH	9CH	Parameter register A	PRMA	R/W	8	00H
1DH	9DH	Parameter register B	PRMB	R/W	8	00H
1EH	9EH	Parameter register C	PRMC	R/W	8	00H
1FH	9FH	Command entry register	ENT	R/W	8	00H
20H	A0H	Result register 00	RSLT00	R/—	8	00H
21H	A1H	Result register 01	RSLT01	R/—	8	00H
22H	A2H	Result register 02	RSLT02	R/—	8	00H
23H	A3H	Result register 03	RSLT03	R/—	8	00H
24H	A4H	Result register 04	RSLT04	R/—	8	00H
25H	A5H	Result register 05	RSLT05	R/—	8	00H
26H	A6H	Result register 06	RSLT06	R/—	8	00H
27H	A7H	Result register 07	RSLT07	R/—	8	00H
28H	A8H	Result register 08	RSLT08	R/—	8	00H
29H	A9H	Result register 09	RSLT09	R/—	8	00H
2AH	AAH	Result register 0A	RSLT0A	R/—	8	00H
2BH	ABH	Result register 0B	RSLT0B	R/—	8	00H

2CH	ACH	Result register 0C	RSLT0C	R/—	8	00H
2DH	ADH	Result register 0D	RSLT0D	R/—	8	00H
2EH	AEH	Result register 0E	RSLT0E	R/—	8	00H
2FH	AFH	Result register 0F	RSLT0F	R/—	8	00H
30H	B0H	Result register 10	RSLT10	R/—	8	00H
31H	B1H	Result register 11	RSLT11	R/—	8	00H
32H	B2H	Result register 12	RSLT12	R/—	8	00H
33H	B3H	Result register 13	RSLT13	R/—	8	00H
34H	B4H	Result register 14	RSLT14	R/—	8	00H
35H	B5H	Result register 15	RSLT15	R/—	8	00H
36H	B6H	Result register 16	RSLT16	R/—	8	00H
37H	B7H	Result register 17	RSLT17	R/—	8	00H
38H	B8H	Result register 18	RSLT18	R/—	8	00H
39H	B9H	Result register 19	RSLT19	R/—	8	00H
3AH	BAH	Result register 1A	RSLT1A	R/—	8	00H
3BH	BBH	Result register 1B	RSLT1B	R/—	8	00H
3CH	BCH	Result register 1C	RSLT1C	R/—	8	00H
3DH	BDH	Result register 1D	RSLT1D	R/—	8	00H
3EH	BEH	Result register 1E	RSLT1E	R/—	8	00H
3FH	BFH	Result register 1F	RSLT1F	R/—	8	00H
40H	C0H	Result register 20	RSLT20	R/W	8	Undefined
41H ~ 7FH	C1H ~ FFH	reserved	—	—	—	—

- Configuration Register CFG

	7	6	5	4	3	2	1	0
CFG	REGMD	SPI3M	—	—	—	INTLVL	—	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

REGMD:
Sets the access mode of the serial interface (I2C/SPI).
When set REGMD= "0", the internal address automatically increases an address value 1-byte by every 1-byte data transmitting /receiving.
Wnen set REGMD= "1", the internal address does not increase an address value.
The Result register 20 does not increase an address value automatically. In addition, it is prohibited to read the Result register 1F and the Result register 20 successively by setting REGMD= "0".

SPI3M:
If the host interface is set "SPI" by applying low level to I2C_SPISEL pin, 3-wires interface (SPI3M="1") or 4-wires interface (SPI3M="0") is selectable.

INTLVL:
The ML610Q794G outputs the signal to a host processor for causing the interrupt in a host processor. When set INTLVL=”0”, this output signal is set to pulse output. And when set INTLVL=”1”, the output signal is set to level output.

- Sensor Interrupt Mask Register INTMSK0, INTMSK1

	7	6	5	4	3	2	1	0
INTMSK0	MSK0[7]	MSK0[6]	MSK0[5]	MSK0[4]	MSK0[3]	MSK0[2]	MSK0[1]	MSK0[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	1	1	1	1	1	1	1	1

	7	6	5	4	3	2	1	0
INTMSK1	MSK1[7]	MSK1[6]	MSK1[5]	MSK1[4]	MSK1[3]	MSK1[2]	MSK1[1]	MSK1[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	1	1	1	1	1	1	1	1

MSK0[7:0]:
Masks the interrupt notification to the host processor by the sensor interrupt request register (INTREQ0). Set to "1" to mask the interrupt notification by REQ0[*n*] bit of INTREQ0.Set to "0" not to mask the interrupt notification.

MSK1[7:0]:
Masks the interrupt notification to the host processor by the sensor interrupt request register (INTREQ1). Set to "1" to mask the interrupt notification by REQ1[*n*] bit of INTREQ1.Set to "0" not to mask the interrupt notification.

- Operation Status Register STATUS

	7	6	5	4	3	2	1	0
STATUS	ST[7]	ST[6]	ST[5]	ST[4]	ST[3]	ST[2]	ST[1]	ST[0]
R/W	R/—	R/—	R/—	R/—	R/—	R/—	R/—	R/—
Initial Value	1	1	1	1	1	1	1	0

ST[n](N=7 to 0):
This is for Indicating the status of sensor measurement.
The STAUS, INTREQ0 and INTREQ1 need to be read successfully by address increment mode.

- Sensor Interrupt Request Register INTREQ*n* (*n* = 0, 1)

	7	6	5	4	3	2	1	0
INTREQ*n*	REQ*n* [7]	REQ*n* [6]	REQ*n* [5]	REQ*n* [4]	REQ*n* [3]	REQ*n* [2]	REQ*n* [1]	REQ*n* [0]
R/W	R/—	R/—	R/—	R/—	R/—	R/—	R/—	R/—
Initial Value	0	0	0	0	0	0	0	0

REQ*n*[7:0]:
This is for indicating the interrupt source to the host processor. Each bit of this register is cleared by access (read) from the host processor.
The INTREQ0 and INTREQ1 need to be read successfully by address increments mode.

- Error Code Register ERROR *n* (*n* = 0, 1)

	7	6	5	4	3	2	1	0
ERROR*n*	ER*n* [7]	ER*n* [6]	ER*n* [5]	ER*n* [4]	ER*n* [3]	ER*n* [2]	ER*n* [1]	ER*n* [0]
R/W	R/—	R/—	R/—	R/—	R/—	R/—	R/—	R/—
Initial Value	0	0	0	0	0	0	0	0

ER *n*[7:0]:
This is for indicating the ERROR Code of host processor.

- Command Register CMD*n* (*n* = 0, 1)

	7	6	5	4	3	2	1	0
CMD*n*	CMD*n*[7]	CMD*n*[6]	CMD*n*[5]	CMD*n*[4]	CMD*n*[3]	CMD*n*[2]	CMD*n*[1]	CMD*n*[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

CMD*n*[7:0]:
This is for setting the measurement conditions of sensors and input commands such as measurement start/stop.

● Parameter Register PRM*n* (*n* = 0 to 9, A to C)

	7	6	5	4	3	2	1	0
PRM*n*	PRM*n*[7]	PRM*n* [6]	PRM*n* [5]	PRM*n* [4]	PRM*n* [3]	PRM*n* [2]	PRM*n* [1]	PRM*n* [0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

PRM*n*[7:0]:
This is for setting the parameters of commands.

● Command Entry Register ENT

	7	6	5	4	3	2	1	0
ENT	—	—	—	—	—	—	—	ENT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value	0	0	0	0	0	0	0	0

ENT:
After a command is set, set this bit "1" to notify the CPU of the command. When the CPU receives the command, this bit is cleared.

● Result Register RSLT *n* (*n* = 00 to 1F)

	7	6	5	4	3	2	1	0
RSLT*n*	RSLT*n*[7]	RSLT*n* [6]	RSLT*n* [5]	RSLT*n* [4]	RSLT*n* [3]	RSLT*n* [2]	RSLT*n* [1]	RSLT*n* [0]
R/W	R/—	R/—	R/—	R/—	R/—	R/—	R/—	R/—
Initial Value	0	0	0	0	0	0	0	0

RSLT*n*[7:0]:
This register indicates the processing result.

● Result Register RSLT20

	7	6	5	4	3	2	1	0
RSLT20	RSLT20[7]	RSLT20 [6]	RSLT20 [5]	RSLT20 [4]	RSLT20 [3]	RSLT20 [2]	RSLT20 [1]	RSLT20 [0]
R/W	R/—	R/—	R/—	R/—	R/—	R/—	R/—	R/—
Initial Value	X	X	X	X	X	X	X	X

RSLT20[7:0]:
This register indicates the processing result. As this register has a FIFO structure, read data with the given size.
This register can be written from a host processor only when using firmware update software which SDK offers.
For details. please refer to a [ML610Q793 SDK firmware updates software manuals].

■ Absolute Maximum Ratings

(DGND=AGND=0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage (Digital I/O)	V_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage (Digital CORE)	V_{DDL}	Ta = 25°C	–0.3 to +3.6	
Power supply voltage (Analog)	V_{DDA}	Ta = 25°C	–0.3 to +4.6	
Power supply voltage (Oscillation circuit)	V_{DDX}	Ta = 25°C	–0.3 to +3.6	
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	
Output current	I_{OUT}	Ta = 25°C	–12 to +11	mA
Power dissipation	PD	Ta = 25°C	0.9	W
Storage temperature	T_{STG}	—	–55 to +150	°C

■ Recommended Operation Conditions

(DGND=AGND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage (Digital I/O)	V_{DD}	—	2.5	3.3	3.6	V
Power supply voltage (Analog)	V_{DDA}	—	2.5	3.3	3.6	
Low-speed clock frequency	F_{OSC}	—		32.768		kHz
V_{DDL} external capacitance	C_{L0}	—	1.54	2.2	2.86	µF
Ambient temperature	Ta	FLASH read operation	-30	25	+85	°C
		FLASH erase/write operation	-30	25	+60	

■ Operating Conditions of Flash Memory

(DGND=AGND=0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	read operation	-30 to +85	°C
		erase/write operation	-30 to +60	
Power supply voltage	V_{DDA}	—	2.5 to 3.6	V
Rewrite count	C_{EP}	—	100	cycles
Data retention	Y_{DR}	—	10	years

■ Electrical Characteristics

● DC Characteristics (1/2)

(DVDD = AVDD = 2.5 to 3.6V, DGND = AGND = 0V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power consumption (HALT)	IDD2	CPU, PLL, ADC : stopped 4MHz clock : stopped 32kHz clock : operating	-	1.1	17.5	µA
Power consumption (Low-speed operation)	IDD3	CPU : operating PLL, ADC : stopped 4MHz clock : stopped 32kHz clock : operating	-	8.5	27	µA
Power consumption (High-speed operation 1)	IDD4-1	CPU, PLL : operating ADC : stopped 4MHz clock : operating 32kHz clock : operating	-	1.0	1.4	mA
Power consumption (High-speed operation 2)	IDD4-2	CPU, PLL, ADC : operating 4MHz clock : operating 32kHz clock : operating	-	1.6	2.4	mA

● DC Characteristics (2/2)

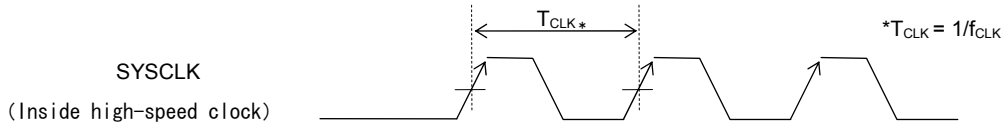
(DVDD = AVDD = 2.5 to 3.6V, DGND = AGND = 0V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage 1 (SDA_M,SCL_M)	VOH1	-	-	-	-	V
	VOL1	IOL1 = +3mA	-	-	0.4	
Output leakage 1 (SDA_M,SCL_M)	IOOH1	-	-	-	-	µA
	IOOL1	VOL=0V (in high-impedance state)	-1	-	-	
Output voltage 2 (Excluding SDA_M and SCL_M)	VOH2	IOH=-0.5mA	DVDD - 0.5	-	-	V
	VOL2	IOL= 0.5mA	-	-	0.5	
Output leakage 2 (Excluding SDA_M and SCL_M)	IOOH2	VOH= DVDD (in high-impedance state)	-	-	1	µA
	IOOL2	VOL= 0V (in high-impedance state)	-1	-	-	
Input current 1 (RESET_N, TEST1)	IIH1	VIH1=DVDD	-	-	1	µA
	IIL1	VIL1 = 0V	-600	-300	-2	
Input current 2 (TEST0)	IIH2	VIH1=DVDD	2	300	600	µA
	IIL2	VIL1 = 0V	-1	-	-	
Input current 3 (Excluding RESET_N, TEST1, and TEST0)	IIH3	VIH1 = DVDD(pull-down)	2	30	200	µA
	IIL3	VIL1 = 0V(pull-up)	-200	-30	-2	
	IIH3Z	VIH1=DVDD (in high-impedance state)	-	-	1	
	IIL3Z	VIL1= 0V (in high-impedance state)	-1	-	-	
Input voltage	VIH1	-	DVDD × 0.7	-	-	V
	VIL1	-	-	-	DVDD × 0.3	

●AC Characteristics (Clock)

(Unless otherwise specified, DVDD = AVDD = 2.5 to 3.6V, DGND = AGND = 0V, Ta = -30 to +85°C)

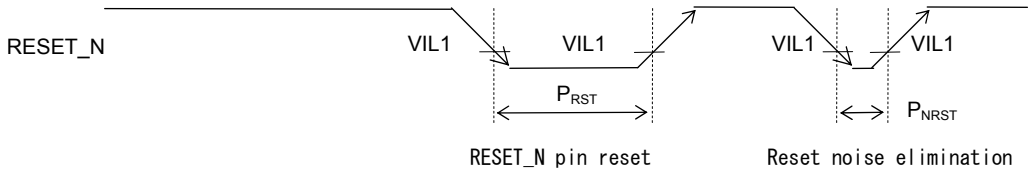
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Input clock frequency	f_{CLK}	-	3.89	4.096	4.30	MHz

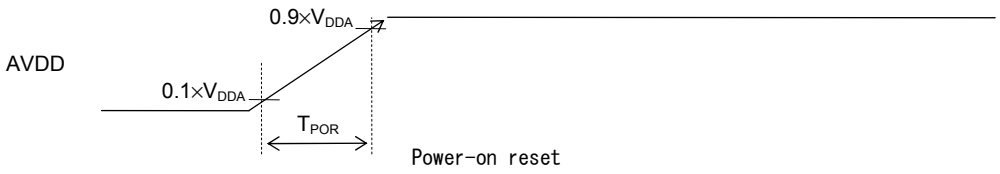


●AC Characteristics (Reset)

(Unless otherwise specified, DVDD = AVDD = 2.5 to 3.6V, DGND = AGND = 0V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Reset pulse width	P_{RST}	-	200	-	-	µs
Reset noise elimination pulse width	P_{NRST}	-	-	-	0.3	
Power on reset generated power rise time	T_{POR}	-	-	-	5	ms

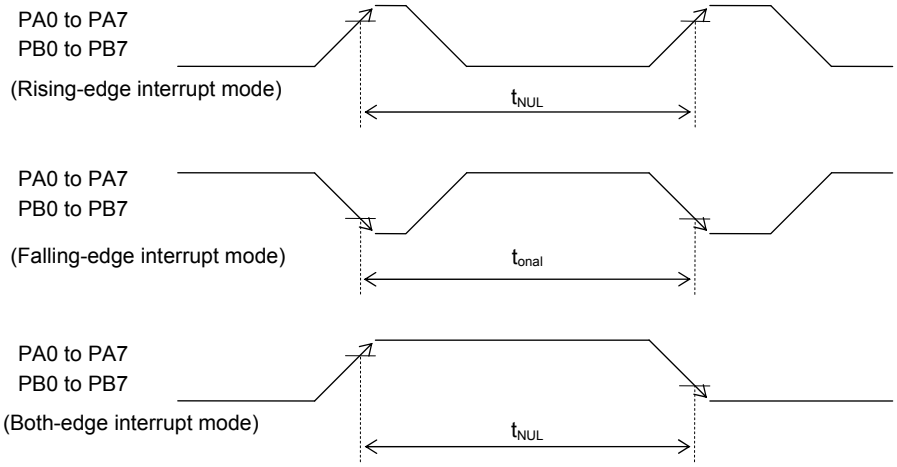




●AC Characteristics (External Interrupt)

(Unless otherwise specified, DVDD = AVDD = 2.5 to 3.6V, DGND = AGND = 0V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	-	106.8	µs

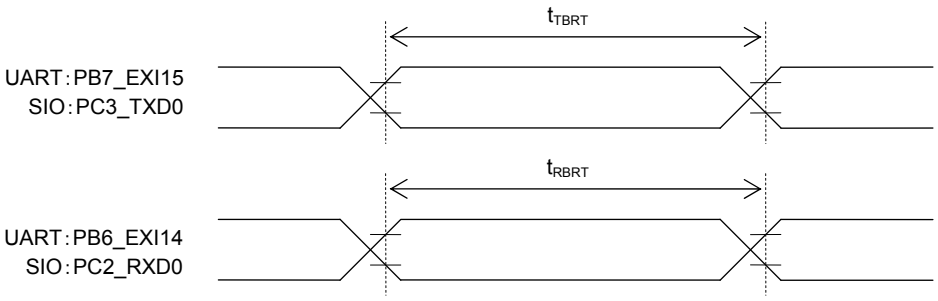


●AC Characteristics (UART/SIO)

(Unless otherwise specified, DVDD = AVDD = 2.5 to 3.6V, DGND = AGND = 0V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	-	-	BRT*1	-	s
Receive baud rate	t_{RBRT}	-	BRT*1 -3%	BRT*1	BRT*1 +3%	s

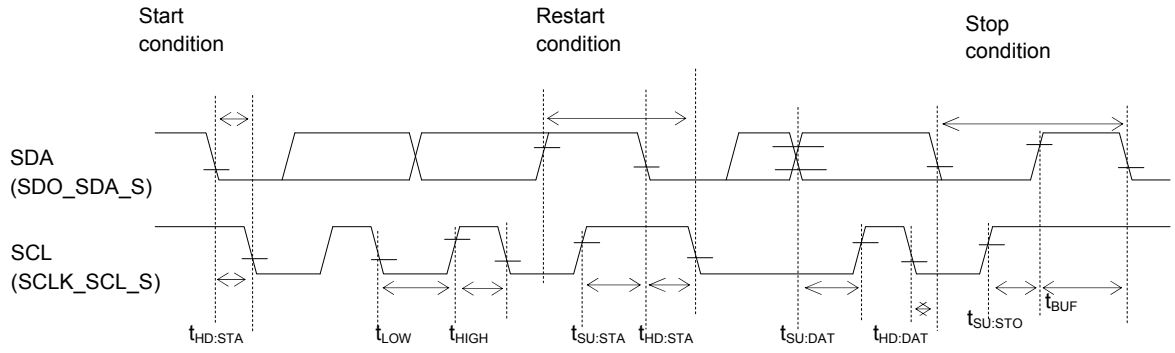
*1: UART : Baud rate period set with the UART baud rate dividing register (LSB/MSB).
SIO : Baud rate period set with the UART0 baud rate register (UA0BRTL,H) and the UART0 mode register 0 (UA0MOD0).



● AC Characteristics (Host Interface: I2C Slave Interface)

(Unless otherwise specified, DVDD = AVDD = 2.5 to 3.6, DGND = AGND = 0V, Ta = -30 to +85°C)

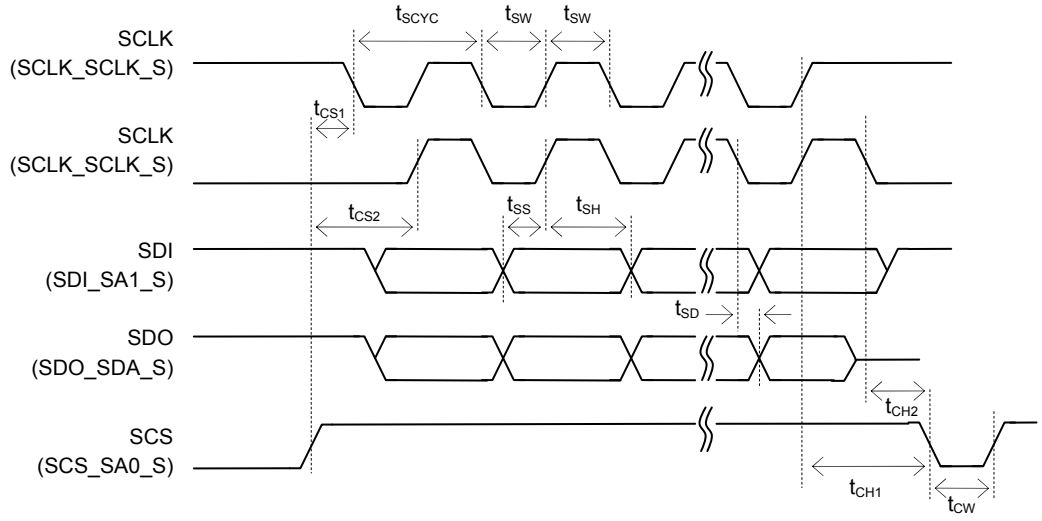
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL ”L” level time	t_{LOW}	—	1.3	—	—	µs
SCL ”H” level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	ns
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs



● AC Characteristics (Host Interface: SPI Slave Interface)

(Unless otherwise specified, DVDD = AVDD = 2.5 to 3.6, DGND = AGND = 0V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle	t_{SCYC}	-	0.5	-	-	µs
SCLK input pulse width	t_{SW}	-	0.2	-	-	µs
SCS setup time	t_{CS1}	-	80	-	-	ns
	t_{CS2}	-	80	-	-	ns
SCS hold time	t_{CH1}	-	80	-	-	ns
	t_{CH2}	-	80	-	-	ns
SCS input pulse width	t_{CW}	-	90	-	-	ns
SDO output delay time	t_{SD}	-	-	-	240	ns
SDI input setup time	t_{SS}	-	80	-	-	ns
SDI input hold time	t_{SH}	-	80	-	-	ns

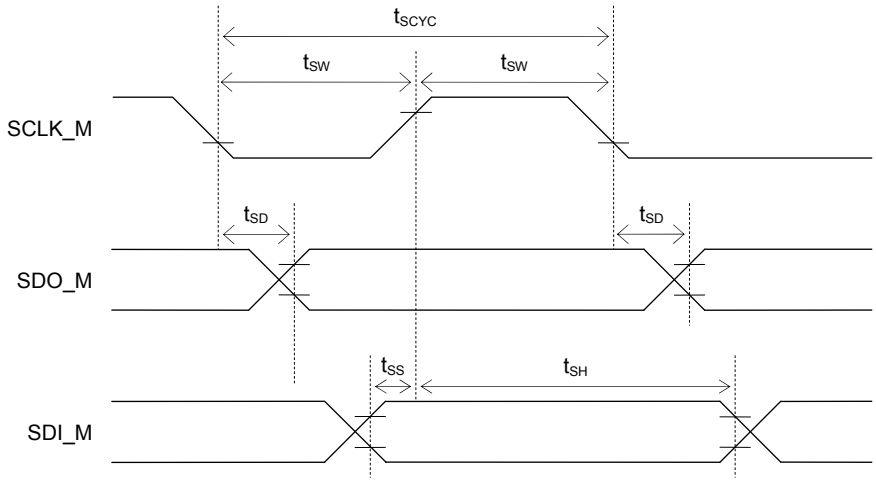


● AC Characteristics (SPI Master Interface)

(Unless otherwise specified, DVDD = AVDD = 2.5 to 3.6, DGND = AGND = 0V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK_M output cycle	t_{SCYC}	-	-	SCLK*1	-	s
SCLK_M output pulse width	t_{SW}	-	SCLK*1 ×0.4	SCLK*1 ×0.5	SCLK*1 ×0.6	s
SDO_M output delay time	t_{SD}	-	-	-	240	ns
SDI_M input setup time	t_{SS}	-	240	-	-	ns
SDI_M input hold time	t_{SH}	-	80	-	-	ns

*1: Internal clock cycle selected by the interface register



● AC Characteristics (I2C Master Interface: Standard Mode 100 kHz)

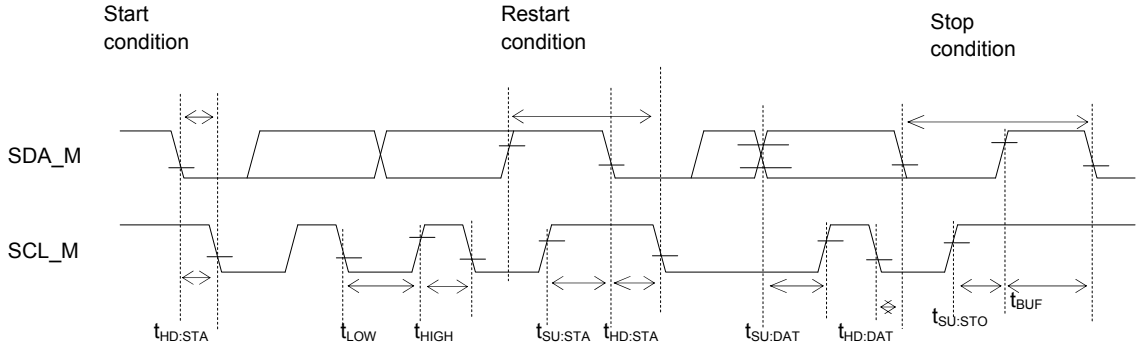
(Unless otherwise specified, DVDD = AVDD = 2.5 to 3.6, DGND = AGND = 0V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

● AC Characteristics (I2C Master Interface: Fast Mode 400 kHz)

(Unless otherwise specified, DVDD = AVDD = 2.5 to 3.6, DGND = AGND = 0V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL_M clock frequency	f_{SCL}	—	0	—	400	kHz
SCL_M hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL_M "L" level time	t_{LOW}	—	1.3	—	—	µs
SCL_M "H" level time	t_{HIGH}	—	0.6	—	—	µs
SCL_M setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA_M hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA_M setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA_M setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs



● Electrical Characteristics of Successive Approximation Type A/D Converter

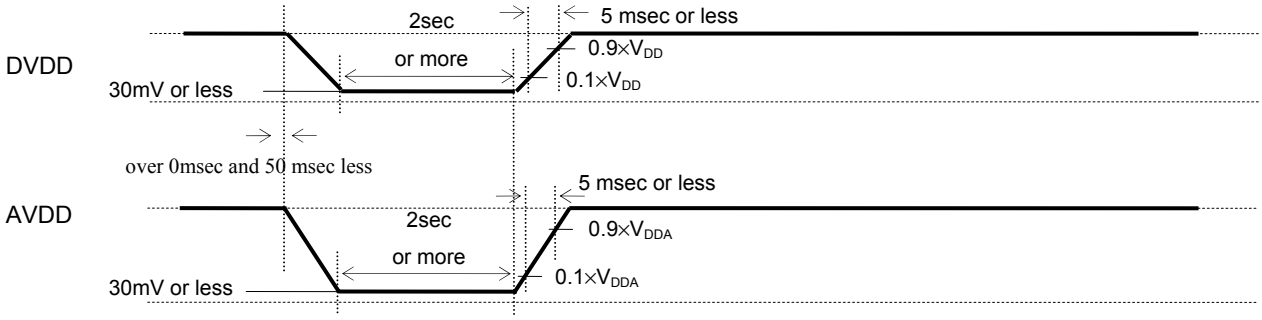
(Unless otherwise specified, DVDD = AVDD = 2.5 to 3.6, DGND = AGND = 0V, Ta = -30 to +85°C)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	-	-	-	12	bit
Integral non-linearity error margin	INL	2.7V≤AVDD≤3.6V	-4	-	+4	LSB
		2.5V≤AVDD≤2.7V	-6	-	+6	
Differential non-linearity error margin	DNL	2.7V≤AVDD≤3.6V	-3	-	+3	
		2.5V≤AVDD≤2.7V	-5	-	+5	
Zero-scale error	V_{OFF}	-	-6	-	+6	
Full-scale error	FSE	-	-6	-	+6	
Reference voltage	AVDD	-	2.5	-	V_{DDA}	V
Conversion time	t_{CONV}	At high-speed operation	-	112	-	φ/CH

φ: Cycle of high-speed clock

■ Power-On / Power-Off Procedures

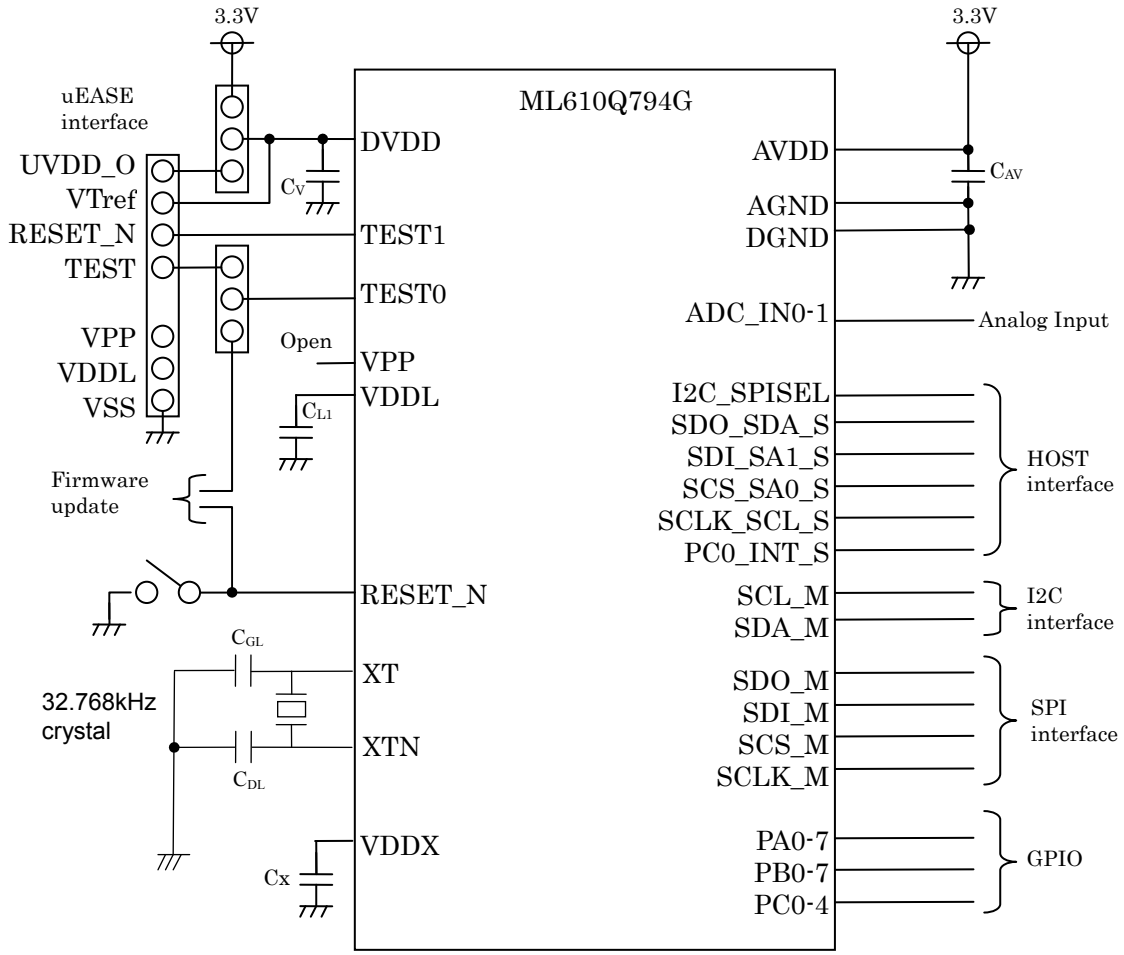
The power-on and power-off procedures of DVDD and AVDD need to meet with the following timing restrictions.



■ Application Circuit Example

(1) Overview

The below diagram shows the example of application circuit of the ML610Q794G, and the table shows the recommended value of capacitors and resisters in this circuit.



Recommended Values of Circuit Constants

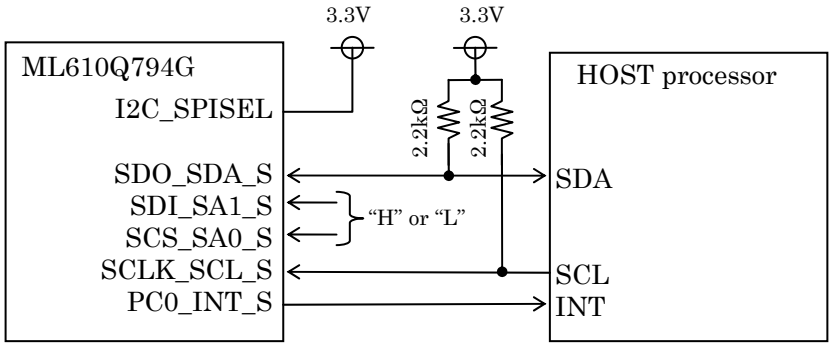
Symbol	Recommended Value
C_V	1µF
C_{AV}	1µF
C_{L1}	2.2µF
C_X	0.1µF
C_{GL}	3 ~ 18pF
C_{DL}	3 ~ 18pF

(2)Host Interface

The HOST interface can be selected from I2C or SPI by using I2C_SPISEL pin. Connection example for each usage is shown below.

◆ I2C Slave Interface

When applying “H” level to I2C_SPISEL pin, I2C is selected. The I2C slave address can be set by using the SDI_SA1_S pin and the SCS_SA0_S pin. The table shows a matrix of applied level on each pin and the slave address.

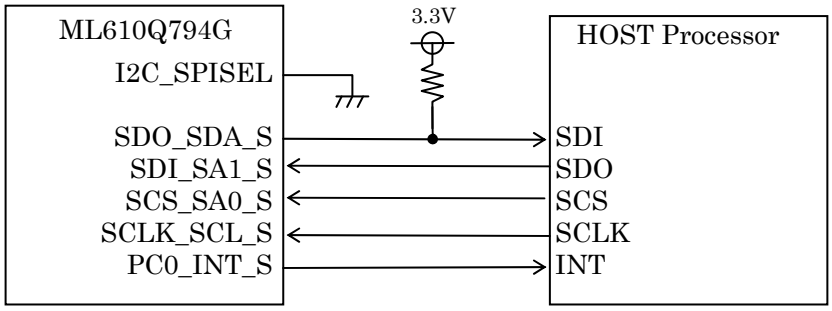


I2C Slave Address

SDI_SA1_S	SCS_SA0_S	Write Address	Read Address
"H"	"H"	8'b1110_1110	8'b1110_1111
"H"	"L"	8'b1010_1110	8'b1010_1111
"L"	"H"	8'b0110_1110	8'b0110_1111
"L"	"L"	8'b0010_1110	8'b0010_1111

◆ SPI Slave Interface

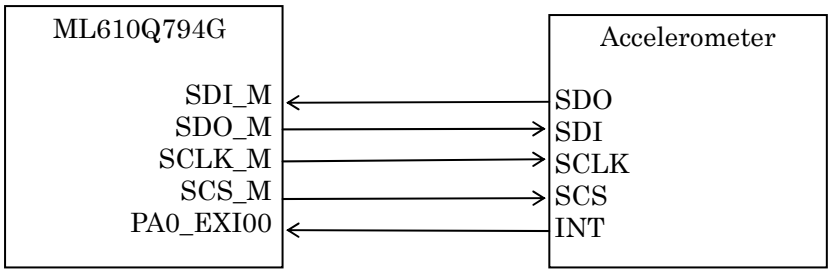
When applying "L" level to I2C_SPISEL pin, SPI is selected.



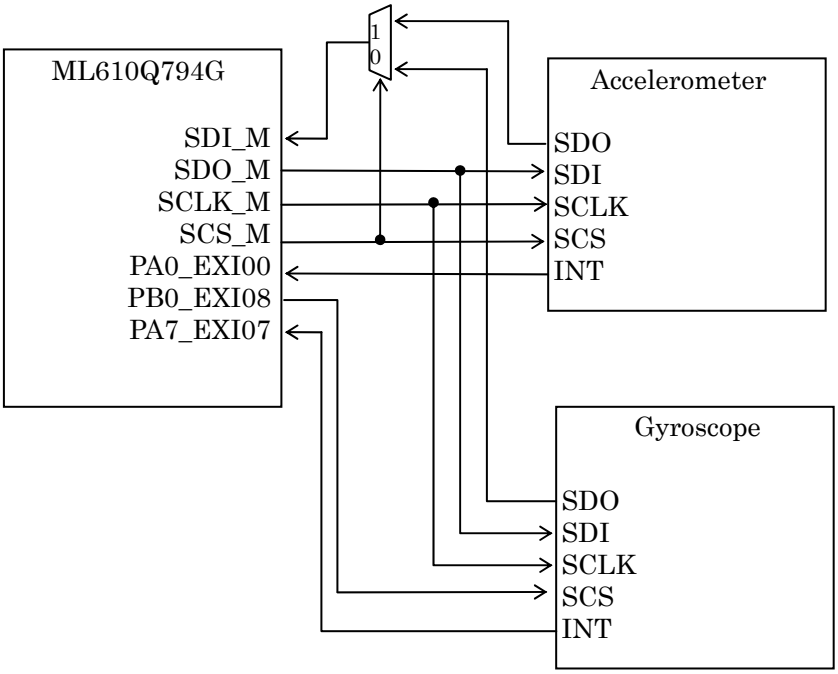
(3)Sensor Interface

The ML610Q794G supports 1channel of SPI master interface and 1 channel of I2C master interface for sensor control.
The example of connecting each sensor is shown below.

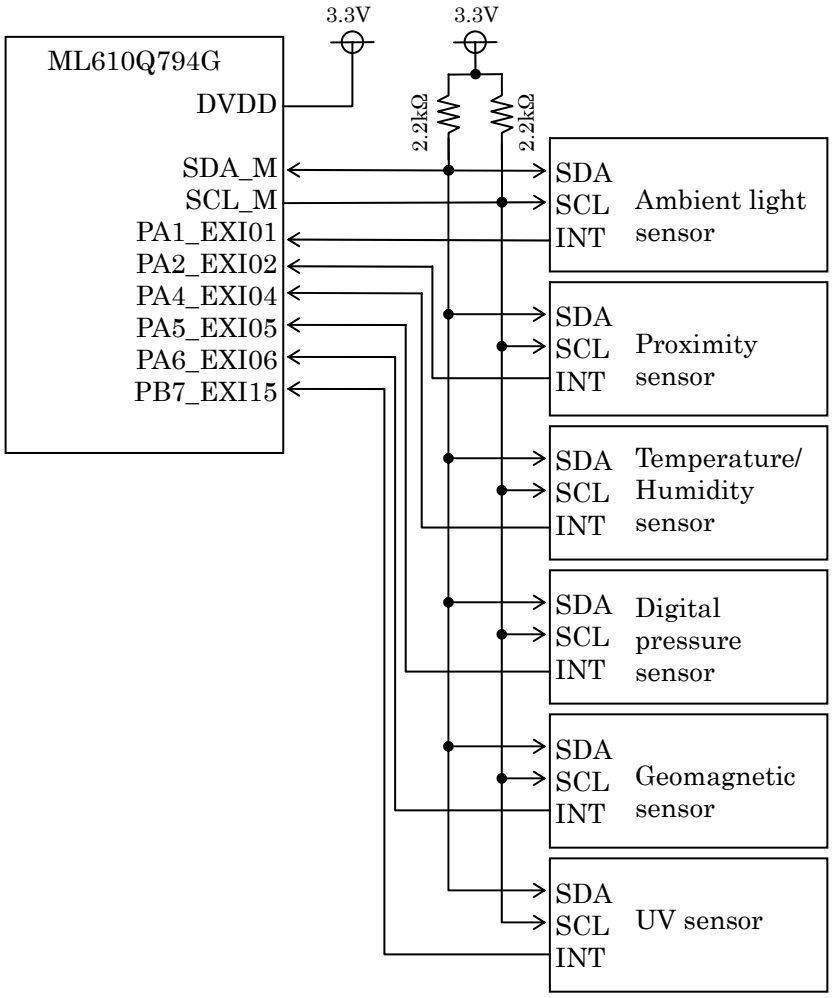
◆ SPI Master Interface (single sensor)



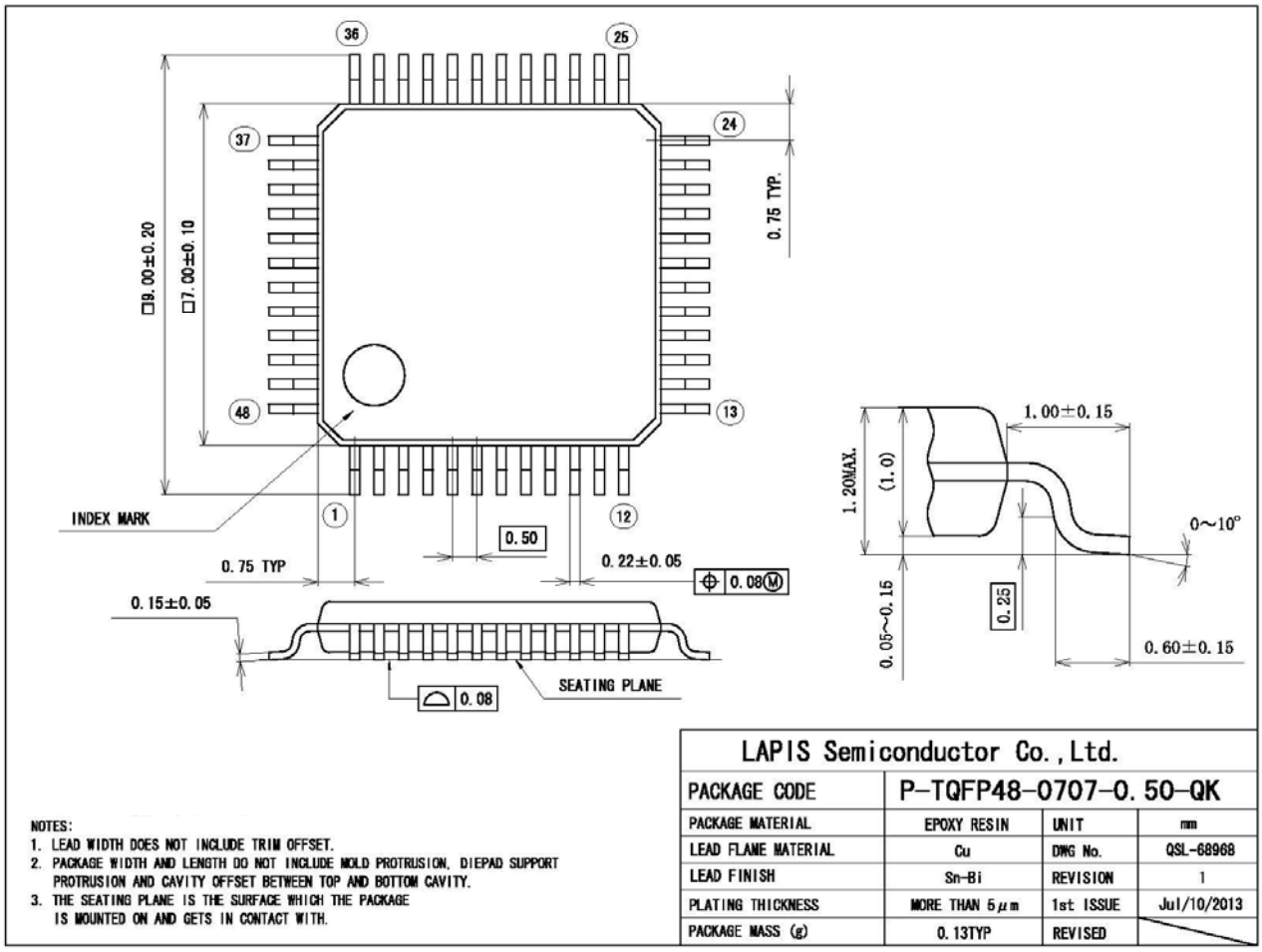
◆ SPI Master Interface (multi sensors)



◆ I2C Interface



■ Package Dimensions



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

■ Revision History

Document No.	Issue Date	Page		Description
		Previous Edition	New Edition	
FEDL610Q794-01	2014.3.10	—	—	First edition issued
FEDL610Q794-02	2015.1.29	—	—	Minor error correction
		5	5	List of Pins error correction Secondary function of PC2_RXD0 is SIO RXD Secondary function of PC3_TXD0 is SIO TXD Secondary function of PB3_EXI11 add
		10	10	Operation Status Register initial value change
		13	13	DC Characteristics(2/2) Output voltage 1(SDA_M,SCL_M) VOL1 condition and spec change
		13	13	DC Characteristics(2/2) VOL2 test condition error correction
		13	13	DC Characteristics(2/2) IIH1 min spec and IIL2 max spec change

NOTES

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