

MJD243 (NPN), MJD253 (PNP)

Preferred Device

Complementary Silicon Plastic Power Transistor DPAK-3 for Surface Mount Applications

Designed for low voltage, low-power, high-gain audio amplifier applications.

Features

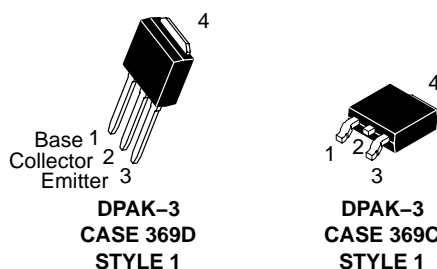
- Collector-Emitter Sustaining Voltage –
 $V_{CEO(sus)} = 100 \text{ Vdc (Min) @ } I_C$
 $= 10 \text{ mAdc}$
- High DC Current Gain –
 $h_{FE} = 40 \text{ (Min) @ } I_C$
 $= 200 \text{ mAdc}$
 $= 15 \text{ (Min) @ } I_C = 1.0 \text{ Adc}$
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“-1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C$
 $= 500 \text{ mAdc}$
 $= 0.6 \text{ Vdc (Max) @ } I_C = 1.0 \text{ Adc}$
- High Current-Gain – Bandwidth Product –
 $f_T = 40 \text{ MHz (Min) @ } I_C$
 $= 100 \text{ mAdc}$
- Annular Construction for Low Leakage –
 $I_{CBO} = 100 \text{ nAdc @ Rated } V_{CB}$
- Epoxy Meets UL 94, V-0 @ 0.125 in.
- ESD Ratings: Human Body Model, 3B > 8000 V
Machine Model, C > 400 V
- Pb-Free Package is Available



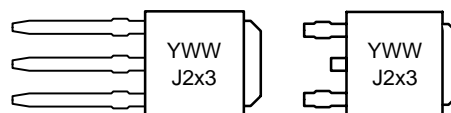
ON Semiconductor®

<http://onsemi.com>

4.0 A, 100 V, 12.5 W POWER TRANSISTOR



MARKING DIAGRAMS



Y = Year
WW = Work Week
J2x3 = Device Code
x = 4 or 5

ORDERING INFORMATION

Device	Package	Shipping†
MJD243	DPAK-3	75 Units/Rail
MJD243T4	DPAK-3	2500/Tape & Reel
MJD243T4G	DPAK-3 (Pb-Free)	2500/Tape & Reel
MJD253-1	DPAK-3	75 Units/Rail
MJD253T4	DPAK-3	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	100	Vdc
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Emitter–Base Voltage	V_{EB}	7.0	Vdc
Collector Current–Continuous –Peak	I_C	4.0 8.0	Adc
Base Current	I_B	1.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	12.5 0.1	W W/ $^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) Derate above 25°C	P_D	1.4 0.011	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted on minimum pad sizes recommended.

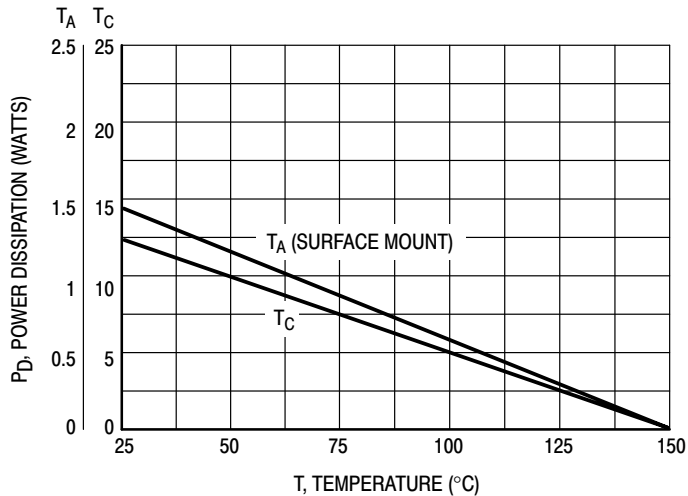


Figure 1. Power Derating

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	10	$^{\circ}\text{C/W}$
Junction-to-Ambient (Note 2)	$R_{\theta JA}$	89.3	

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Note 3) ($I_C = 10 \text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	100	–	Vdc
Collector Cutoff Current ($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$) ($V_{CB} = 100 \text{ Vdc}$, $I_E = 0$, $T_J = 125^{\circ}\text{C}$)	I_{CBO}	–	100	nAdc μAdc
Emitter Cutoff Current ($V_{BE} = 7.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	100	nAdc
DC Current Gain (Note 3) ($I_C = 200 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$) ($I_C = 1.0 \text{ Adc}$, $V_{CE} = 1.0 \text{ Vdc}$)	h_{FE}	40 15	180 –	–
Collector-Emitter Saturation Voltage (Note 3) ($I_C = 500 \text{ mAdc}$, $I_B = 50 \text{ mAdc}$) ($I_C = 1.0 \text{ Adc}$, $I_B = 100 \text{ mAdc}$)	$V_{CE(sat)}$	– –	0.3 0.6	Vdc
Base-Emitter Saturation Voltage (Note 3) ($I_C = 2.0 \text{ Adc}$, $I_B = 200 \text{ mAdc}$)	$V_{BE(sat)}$	–	1.8	Vdc
Base-Emitter On Voltage (Note 3) ($I_C = 500 \text{ mAdc}$, $V_{CE} = 1.0 \text{ Vdc}$)	$V_{BE(on)}$	–	1.5	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain – Bandwidth Product (Note 4) ($I_C = 100 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 10 \text{ MHz}$)	f_T	40	–	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	–	50	pF

2. When surface mounted on minimum pad sizes recommended.

3. Pulse Test: Pulse Width = 300 μs , Duty Cycle $\approx 2\%$.

4. $f_T = |h_{FE}| \cdot f_{test}$.

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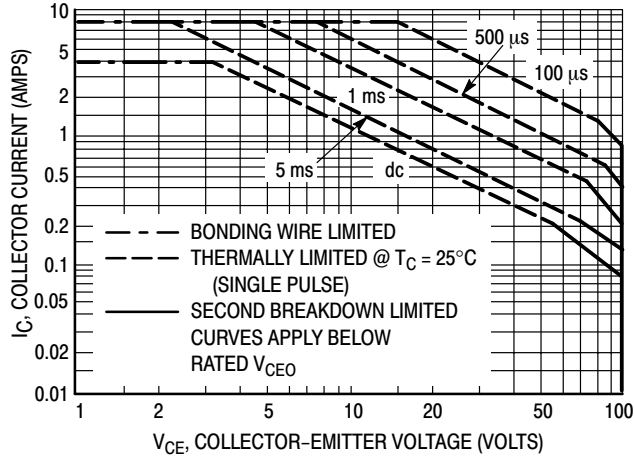


Figure 2. Active Region Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

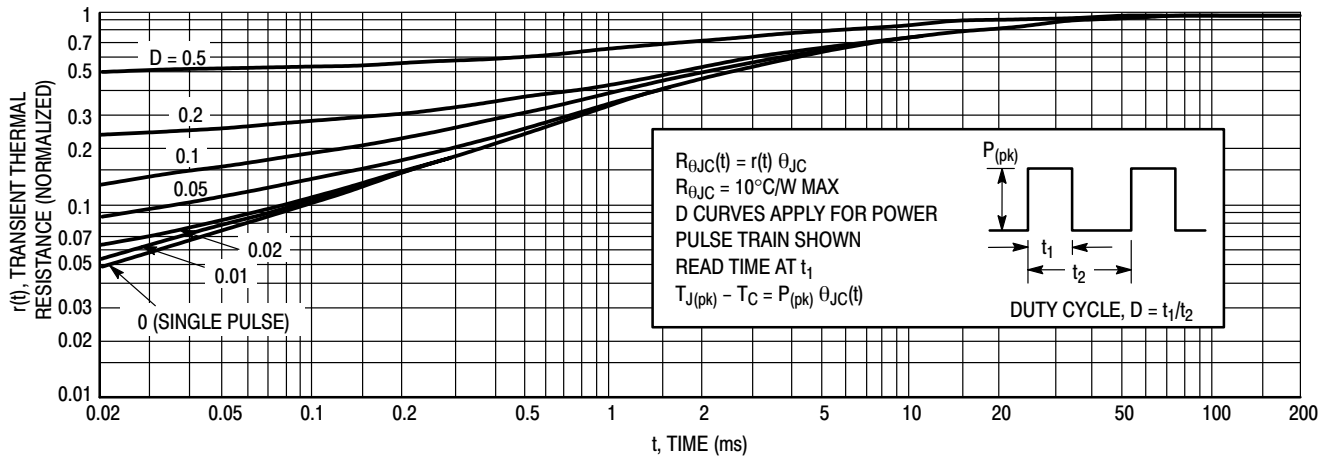


Figure 3. Thermal Response

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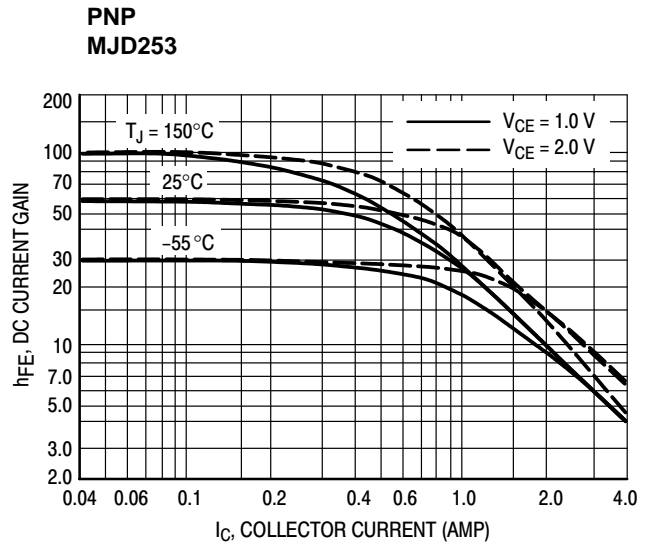
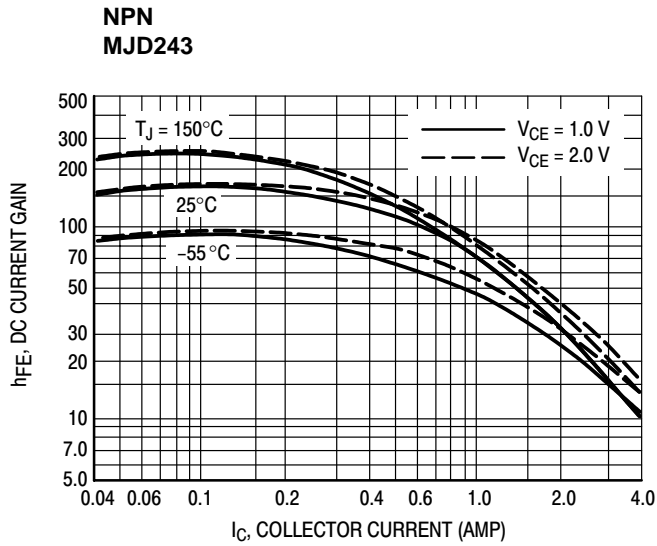


Figure 4. DC Current Gain

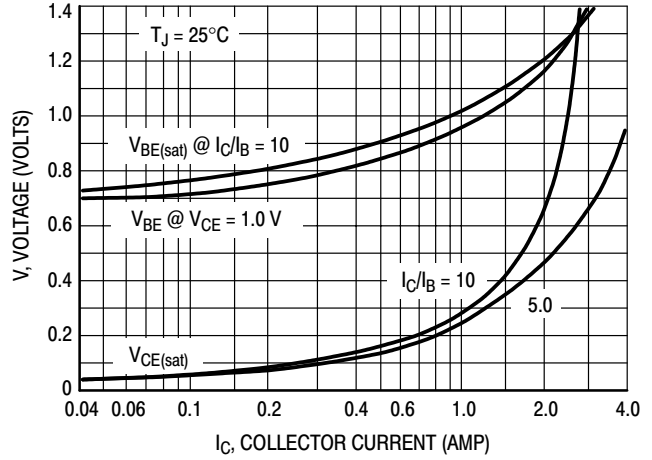
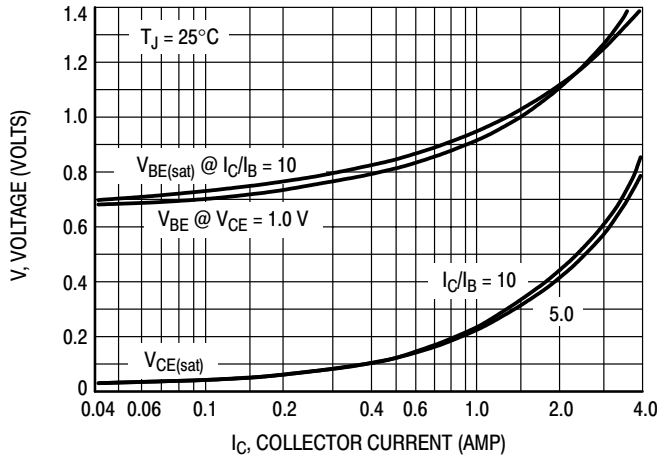


Figure 5. "On" Voltages

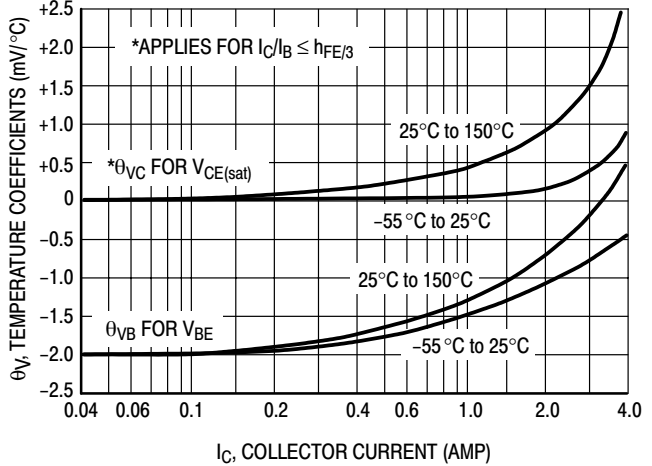
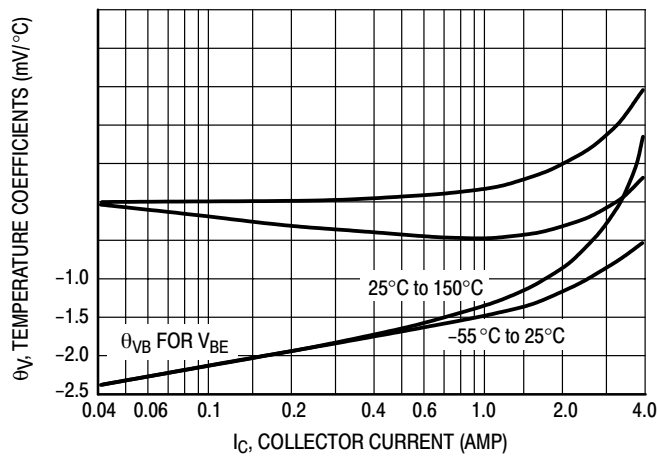


Figure 6. Temperature Coefficients

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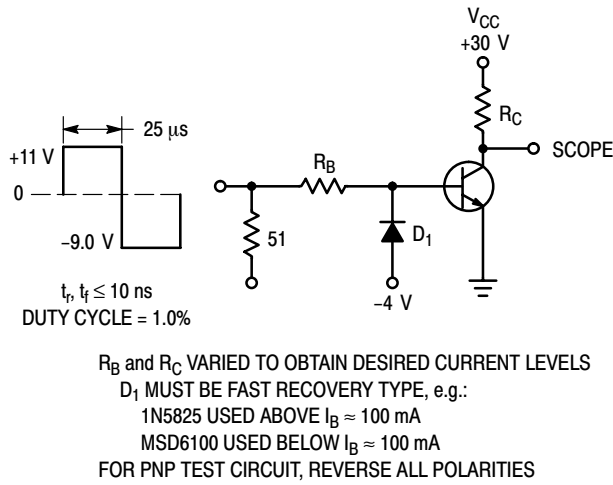


Figure 7. Switching Time Test Circuit

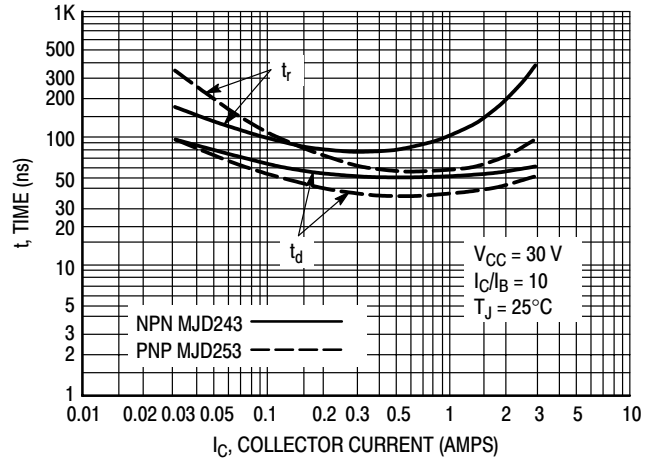


Figure 8. Turn-On Time

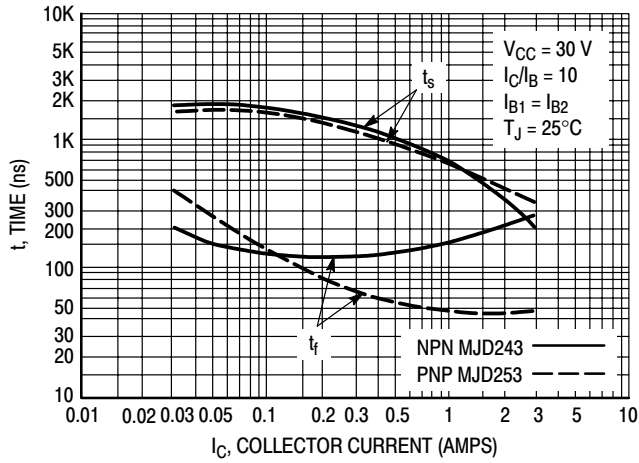


Figure 9. Turn-Off Time

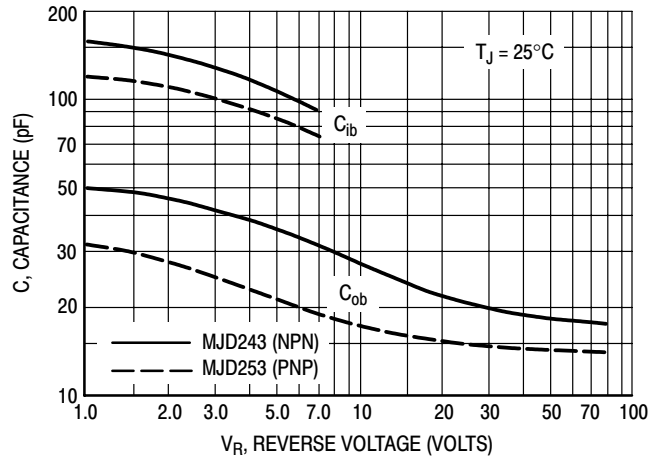


Figure 10. Capacitance

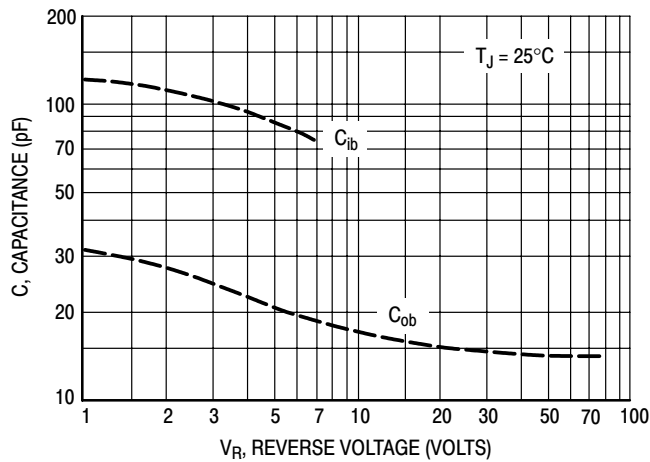
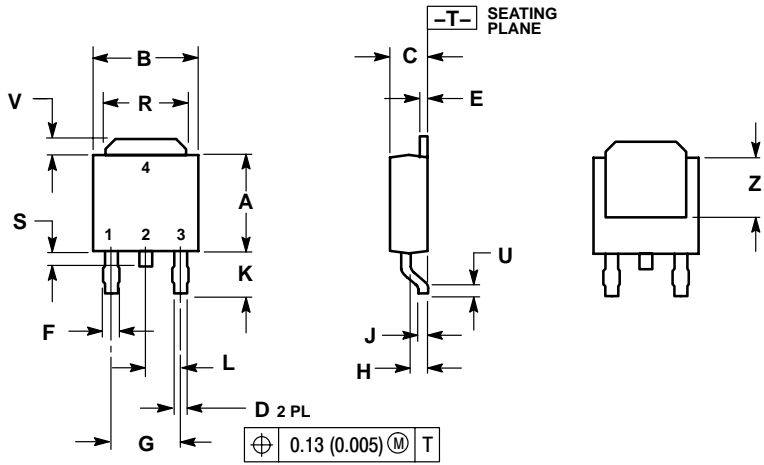


Figure 11. Capacitance

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PACKAGE DIMENSIONS

DPAK-3
CASE 369C-01
ISSUE O

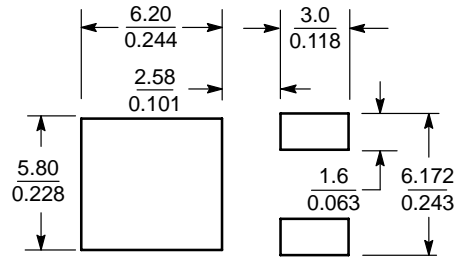


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}} \right)$

DPAK-3

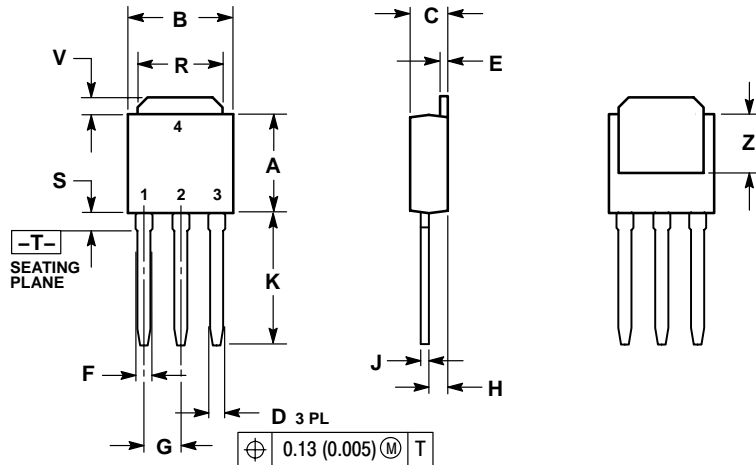
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MJD243 (NPN), MJD253 (PNP)

PACKAGE DIMENSIONS

DPAK-3 (SINGLE GAUGE)

CASE 369D-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 1:

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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