

8/16-bit Data Bus
Static RAM Card

Connector Type

Two-piece 68-pin

- MF365A-LZCATXX**
- MF3129-LZCATXX**
- MF3257-LZCATXX**
- MF3513-LZCATXX**
- MF31M1-LZCATXX**
- MF32M1-LZCATXX**
- MF34M1-LZCATXX**

1. DESCRIPTION

Mitsubishi's Static RAM cards provide large memory capacities on a device approximately the size of a credit card (85.6mm×54mm×3.3mm). The cards use a 8/16 bit data-bus. The devices use a replaceable lithium battery to maintain data. Available in 64K byte-4M byte capacities, Mitsubishi's Static RAM cards are available with a 68-pin, two-piece connector.

2. FEATURES

- Uses TSOP (Thin Small Outline Package) to achieve very high memory density coupled with high reliability, without enlarging card size
- Electrostatic discharge protection to 15kV
- Buffered interface
- Write protect switch
- Attribute memory
- 68pin

3. APPLICATIONS

- Office automation
- Computers
- Telecommunications
- Data Communication
- Industrial
- Consumer

4. PRODUCT LIST

Type name	Item	Memory capacity	Data Bus width(bits)	Attribute memory	Auxiliary battery
MF365A-LZCATXX		64KB	8/16	8KB E ² PROM	NO
MF3129-LZCATXX		128KB			
MF3257-LZCATXX		256KB			
MF3513-LZCATXX		512KB			
MF31M1-LZCATXX		1MB			
MF32M1-LZCATXX		2MB			
MF34M1-LZCATXX		4MB			



5. SUMMARY

MF3XXX-LZCATXX series is the Static RAM cards which has 8/16 bit changeable data-bus width. The card has a replaceable lithium battery to maintain data in memory. When the card is not use or the supply voltage drops, the battery will automatically maintain data in memory.

6. FUNCTIONAL DESCRIPTION

The function of the card is determined by the combination of the following five control signals, REG#, CE1#, CE2#, OE#, WE#; active low signals. (Please refer to section 10 FUNCTION TABLE on page 5)

(1)COMMON MEMORY FUNCTION

When REG# signal is high level, the common memory area is selected.

(a)READ MODE

To read, WE# is set high level and CE1# or CE2# is set low level and the memory address is applied at inputs A0-A21(4MB). Setting OE# low level executes the reading with output at data-bus. It is available to make the following functions according to the combination of CE1# and CE2#.

When CE1# is set low level and CE2# is set high level, the card operates as an 8 bit data-bus width card. The data can be dealt with lower data-bus(D0-D7).

When both CE1# and CE2# are set low level, the card operates as a 16 bit data-bus width card.

At this mode LSB of address-bus (A0) is ignored.

In addition odd byte can be accessed through upper data-bus(D8-D15) when CE1# is set high level and CE2# is set low level. This mode is useful when handling only odd bytes in the 16 bit data-bus interface system (A0 is ignored).

When both CE1# and CE2# are set high level, the card becomes a standby mode where the card consumes low power and the data-bus is placed in high impedance state (above functions of CE1# and CE2# are the same as in the following modes).

When both OE# and WE# are set high level, the card becomes a output disable mode and the data-bus is placed in high impedance state.

(b)WRITE MODE

To write, the memory address is first applied at inputs A0-A21(4MB) and the data is applied at output pins. Setting CE1# or CE2# low level, WE# low level and OE# high level executes the writing.

(2)ATTRIBUTE MEMORY FUNCTION

When REG# is set low level, the attribute memory area is selected. MF3XXX-LZCATXX series accommodates an attribute memory of 8KB E²PROM on even addresses.

(a)READ MODE

First set CE1# and CE2# low level or high level and select residing address (even address). Data can be read by setting OE# low level and WE# high level.

(b)WRITE MODE

Writing can be done either by byte-mode or page-mode. The page-mode write is the function to be able to write data of 32 bytes in a single write cycle. The page address is set by A6 to A13 (Please note that attribute memory exists in even bytes only). To write, set OE# high level and WE# low level. Data will be latched at the rising edge of WE#. After the first load unless WE# changes from high level to low level within 30 μ s, the automatic erase/program starts and completes in 10ms or before. Page data can be latched if WE# transits from high level to low level before the 30 μ s. Page-mode write also executes erase/program operation within 10ms.

The page address must be maintained during the page data loading.

7. WRITE PROTECT MODE

When the write protect switch is switched on, this card goes into a write protect mode that can read but not write data. In this mode, WP pin becomes "H" level.

At the shipment the write protect switch is switched off (Normal mode : The card can be written ; WP pin indicates "L" level).

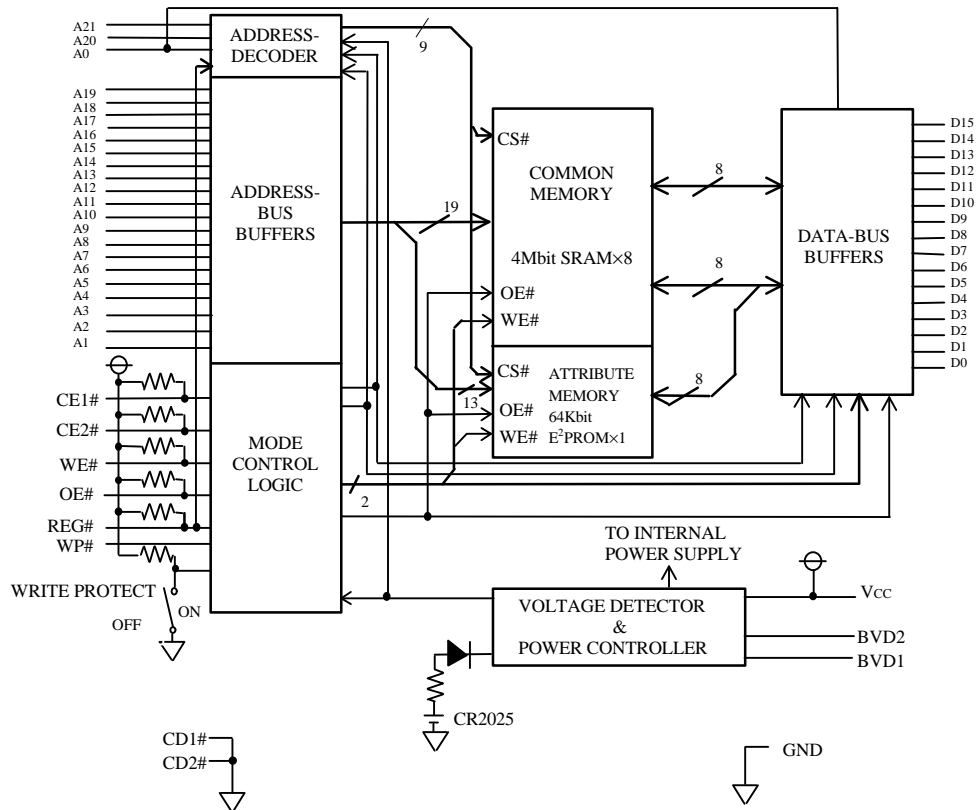


8. PIN ASSIGNMENTS

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D3	} Data I/O	36	CD1#	Card detect 1
3	D4		37	D11	} Data I/O
4	D5		38	D12	
5	D6		39	D13	
6	D7		40	D14	
7	CE1#	Card enable 1	41	D15	
8	A10	Address input	42	CE2#	
9	OE#	Output enable	43	NC	} No connection
10	A11	} Address input	44	NC	
11	A9		45	NC	
12	A8		46	A17	} Address input
13	A13		47	A18	
14	A14		48	A19	
15	WE#	Write enable	49	A20	
16	NC	No connection	50	A21	
17	VCC	Power supply voltage	51	VCC	Power supply voltage
18	NC	No connection	52	NC	} No connection
19	A16	A16 (NC for 64KB type)	53	NC	
20	A15	} Address input	54	NC	
21	A12		55	NC	
22	A7		56	NC	
23	A6		57	NC	
24	A5		58	NC	
25	A4		59	NC	
26	A3		60	NC	
27	A2		61	REG#	
28	A1		62	BVD2	Battery voltage detect 2
29	A0		63	BVD1	Battery voltage detect 1
30	D0	} Data I/O	64	D8	} Data I/O
31	D1		65	D9	
32	D2		66	D10	
33	WP	Write protect	67	CD2#	
34	GND	Ground	68	GND	Ground



9. BLOCK DIAGRAM (4MB) (MF34M1-LZCATXX)



10. FUNCTION TABLE

Mode	REG#	CE1#	CE2#	OE#	WE#	A0	I/O (D15~D8)	I/O (D7~D0)	Icc
Standby	X	H	H	X	X	X	High-impedance	High-impedance	standby
Read A (16bit) common	H	L	L	L	H	X	Odd Byte Data out	Even Byte Data out	Active
Write A (16bit) common	H	L	L	H	L	X	Odd Byte Data in	Even Byte Data in	Active
Read B (8bit) common	H	L	H	L	H	L	High-impedance	Even Byte Data out	Active
	H	L	H	L	H	H	High-impedance	Odd Byte Data out	Active
Write B (8bit) common	H	L	H	H	L	L	High-impedance	Even Byte Data in	Active
	H	L	H	H	L	H	High-impedance	Odd Byte Data in	Active
Read C (8bit) common	H	H	L	L	H	X	Odd Byte Data out	High-impedance	Active
Write C (8bit) common	H	H	L	H	L	X	Odd Byte Data in	High-impedance	Active
Output disable	X	X	X	H	H	X	High-impedance	High-impedance	Active
Read A (16bit) attribute	L	L	L	L	H	X	Data out (unknown)	Even Byte Data out	Active
Read B (8bit) attribute	L	L	H	L	H	L	High-impedance	Even Byte Data out	Active
	L	L	H	L	H	H	High-impedance	Data out (unknown)	Active
Read C (8bit) attribute	L	H	L	L	H	X	Data out (unknown)	High-impedance	Active
Write A (16bit) attribute	L	L	L	H	L	X	don't care	Even Byte Data in	Active
Write B (8bit) attribute	L	L	H	H	L	L	don't care	Even Byte Data in	Active
	L	L	H	H	L	H	don't care	don't care	Active
Write C (8bit) attribute	L	H	L	H	L	X	don't care	don't care	Active

Note 1 : H=VIH, L=VIL, X=VIH or VIL

11. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	-0.3~6.0	V
Vi	Input voltage		-0.3~VCC+0.3	V
Vo	Output voltage		0~VCC	V
Topr1	Operating temperature 1	Read, Write Operation	0~60	°C
Topr2	Operating temperature 2	Data retention	0~60	°C
Tstg	Storage temperature	Excludes data retention	-20~70	°C

12. RECOMMENDED OPERATING CONDITIONS (Ta=0~55°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vcc	Vcc Supply voltage	4.75	5.0	5.25	V
GND	System ground		0		V
VIH	High input voltage	2.4		VCC	V
VIL	Low input voltage	0		0.8	V



STATIC RAM CARDS

13. ELECTRICAL CHARACTERISTICS (Ta=0~55°C, Vcc=5V±5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	High output voltage	IOH= -1.0mA	2.4			V
VOL	Low output voltage	IOL=2mA			0.4	V
IiH	High input current	Vi=Vcc V			10	µA
IiL	Low input current	Vi=0V CE1#, CE2#, WE#, OE#, REG# Other inputs	-10		-70	µA
					-10	
IOZH	High output current in off state	CE1#=CE2#=VIH or OE#=VIH WE#=VIH, Vo=Vcc			10	µA
IOZL	Low output current in off state	CE1#=CE2#=VIH or OE#=VIH WE#=VIH, Vo=0V			-10	µA
Icc 1 • 1	Active supply current 1	CE1#=CE2#=VIL, Other inputs =VIH or VIL, Outputs=open	64KB~512KB		170	mA
			1MB~4MB		230	
Icc 1 • 2	Active supply current 2	CE1#=CE2# ≤ 0.2V, Other inputs ≤ 0.2V or ≥ Vcc-0.2V, Outputs=open	64KB~512KB		160	mA
			1MB~4MB		220	
Icc 2 • 1	Standby supply current 1	CE1#=CE2#=VIH Other inputs=VIH or VIL	64KB~4MB		10	mA
Icc 2 • 2	Standby supply current 2	CE1#=CE2# ≥ Vcc-0.2V Other inputs ≤ 0.2V or ≥ Vcc-0.2V	64KB~512KB		0.45	mA
			1MB~4MB		0.65	
VBDET1	Battery detect reference voltage 1	Vcc=5V, Ta=25°C	2.27	2.37	2.47	V
VBDET2	Battery detect reference voltage 2	Vcc=5V, Ta=25°C	2.55	2.65	2.75	V

Note 2 : Currents flowing into the card are taken as positive (unsigned).

3 : Typical values are measured at Vcc=5V, Ta=25°C.

14. CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
CI	Input capacitance	Vi=GND, vi=25mVrms f=1MHz, Ta=25°C			30	pF
CO	Output Capacitance	Vo=GND, vo=25mVrms f=1MHz, Ta=25°C			20	pF

Note 4 : These parameters are not 100% tested.



15. SWITCHING CHARACTERISTICS

Read Cycle ($T_a=0\sim 55^\circ\text{C}$, $V_{CC}=5V\pm 5\%$, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tcR	Read cycle time	150		ns
ta(A)	Address access time		150	ns
ta(CE)	Card enable access time		150	ns
ta(OE)	Output enable access time		75	ns
t _{dis} (CE)	Output disable time (from CE#)		75	ns
t _{dis} (OE)	Output disable time (from OE#)		75	ns
t _{en} (CE)	Output enable time (from CE#)	5		ns
t _{en} (OE)	Output enable time (from OE#)	5		ns
tv(A)	Data valid time (after address change)	0		ns

16. TIMING REQUIREMENTS

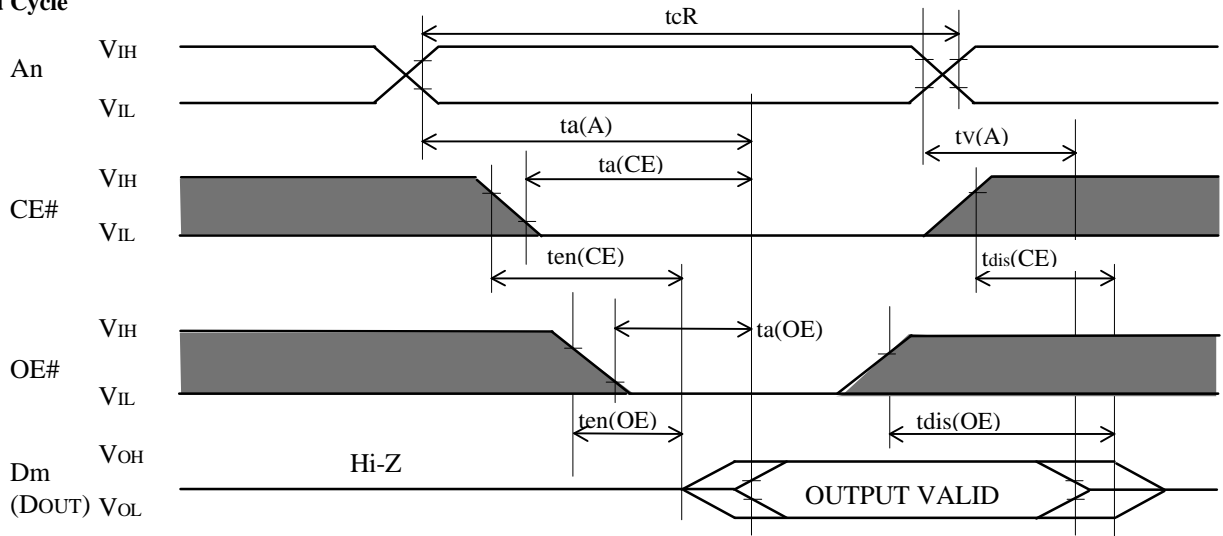
Write Cycle ($T_a=0\sim 55^\circ\text{C}$, $V_{CC}=5V\pm 5\%$, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tcW	Write cycle time	150		ns
tw(WE)	Write pulse width	80		ns
tsu(A)	Address set up time	20		ns
tsu(A-WEH)	Address set up time with respect to WE# high	100		ns
tsu(CE-WEH)	Card enable set up time with respect to WE# high	100		ns
t(D-WEH)	Data set up time with respect to WE# high	50		ns
th(D)	Data hold time	20		ns
trec(WE)	Write recovery time	20		ns
t _{dis} (WE)	Output disable time (from WE#)		75	ns
t _{dis} (OE)	Output disable time (from OE#)		75	ns
t _{en} (WE)	Output enable time (from WE#)	5		ns
t _{en} (OE)	Output enable time (from OE#)	5		ns
tsu(OE-WE)	OE# set up time with respect to WE# low	10		ns
th(OE-WE)	OE# hold time with respect to WE# high	10		ns



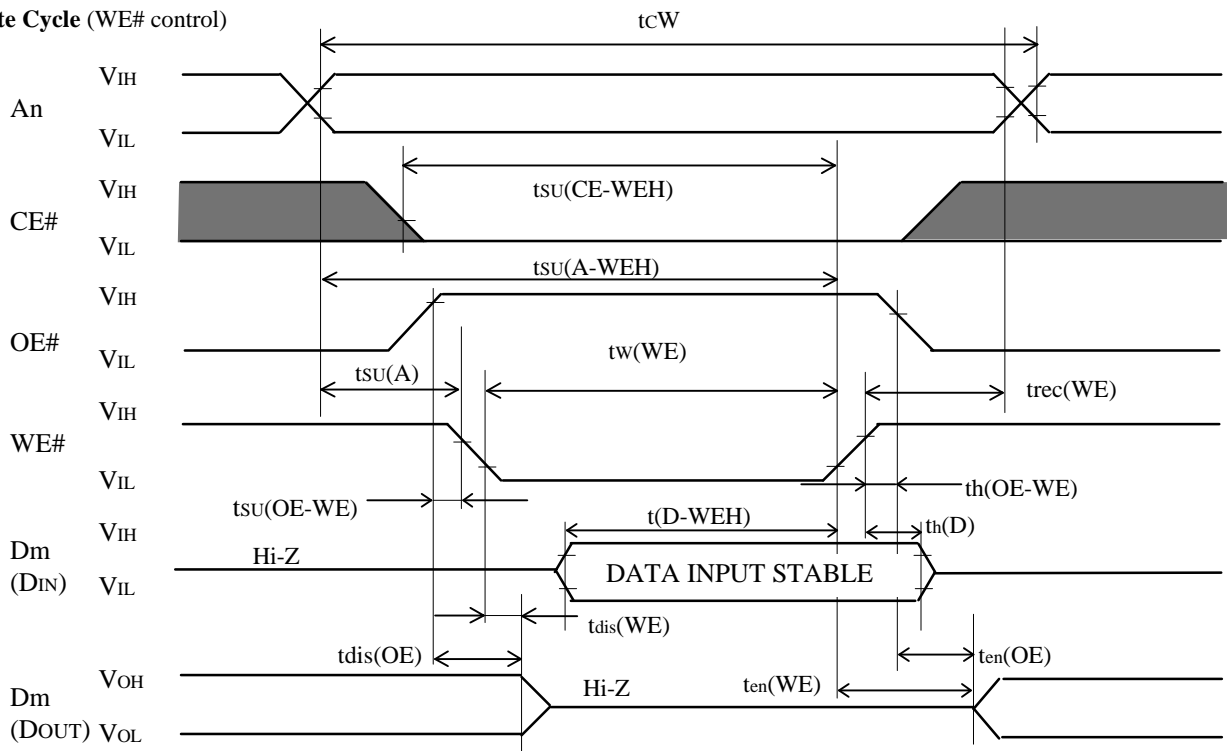
TIMING DIAGRAM

Read Cycle



WE#="H" level
REG#="H" level

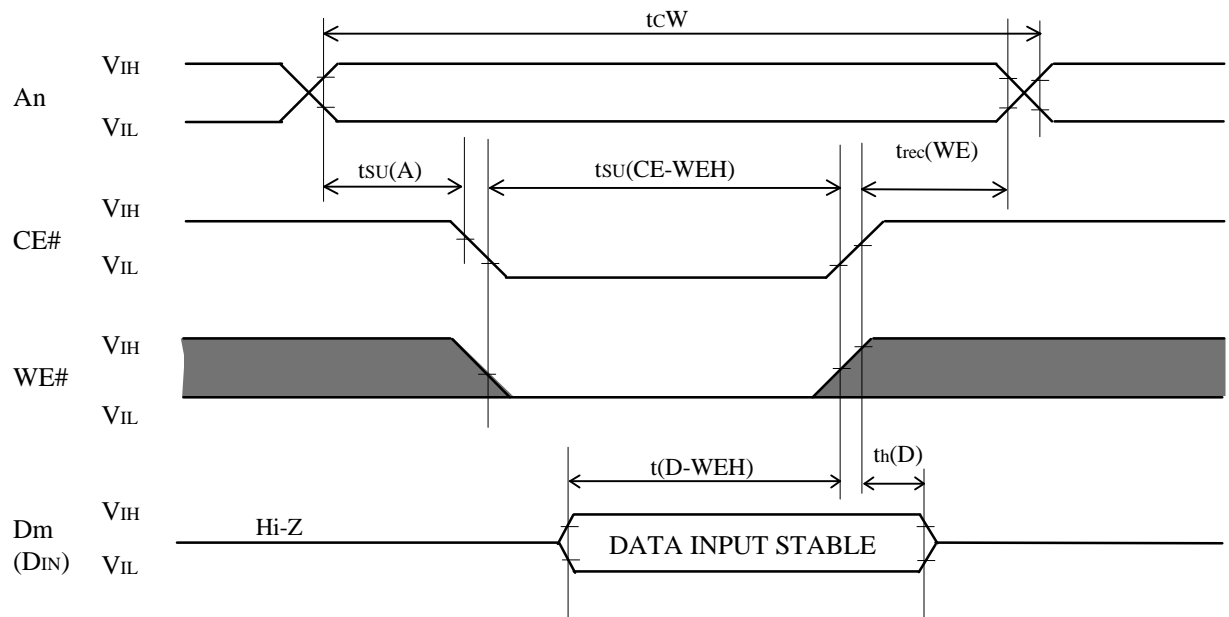
Write Cycle (WE# control)



REG#="H" level



Write Cycle (CE# control)



OE#="H" level
REG#="H" level

17. SWITCHING CHARACTERISTICS (Attribute)

Read Cycle (Ta=0~55°C, Vcc=5V±5%, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tcRR	Read cycle time	300		ns
ta(A)R	Address access time		300	ns
ta(CE)R	Card enable access time		300	ns
ta(OE)R	Output enable access time		150	ns
tdis(CE)R	Output disable time (from CE#)		100	ns
tdis(OE)R	Output disable time (from OE#)		100	ns
ten(CE)R	Output enable time (from CE#)	5		ns
ten(OE)R	Output enable time (from OE#)	5		ns
tV(A)R	Data valid time after address change	0		ns

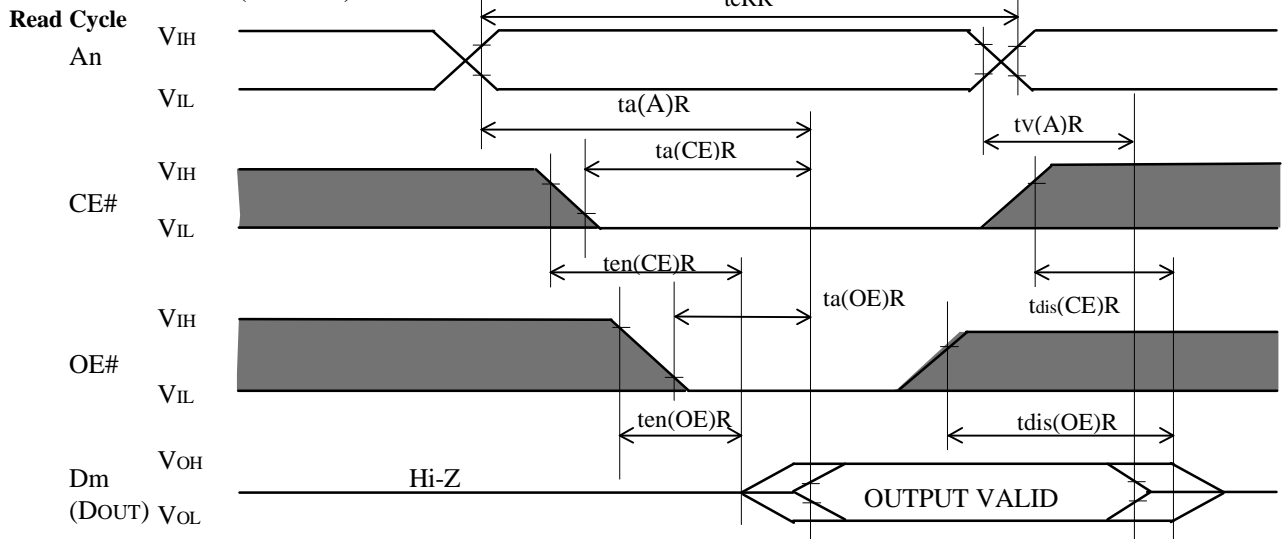


18. TIMING REQUIREMENTS (Attribute)

Write Cycle ($T_a=0\sim 55^\circ\text{C}$, $V_{cc}=5\text{V}\pm 5\%$, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tsu(A)R	Address setup time	30		ns
tsu(CE)R	CE# setup time	40		ns
th(CE)R	CE# hold time	30		ns
t(D-WEH)R	Data setup time	120		ns
th(D)R	Data hold time	40		ns
tsu(OE-WE)R	OE# setup time	30		ns
th(OE-WE)R	OE# hold time	40		ns
tw(WE)R	Write pulse width	170		ns
tDLR	Data latch time	120		ns
tBLCR	Byte load cycle time	0.3	30	μs
tcWR	Write cycle time	10		ms
ten(OE)R	Output enable time from OE#	5		ns
trec(WE)R	Write recovery time	30		ns

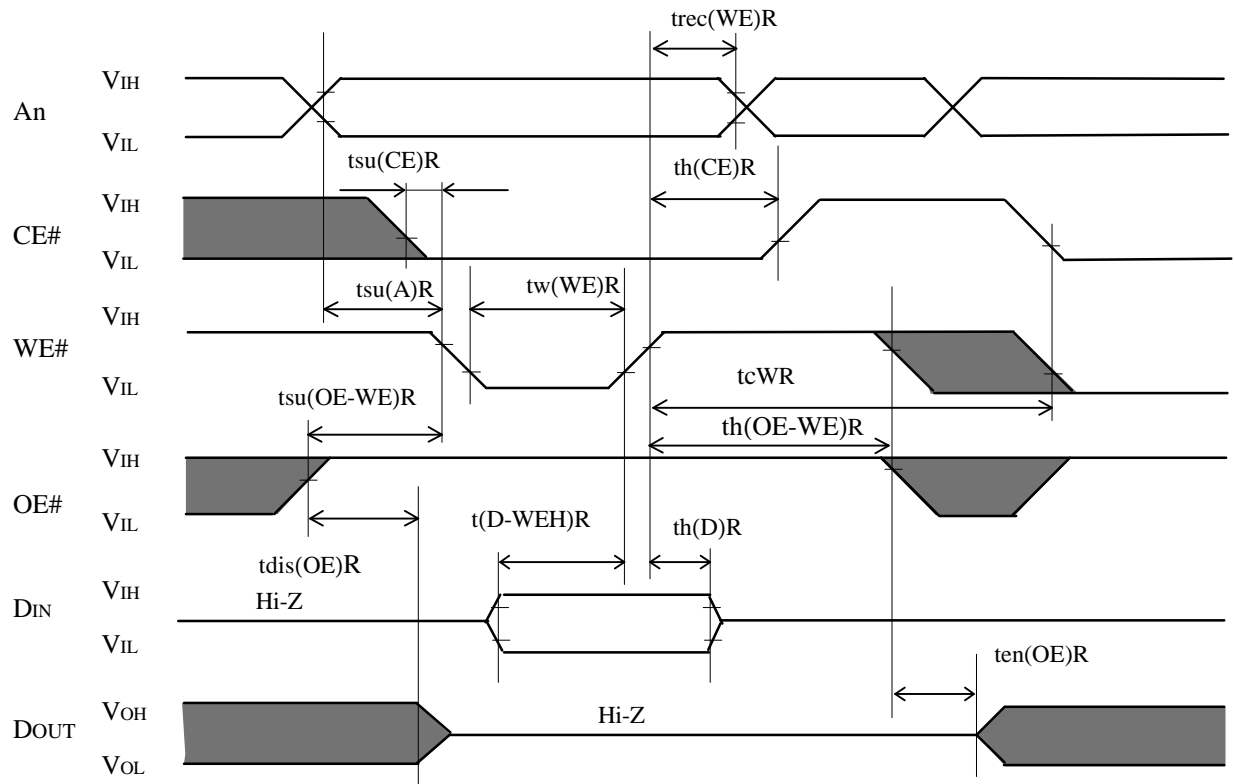
TIMING DIAGRAM (Attribute)



WE#="H" level
 REG#="L" level



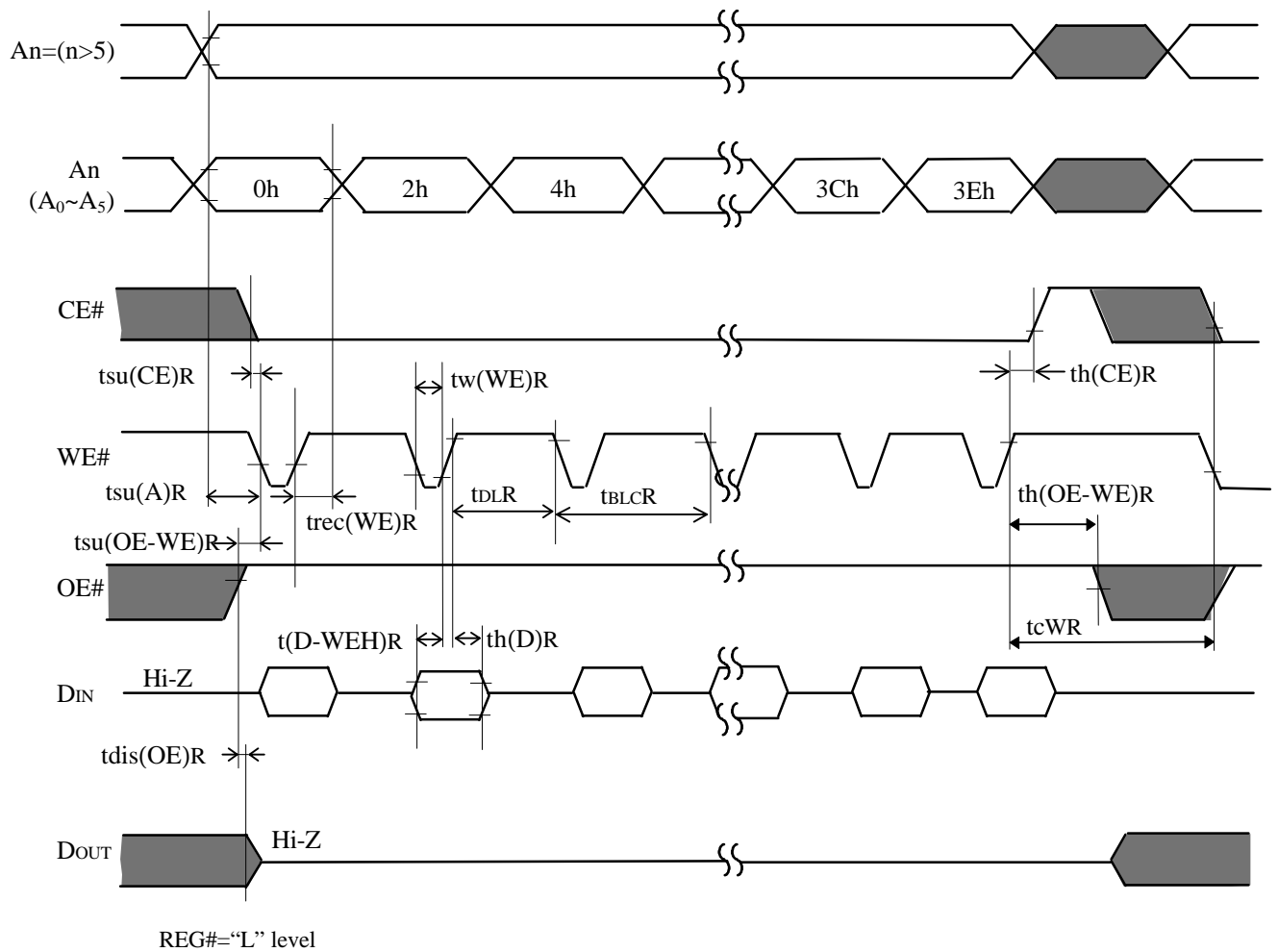
BYTE WRITE TIMING CHART



REG#="L" level



PAGE MODE WRITE TIMING CHART



Note 5 : Test Conditions

- Input pulse levels : $V_{IL}=0.4V, V_{IH}=2.8V$
- Input pulse rise, fall time : $t_r=t_f=10ns$
- Reference voltage
 - Input : $V_{IL}=0.8V, V_{IH}=2.4V$
 - Output : $V_{OL}=0.8V, V_{OH}=2.0V$
 (ten and tdis are measured when output voltage is $\pm 500mV$ from steady state.)
- Load : $100pF + 1$ TTL gate
- $5pF + 1$ TTL gate (at ten and tdis measuring)

- 6 : Indicates the don't care input
- 7 : Writing is executed in overlap of CE# and WE# are "L" level. (only for Common Memory)
- 8 : Don't apply inverted phase signal externally when Dm pin is in output mode.
- 9 : CE# is indicated as follows:
 - Read A/Write A : CE#=CE1#=CE2#
 - Read B/Write B : CE#=CE1#, CE2#="H" level
 - Read C/Write C : CE#=CE2#, CE1#="H" level

19. ELECTRICAL CHARACTERISTICS

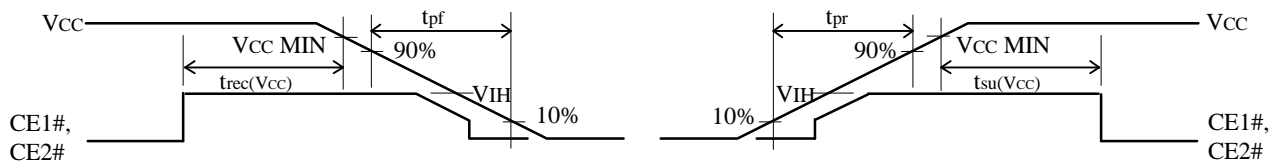
BATTERY BACKUP (Ta=0~55°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
V _{BATT}	Back-up enable battery voltage	All pins open	2.6			V	
V _i (CE)	Card enable voltage	2.4V ≤ V _{CC} ≤ 5.25V	2.4			V	
		0V ≤ V _{CC} < 2.4V	V _{cc} -0.1	V _{cc}	V _{cc} +0.1		
I _{cc} (Bup)	Battery back-up supply current	All pins open, V _{BATT} =3V, Ta=25°C	64KB			3	μA
			128KB			3	
			256KB			3	
			512KB			5	
			1MB			3	
			2MB			5	
			4MB			9	
	Battery back-up supply current	All pins open, V _{BATT} =3V	64KB			30	μA
			128KB			30	
			256KB			30	
			512KB			50	
			1MB			30	
			2MB			50	
			4MB			90	

20. TIMING REQUIREMENTS (Ta=0~55°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{pr}	Power supply rise time	0.1		300	ms
t _{pf}	Power supply fall time	3		300	ms
t _{su} (V _{cc})	Setup time at power on	20			ms
t _{rec} (V _{cc})	Recovery time at power off	1000			ns

CARD INSERTION/REMOVAL TIMING DIAGRAM



⚠ Warning (if card with battery / card with auxiliary battery)

- (1) Do not charge, short, disassemble, deform, heat, or throw the batteries into fire, as they may ignite, overheat, rupture or explode.
- (2) Place the batteries out of the reach of children. If somebody swallows them, they should see a doctor immediately.
- (3) When discarding or storing the batteries, wrap them individually with cellophane tape or other nonconductive material. If they are positioned in contact with any other metals or batteries, they may explode, rupture or leak electrolyte solution.

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