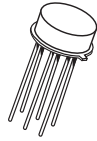


MD3250 MD3250A  
MD3251 MD3251A

DUAL PNP  
SILICON TRANSISTOR



TO-78 CASE

**Central**<sup>TM</sup>  
**Semiconductor Corp.**

**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR MD3250 and MD3251 Series types are dual PNP silicon transistors, manufactured by the epitaxial planar process utilizing two individual chips mounted in a hermetically sealed metal case, designed for differential amplifier applications.

**MARKING: FULL PART NUMBER**

**MAXIMUM RATINGS:** ( $T_A=25^\circ\text{C}$ )

Collector-Emitter Voltage
Collector-Base Voltage
Emitter-Base Voltage
Continuous Collector Current
Power Dissipation (One Die)
Power Dissipation (Both Die)
Power Dissipation (One Die), $T_C=25^\circ\text{C}$
Power Dissipation (Both Die), $T_C=25^\circ\text{C}$
Operating and Storage Junction Temperature

SYMBOL		UNITS
$V_{CEO}$	40	V
$V_{CBO}$	50	V
$V_{EBO}$	5.0	V
$I_C$	50	mA
$P_D$	575	mW
$P_D$	625	mW
$P_D$	1.8	W
$P_D$	2.5	W
$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS:** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
$I_{CBO}$	$V_{CB}=40\text{V}$		10	nA
$I_{CBO}$	$V_{CB}=40\text{V}, T_A=150^\circ\text{C}$		10	$\mu\text{A}$
$I_{EBO}$	$V_{BE}=3.0\text{V}$		10	nA
$BV_{CEO}$	$I_C=10\text{mA}$	40		V
$BV_{CBO}$	$I_C=10\mu\text{A}$	50		V
$BV_{EBO}$	$I_E=10\mu\text{A}$	5.0		V
$V_{CE}(\text{SAT})$	$I_C=10\text{mA}, I_B=1.0\text{mA}$		0.25	V
$V_{CE}(\text{SAT})$	$I_C=50\text{mA}, I_B=5.0\text{mA}$		0.50	V
$V_{BE}(\text{SAT})$	$I_C=10\text{mA}, I_B=1.0\text{mA}$	0.60	0.90	V
$V_{BE}(\text{SAT})$	$I_C=50\text{mA}, I_B=5.0\text{mA}$		1.2	V
$h_{FE}$	$V_{CE}=5.0\text{V}, I_C=10\mu\text{A}$ (MD3250,A)	25		
$h_{FE}$	$V_{CE}=5.0\text{V}, I_C=10\mu\text{A}$ (MD3251,A)	50		
$h_{FE}$	$V_{CE}=5.0\text{V}, I_C=100\mu\text{A}$ (MD3250,A)	50	150	
$h_{FE}$	$V_{CE}=5.0\text{V}, I_C=100\mu\text{A}$ (MD3251,A)	80	300	
$h_{FE}$	$V_{CE}=5.0\text{V}, I_C=1.0\text{mA}$ (MD3250,A)	50	150	
$h_{FE}$	$V_{CE}=5.0\text{V}, I_C=1.0\text{mA}$ (MD3251,A)	100	300	
$h_{FE}$	$V_{CE}=5.0\text{V}, I_C=10\text{mA}$ (MD3250,A)	50		
$h_{FE}$	$V_{CE}=5.0\text{V}, I_C=10\text{mA}$ (MD3251,A)	100		

R0 (9-June 2009)

DUAL PNP  
SILICON TRANSISTOR

**ELECTRICAL CHARACTERISTICS - Continued:** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

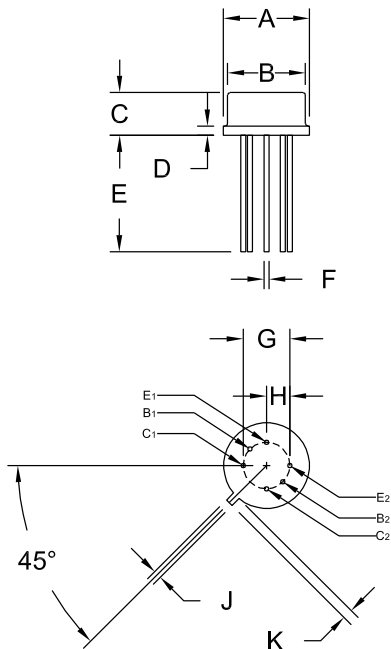
SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
$h_{FE}$	$V_{CE}=5.0\text{V}$ , $I_C=50\text{mA}$ (MD3250,A)	15		
$h_{FE}$	$V_{CE}=5.0\text{V}$ , $I_C=50\text{mA}$ (MD3251,A)	30		
$f_T$	$V_{CE}=20\text{V}$ , $I_C=10\text{mA}$ , $f=100\text{MHz}$ (MD3250,A)	200		MHz
$f_T$	$V_{CE}=20\text{V}$ , $I_C=10\text{mA}$ , $f=100\text{MHz}$ (MD3251,A)	250		MHz
$C_{ob}$	$V_{CB}=5.0\text{V}$ , $I_E=0$ , $f=100\text{kHz}$		6.0	pF
$C_{ib}$	$V_{BE}=1.0\text{V}$ , $I_C=0$ , $f=100\text{kHz}$		8.0	pF

**MATCHING CHARACTERISTICS:**

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
$h_{FE1}/h_{FE2}$ (Note 1)	$V_{CE}=5.0\text{V}$ , $I_C=100\mu\text{A}$	0.90	1.0	
$h_{FE1}/h_{FE2}$ (Note 1)	$V_{CE}=5.0\text{V}$ , $I_C=1.0\text{mA}$	0.90	1.0	
$ V_{BE1}-V_{BE2} $	$V_{CE}=5.0\text{V}$ , $I_C=10\mu\text{A}$		5.0	mV
$ V_{BE1}-V_{BE2} $	$V_{CE}=5.0\text{V}$ , $I_C=100\mu\text{A}$		3.0	mV
$ V_{BE1}-V_{BE2} $	$V_{CE}=5.0\text{V}$ , $I_C=10\text{mA}$		5.0	mV

1) The lowest  $h_{FE}$  reading is taken as  $h_{FE1}$ .

**TO-78 CASE - MECHANICAL OUTLINE**



SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A (DIA)	0.335	0.370	8.51	9.40
B (DIA)	0.305	0.335	7.75	8.51
C	0.150	0.185	3.81	4.70
D	-	0.040	-	1.02
E	0.500	-	12.70	-
F (DIA)	0.016	0.021	0.41	0.53
G	0.200		5.08	
H	0.100		2.54	
J	0.028	0.034	0.71	0.86
K	0.029	0.045	0.74	1.14

TO-78 (REV: R1)

**MARKING: FULL PART NUMBER**

R1

R0 (9-June 2009)