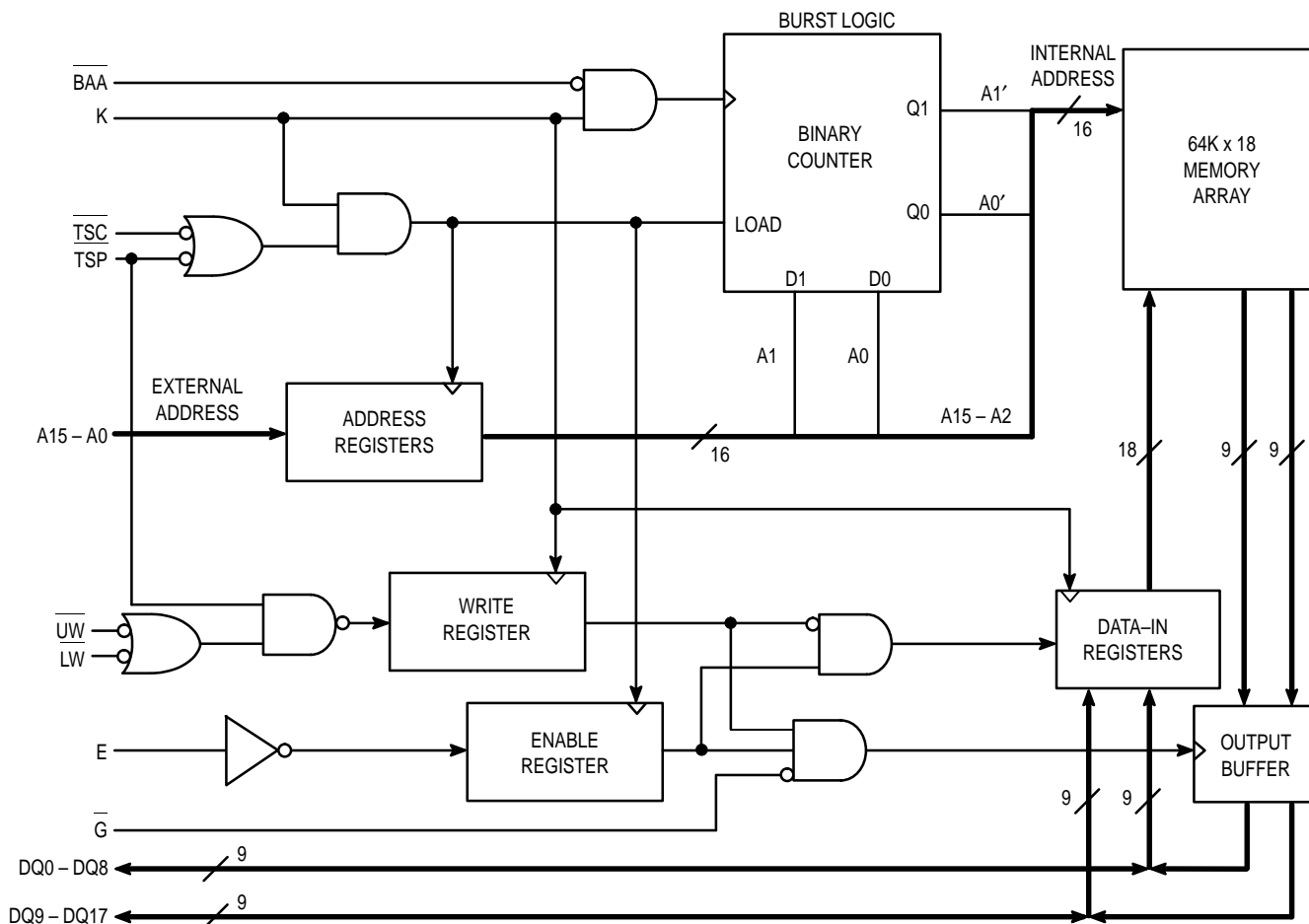
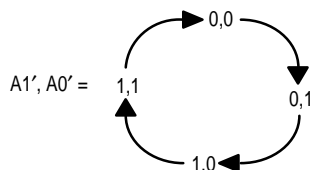


BLOCK DIAGRAM (See Note)



NOTE: All registers are positive-edge triggered. The $\overline{\text{TSC}}$ or $\overline{\text{TSP}}$ signals control the duration of the burst and the start of the next burst. When $\overline{\text{TSP}}$ is sampled low, any ongoing burst is interrupted and a read (independent of W and $\overline{\text{TSC}}$) is performed using the new external address. Alternatively, a $\overline{\text{TSP}}$ -initiated two cycle WRITE can be performed by asserting $\overline{\text{TSP}}$ and a valid address on the first cycle, then negating both $\overline{\text{TSP}}$ and $\overline{\text{TSC}}$ and asserting LW and/or UW with valid data on the second cycle (see Single Write Cycle in WRITE CYCLES timing diagram). When $\overline{\text{TSC}}$ is sampled low (and $\overline{\text{TSP}}$ is sampled high), any ongoing burst is interrupted and a read or write (dependent on W) is performed using the new external address. Chip enable (E) is sampled only when a new base address is loaded. After the first cycle of the burst, BAA controls subsequent burst cycles. When BAA is sampled low, the internal address is advanced prior to the operation. When BAA is sampled high, the internal address is not advanced, thus inserting a wait state into the burst sequence accesses. Upon completion of a burst, the address will wrap around to its initial state. See BURST SEQUENCE TABLE. Write refers to either or both byte write enables (LW, UW).

BURST SEQUENCE GRAPH (See Note)



NOTE: The external two values for A1 and A0 provide the starting point for the burst sequence graph. The burst logic advances A1 and A0 as shown above.

SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, and 3)

E	TSP	TSC	BAA	LW or UW	K	Address	Operation
H	L	X	X	X	L–H	N/A	Deselected
H	X	L	X	X	L–H	N/A	Deselected
L	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
L	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
L	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Suspend Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

NOTES:

1. X means Don't Care.
2. All inputs except G must meet setup and hold times for the low-to-high transition of clock (K).
3. Wait states are inserted by suspending burst.

ASYNCHRONOUS TRUTH TABLE (See Notes 1 and 2)

Operation	G	I/O Status
Read	L	Data Out
Read	H	High-Z
Write	X	High-Z — Data In
Deselected	X	High-Z

NOTES:

1. X means Don't Care.
2. For a write operation following a read operation, G must be high before the input data required setup time and held high through the input data hold time.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{CC}	– 0.5 to + 7.0	V
Voltage Relative to V _{SS} for Any Pin Except V _{CC}	V _{in} , V _{out}	– 0.5 to V _{CC} + 0.5	V
Output Current (per I/O)	I _{out}	± 30	mA
Power Dissipation	P _D	1.6	W
Temperature Under Bias	T _{bias}	– 10 to + 85	°C
Ambient Temperature	T _A	0 to +70	°C
Storage Temperature	T _{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 5\%$, $T_A = 0\text{ to } +70^\circ\text{C}$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.75	5.25	V
Input High Voltage	V_{IH}	2.2	$V_{CC} + 0.3^{**}$	V
Input Low Voltage	V_{IL}	-0.5*	0.8	V

* V_{IL} (min) = -0.5 V dc; V_{IL} (min) = -2.0 V ac (pulse width $\leq 20.0\text{ ns}$) for $I \leq 20.0\text{ mA}$.

** V_{IH} (max) = $V_{CC} + 0.3\text{ V}$ dc; V_{IH} (max) = $V_{CC} + 2.0\text{ V}$ ac (pulse width $\leq 20.0\text{ ns}$) for $I \leq 20.0\text{ mA}$.

DC CHARACTERISTICS AND SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0\text{ to } V_{CC}$)	$I_{kg(I)}$	—	± 1.0	μA
Output Leakage Current ($G = V_{IH}$)	$I_{kg(O)}$	—	± 1.0	μA
AC Supply Current (Device Selected, All Outputs Open, Freq = Max)	I_{CCA}	—	TBD	mA
	MCM67M618B-9 MCM67M618B-10 MCM67M618B-12			
CMOS Standby Supply Current (Device Deselected, Freq = 0, $V_{CC} = \text{Max}$, All Inputs Static at CMOS Levels $V_{in} \leq V_{SS} + 0.2\text{ V}$ or $\geq V_{CC} - 0.2\text{ V}$)	I_{SB2}	—	TBD	mA
Clock Running (Device Deselected, Freq = Max, $V_{CC} = \text{Max}$, All Inputs Toggling at CMOS Levels $V_{in} \leq V_{SS} + 0.2\text{ V}$ or $\geq V_{CC} - 0.2\text{ V}$)	I_{SB4}	—	TBD	mA
Output Low Voltage ($I_{OL} = +8.0\text{ mA}$)	V_{OL}	—	0.4	V
Output High Voltage ($I_{OH} = -4.0\text{ mA}$)	V_{OH}	2.4	3.3	V

NOTE: Good decoupling of the local power supply should always be used. DC characteristics are guaranteed for all possible 68040 and PowerPC bus cycles.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A = 25^\circ\text{C}$, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_{in}	—	4	5	pF
Input/Output Capacitance	$C_{I/O}$	—	6	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 5\%$, $T_A = 0\text{ to } +70^\circ\text{C}$, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V Output Timing Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V Output Load See Figure 1 Unless Otherwise Noted
 Input Rise/Fall Time 3 ns

READ/WRITE CYCLE TIMING (See Notes 1, 3, and 4)

Parameter	Symbol	MCM67M618B-9		MCM67M618B-10		MCM67M618B-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{KHKH}	15	—	16.6	—	20	—	ns	
Clock Access Time	t_{KHQV}	—	9	—	10	—	12	ns	5
Output Enable to Output Valid	t_{GLQV}	—	5	—	5	—	6	ns	
Clock High to Output Active	t_{KHQX1}	6	—	6	—	6	—	ns	
Clock High to Output Change	t_{KHQX2}	3	—	3	—	3	—	ns	
Output Enable to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	
Output Disable to Q High-Z	t_{GHQZ}	—	6	—	7	—	7	ns	6
Clock High to Q High-Z	t_{KHQZ}	3	6	3	7	3	7	ns	6
Clock High Pulse Width	t_{KHKL}	5	—	5	—	6	—	ns	
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	6	—	ns	
Setup Times: Address Address Status Data In Write Address Advance Chip Enable	t_{AVKH} t_{TSVKH} t_{DVKH} t_{WVKH} t_{BAVKH} t_{EVKH}	2.5	—	2.5	—	2.5	—	ns	7
Hold Times: Address Address Status Data In Write Address Advance Chip Enable	t_{KHAX} t_{KHTSX} t_{KHDX} t_{KHWX} t_{KHBAX} t_{KHEX}	0.5	—	0.5	—	0.5	—	ns	7

NOTES:

- In setup and hold times, W (write) refers to either one or both byte write enables \overline{LW} and \overline{UW} .
- A read cycle is defined by \overline{UW} and \overline{LW} high or TSP low for the setup and hold times. A write cycle is defined by \overline{LW} or \overline{UW} low and TSP high for the setup and hold times.
- All read and write cycle timings are referenced from K or G.
- G is a don't care when \overline{UW} or \overline{LW} is sampled low.
- Maximum access times are guaranteed for all possible MC68040 and PowerPC external bus cycles.
- Transition is measured $\pm 500\text{ mV}$ from steady-state voltage. This parameter is sampled rather than 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQZ1} min for a given device and from device to device.
- This is a synchronous device. All addresses must meet the specified setup and hold times for **ALL** rising edges of K whenever \overline{TSP} or \overline{TSC} is low, and the chip is selected. All other synchronous inputs must meet the specified setup and hold times for **ALL** rising edges of K when the chip is enabled. Chip enable must be valid at each rising edge of clock for the device (when \overline{TSP} or \overline{TSC} is low) to remain enabled.

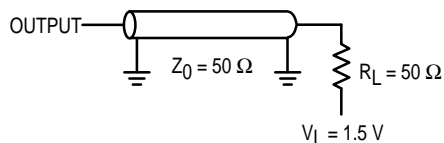
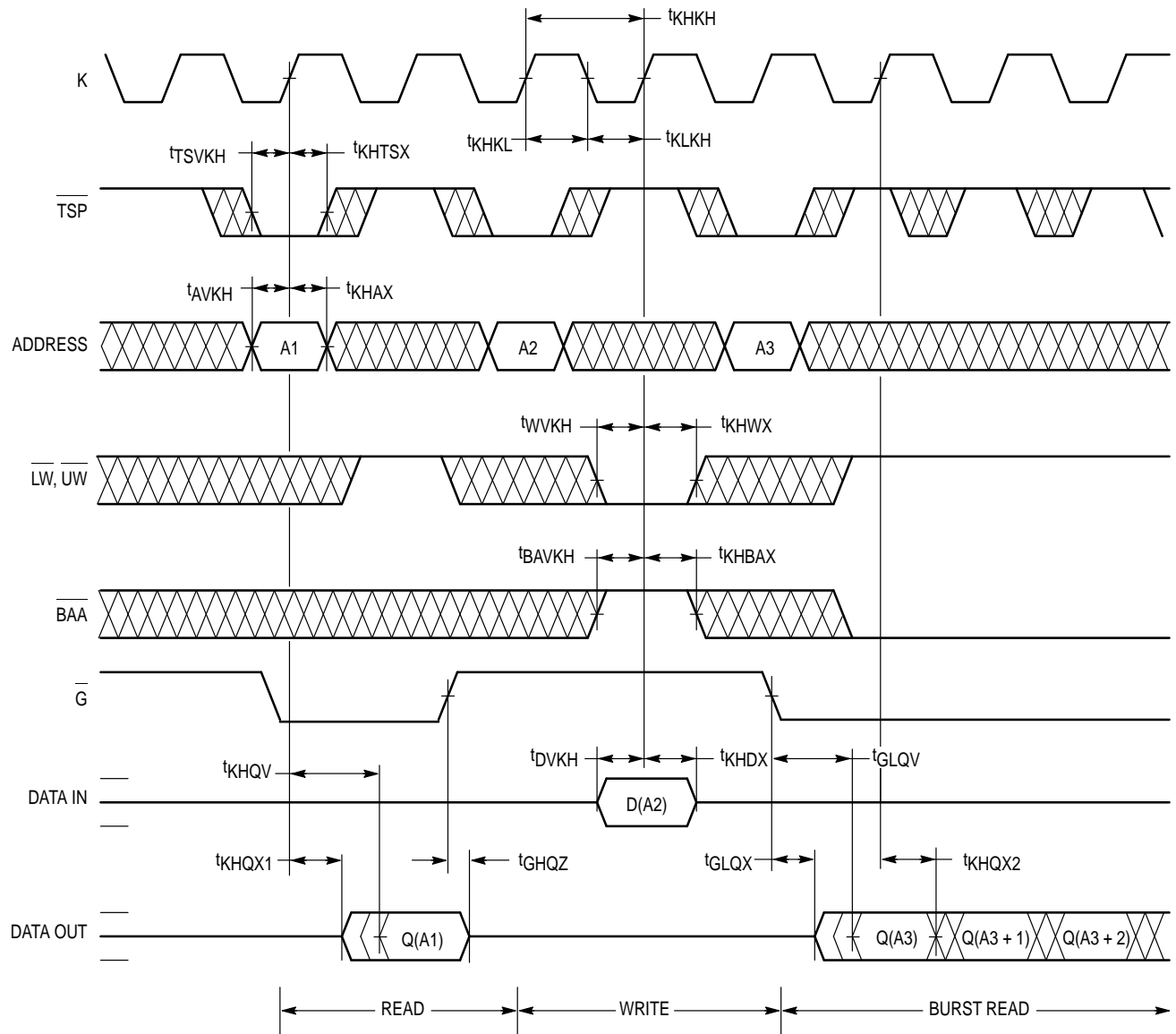
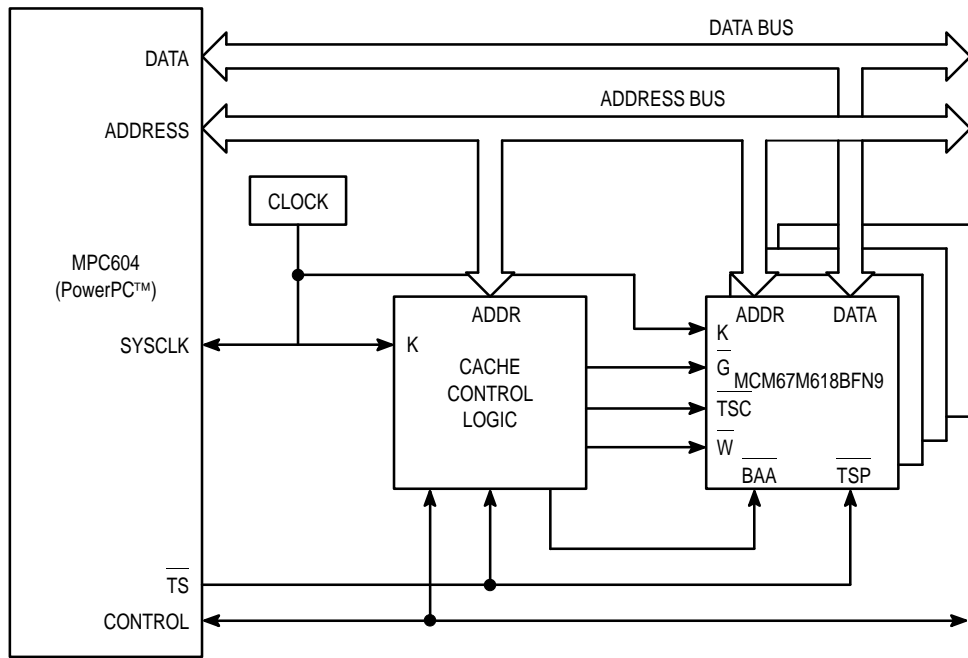


Figure 1. Test Load

COMBINATION READ/WRITE CYCLE (\overline{E} Low, \overline{TSC} High)



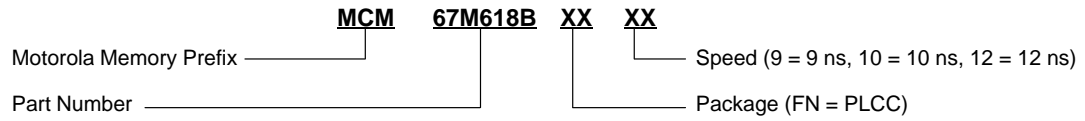
APPLICATION EXAMPLE



512K Byte Burstable, Secondary Cache
Using Four MCM67M618BFN9s with a 66 MHz MPC604 PowerPC™

Figure 2.

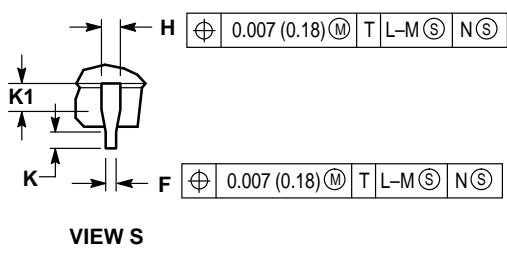
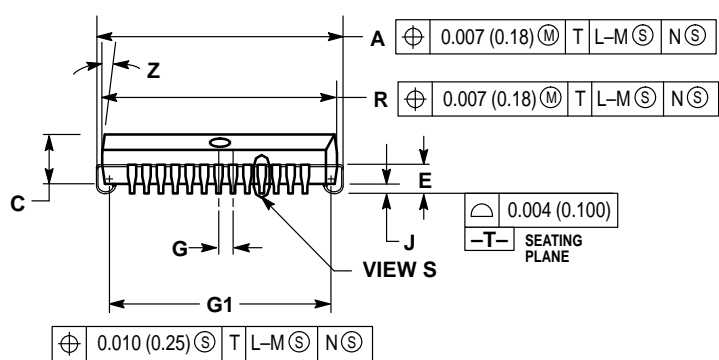
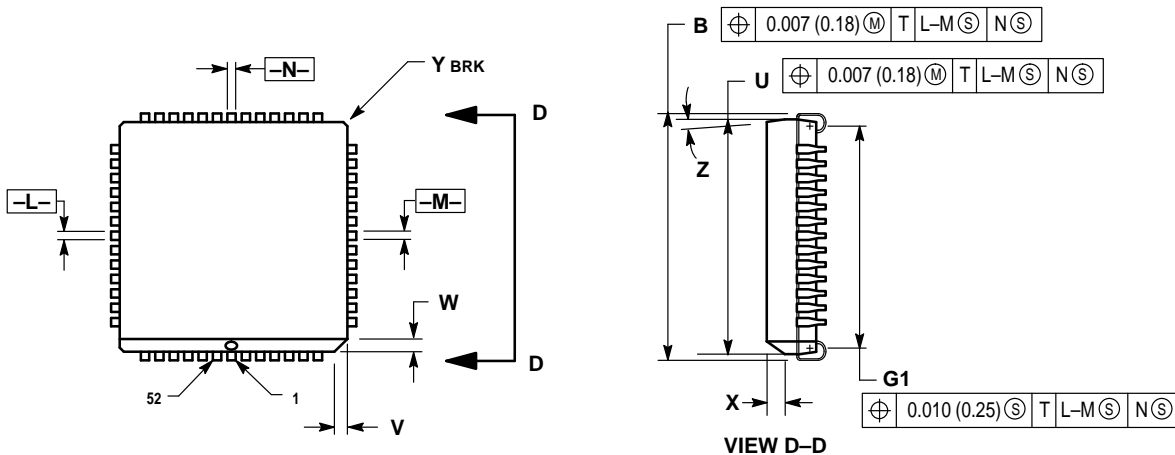
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM67M618BFN9 MCM67M618BFN10 MCM67M618BFN12


PACKAGE DIMENSIONS

**FN PACKAGE
52-LEAD PLCC
CASE 778-02**



- NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
 2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
 3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 5. CONTROLLING DIMENSION: INCH.
 6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
 7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.785	0.795	19.94	20.19
B	0.785	0.795	19.94	20.19
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.750	0.756	19.05	19.20
U	0.750	0.756	19.05	19.20
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2° 10°		2° 10°	
G1	0.710	0.730	18.04	18.54
K1	0.040	—	1.02	—

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