

# 64K x 4 Bit Static RAM

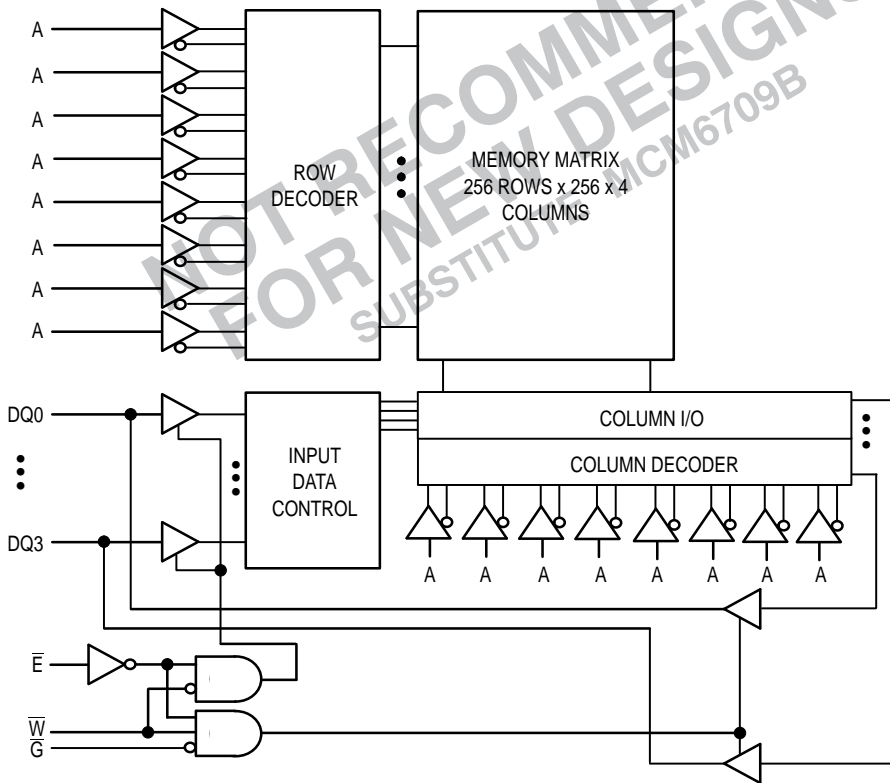
The MCM6709A is a 262,144 bit static random access memory organized as 65,536 words of 4 bits, fabricated using high-performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ( $\bar{G}$ ) provides increased system flexibility and eliminates bus contention problems.

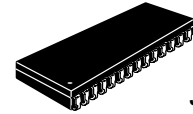
The MCM6709A is available in a 300 mil, 28 lead plastic surface-mount SOJ package.

- Single 5 V  $\pm$  10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times:
  - MCM6709A-8 = 8 ns
  - MCM6709A-10 = 10 ns
  - MCM6709A-12 = 12 ns

### BLOCK DIAGRAM



## MCM6709A



**J PACKAGE**  
**300 MIL SOJ**  
**CASE 810B-03**

### PIN ASSIGNMENT

NC	1	28	VCC
A0	2	27	A15
A1	3	26	A14
A2	4	25	A13
A3	5	24	A12
A4	6	23	A11
A5	7	22	A10
A6	8	21	NC
A7	9	20	NC
A8	10	19	DQ0
A9	11	18	DQ1
$\bar{E}$	12	17	DQ2
$\bar{G}$	13	16	DQ3
VSS	14	15	$\bar{W}$

### PIN NAMES

A0 – A15	Address Inputs
$\bar{W}$	Write Enable
$\bar{G}$	Output Enable
$\bar{E}$	Chip Enable
DQ0 – DQ3	Data Input/Output
VCC	+ 5 V Power Supply
VSS	Ground
NC	No Connection

**TRUTH TABLE** (X = Don't Care)

$\bar{E}$	$\bar{G}$	$\bar{W}$	Mode	Output	Cycle
H	X	X	Not Selected	High-Z	—
L	H	H	Read	High-Z	—
L	L	H	Read	D <sub>out</sub>	Read Cycle
L	X	L	Write	D <sub>in</sub>	Write Cycle

**ABSOLUTE MAXIMUM RATINGS** (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V <sub>CC</sub>	- 0.5 to + 7.0	V
Voltage Relative to V <sub>SS</sub> for Any Pin Except V <sub>CC</sub>	V <sub>in</sub> , V <sub>out</sub>	- 0.5 to V <sub>CC</sub> + 0.5	V
Output Current (per I/O)	I <sub>out</sub>	± 30	mA
Power Dissipation	P <sub>D</sub>	2.0	W
Temperature Under Bias	T <sub>bias</sub>	- 10 to + 85	°C
Operating Temperature	T <sub>A</sub>	0 to + 70	°C
Storage Temperature — Plastic	T <sub>stg</sub>	- 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

**DC OPERATING CONDITIONS AND CHARACTERISTICS**

(V<sub>CC</sub> = 5.0 V ± 10%, T<sub>A</sub> = 0 to 70°C, Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V <sub>CC</sub>	4.5	5.0	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	—	V <sub>CC</sub> + 0.3*	V
Input Low Voltage	V <sub>IL</sub>	- 0.5**	—	0.8	V

\* V<sub>IH</sub> (max) = V<sub>CC</sub> + 0.3 V dc; V<sub>IH</sub> (max) = V<sub>CC</sub> + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

\*\* V<sub>IL</sub> (min) = - 0.5 V dc @ 30.0 mA; V<sub>IL</sub> (min) = - 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

**DC CHARACTERISTICS**

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V <sub>in</sub> = 0 to V <sub>CC</sub> )	I <sub>lkg(I)</sub>	—	± 1.0	μA
Output Leakage Current ( $\bar{E}$ = V <sub>IH</sub> , V <sub>out</sub> = 0 to V <sub>CC</sub> )	I <sub>lkg(O)</sub>	—	± 1.0	μA
Output High Voltage (I <sub>OH</sub> = - 4.0 mA)	V <sub>OH</sub>	2.4	—	V
Output Low Voltage (I <sub>OL</sub> = 8.0 mA)	V <sub>OL</sub>	—	0.4	V

**POWER SUPPLY CURRENTS**

Parameter	Symbol	MCM6709A-8	MCM6709A-10	MCM6709A-12	Unit	Notes
AC Active Supply Current (I <sub>out</sub> = 0 mA, V <sub>CC</sub> = max, f = f <sub>max</sub> )	I <sub>CCA</sub>	185	175	165	mA	1, 2, 3
AC Standby Current ( $\bar{E}$ = V <sub>IH</sub> , V <sub>CC</sub> = max, f = f <sub>max</sub> )	I <sub>SB1</sub>	120	110	105	mA	1, 2, 3
CMOS Standby Current (V <sub>CC</sub> = max, f = 0 MHz, $\bar{E}$ ≥ V <sub>CC</sub> - 0.2 V, V <sub>in</sub> ≤ V <sub>SS</sub> , or ≥ V <sub>CC</sub> - 0.2 V)	I <sub>SB2</sub>	50	50	50	mA	

**NOTES:**

- Reference AC Operating Conditions and Characteristics for input and timing (V<sub>IH</sub>/V<sub>IL</sub>, t<sub>r</sub>/t<sub>f</sub>, pulse level 0 to 3.0 V, V<sub>IH</sub> = 3.0 V).
- All addresses transition simultaneously low (LSB) and then high (MSB).
- Data states are all zero.

**CAPACITANCE** ( $f = 1.0 \text{ MHz}$ ,  $dV = 3.0 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ , Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	$C_{in}$	5	pF
Control Pin Input Capacitance ( $\overline{E}$ , $\overline{G}$ , $\overline{W}$ )	$C_{in}$	5	pF
Input/Output Capacitance	$C_{I/O}$	6	pF

**AC OPERATING CONDITIONS AND CHARACTERISTICS**

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $T_A = 0 \text{ to } +70^\circ\text{C}$ , Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V      Output Timing Measurement Reference Level ..... 1.5 V  
 Input Pulse Levels ..... 0 to 3.0 V      Output Load ..... See Figure 1A  
 Input Rise/Fall Time ..... 2 ns

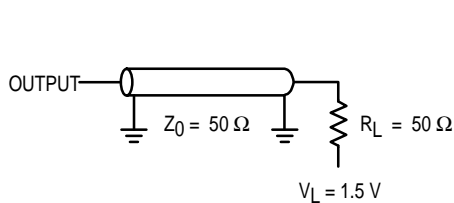
**READ CYCLES 1 AND 2** (See Notes 1 and 2)

Parameter	Symbol	MCM6709A-8		MCM6709A-10		MCM6709A-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	$t_{AVAV}$	8	—	10	—	12	—	ns	3
Address Access Time	$t_{AVQV}$	—	8	—	10	—	12	ns	
Chip Enable Access Time	$t_{ELQV}$	—	8	—	10	—	12	ns	
Output Enable Access Time	$t_{GLQV}$	—	4	—	5	—	6	ns	
Output Hold from Address Change	$t_{AXQX}$	3	—	3	—	3	—	ns	
Chip Enable Low to Output Active	$t_{ELQX}$	1	—	1	—	1	—	ns	4, 5, 6
Output Enable Low to Output Active	$t_{GLQX}$	0	—	0	—	0	—	ns	4, 5, 6
Chip Enable High to Output High-Z	$t_{EHQZ}$	0	4.5	0	5	0	6	ns	4, 5, 6
Output Enable High to Output High-Z	$t_{GHQZ}$	0	4	0	5	0	6	ns	4, 5, 6

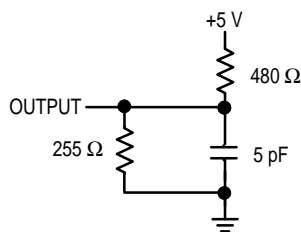
**NOTES:**

1.  $\overline{W}$  is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature,  $t_{EHQZ}$  max is less than  $t_{ELQX}$  min, and  $t_{GHQZ}$  max is less than  $t_{GLQX}$  min, both for a given device and from device to device.
5. Transition is measured 200 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.

**AC TEST LOADS**



**Figure 1A**

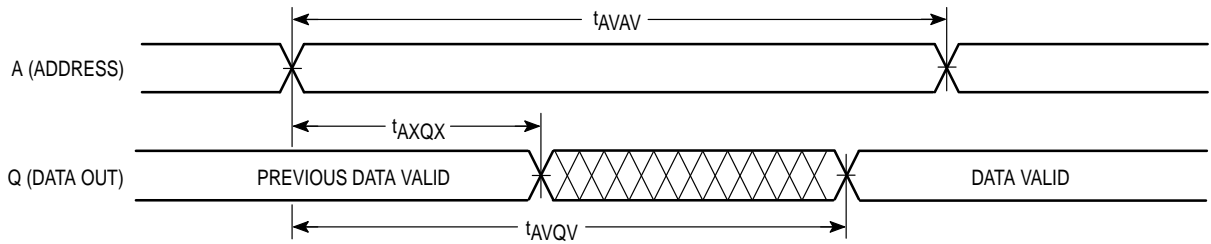


**Figure 1B**

**TIMING LIMITS**

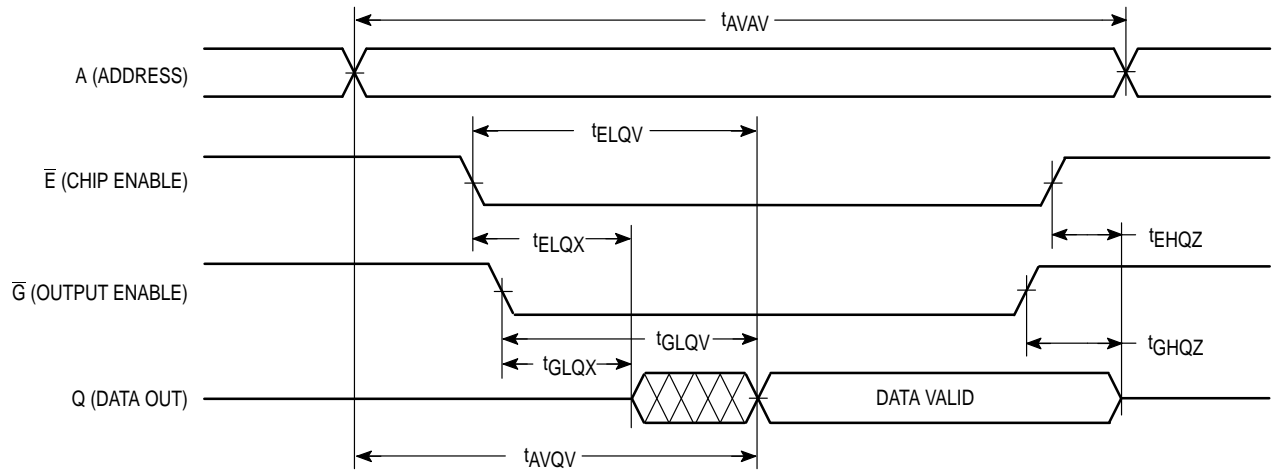
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

**READ CYCLE 1 (See Note)**



NOTE: Device is continuously selected ( $\bar{E} = V_{IL}$ ,  $\bar{G} = V_{IL}$ ).

**READ CYCLE 2 (See Note)**



NOTE: Addresses valid prior to or coincident with  $\bar{E}$  going low.

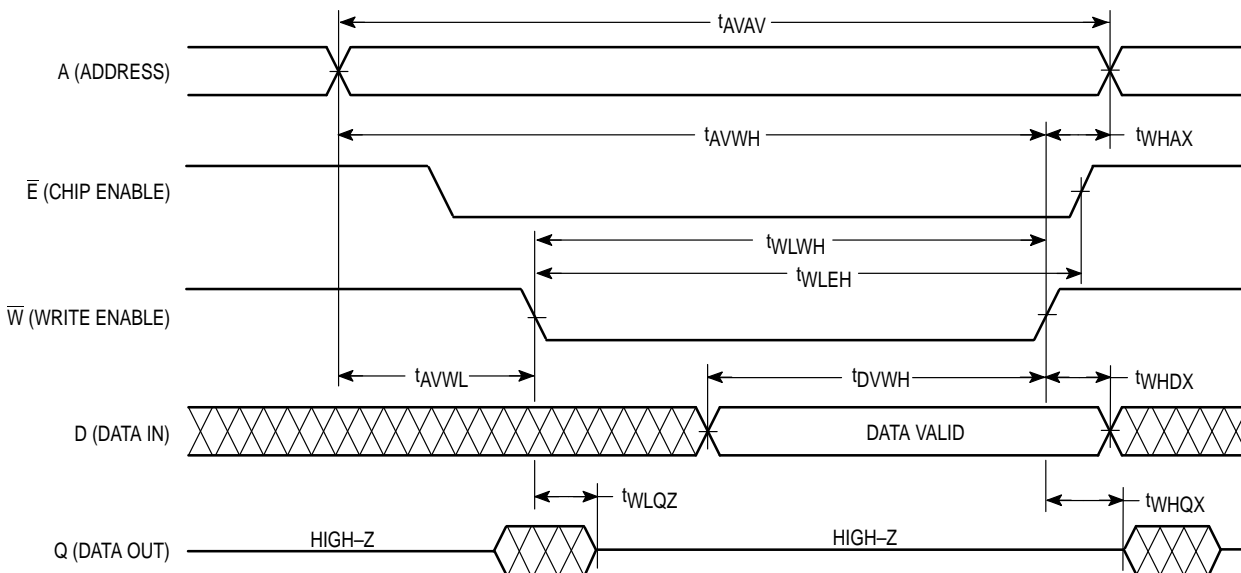
**WRITE CYCLE 1** ( $\bar{W}$  Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709A-8		MCM6709A-10		MCM6709A-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	8	—	10	—	12	—	ns	3
Address Setup Time	$t_{AVWL}$	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVWH}$	8	—	9	—	10	—	ns	
Write Pulse Width	$t_{WLWH}$ , $t_{WLEH}$	8	—	9	—	10	—	ns	
Data Valid to End of Write	$t_{DVWH}$	4	—	5	—	6	—	ns	
Data Hold Time	$t_{WHDX}$	0	—	0	—	0	—	ns	
Write Low to Data High-Z	$t_{WLQZ}$	0	4	0	5	0	6	ns	4, 5, 6
Write High to Output Active	$t_{WHQX}$	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	$t_{WHAX}$	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature,  $t_{WLQZ}$  max is less than  $t_{WHQX}$  min both for a given device and from device to device.

**WRITE CYCLE 1**



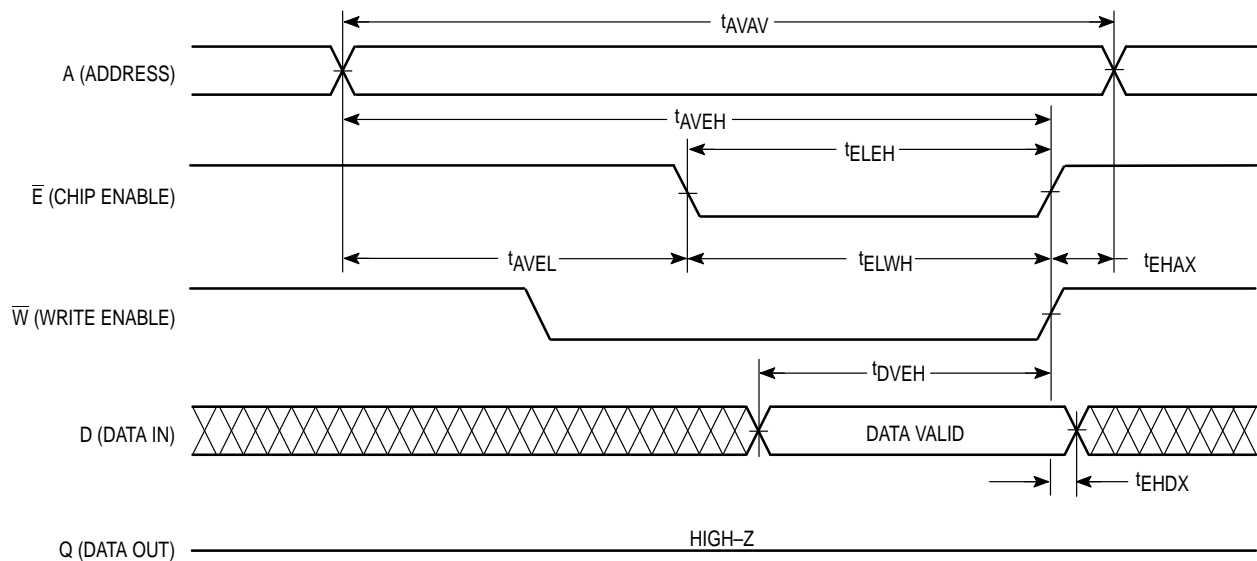
**WRITE CYCLE 2** ( $\bar{E}$  Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6709A-8		MCM6709A-10		MCM6709A-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	$t_{AVAV}$	8	—	10	—	12	—	ns	3
Address Setup Time	$t_{AVEL}$	0	—	0	—	0	—	ns	
Address Valid to End of Write	$t_{AVEH}$	8	—	9	—	10	—	ns	
Chip Enable to End of Write	$t_{ELEH}$ , $t_{ELWH}$	7	—	8	—	9	—	ns	4, 5
Data Valid to End of Write	$t_{DVEH}$	4	—	5	—	6	—	ns	
Data Hold Time	$t_{EHDX}$	0	—	0	—	0	—	ns	
Write Recovery Time	$t_{EHAX}$	0	—	0	—	0	—	ns	

**NOTES:**

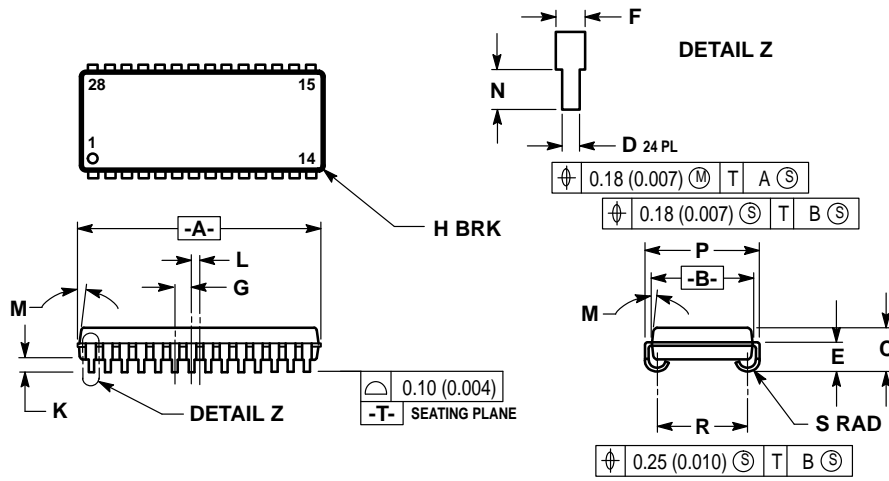
1. A write occurs during the overlap of  $\bar{E}$  low and  $\bar{W}$  low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If  $\bar{E}$  goes low coincident with or after  $\bar{W}$  goes low, the output will remain in a high impedance condition.
5. If  $\bar{E}$  goes high coincident with or before  $\bar{W}$  goes high, the output will remain in a high impedance condition.

**WRITE CYCLE 2**



# PACKAGE DIMENSIONS

## J PACKAGE 300 MIL SOJ CASE 810B-03



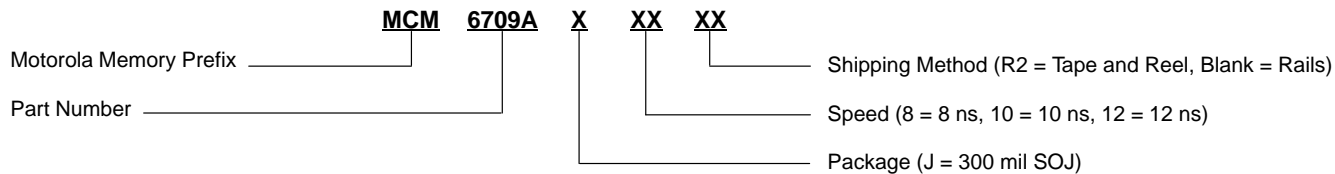
### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.
5. 810B-01 AND -02 OBSOLETE, NEW STANDARD 810B-03.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.29	18.54	0.720	0.730
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	10°	0°	10°
N	0.76	1.14	0.030	0.045
P	8.38	8.64	0.330	0.340
R	6.60	6.86	0.260	0.270
S	0.77	1.01	0.030	0.040

## ORDERING INFORMATION

(Order by Full Part Number)



Full Part Numbers — MCM6709AJ8      MCM6709AJ8R2  
MCM6709AJ10      MCM6709AJ10R2  
MCM6709AJ12      MCM6709AJ12R2

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MCM6709A/D

