

# MC74VHCT240A

## Octal Bus Buffer/Line Driver

### Inverting with 3–State Outputs

The MC74VHCT240A is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT240A is an inverting 3–state buffer, and has two active–low output enables. This device is designed to be used with 3–state memory address drivers, etc.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT240A input and output (when disabled) structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage–input/output voltage mismatch, battery backup, hot insertion, etc.

#### Features

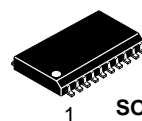
- High Speed:  $t_{PD} = 5.6$  ns (Typ) at  $V_{CC} = 5.0$  V
- Low Power Dissipation:  $I_{CC} = 4$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- TTL–Compatible Inputs:  $V_{IL} = 0.8$  V;  $V_{IH} = 2.0$  V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 1.1$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- Chip Complexity: 110 FETs or 27.5 Equivalent Gates
- These Devices are Pb–Free and are RoHS Compliant



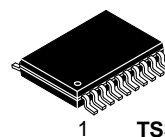
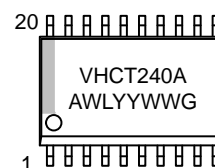
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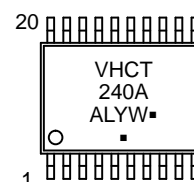
#### MARKING DIAGRAMS



SOIC–20WB  
SUFFIX DW  
CASE 751D



TSSOP–20  
SUFFIX DT  
CASE 948E



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb–Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

# MC74VHCT240A

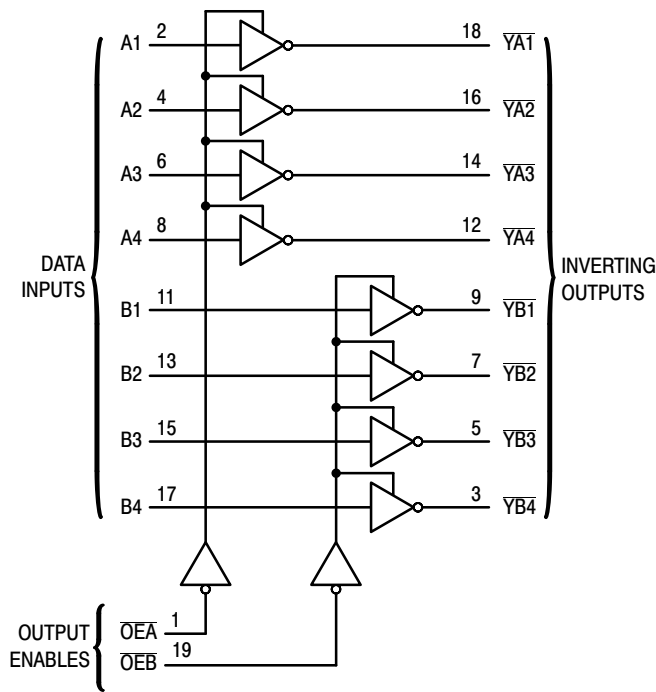


Figure 1. Logic Diagram

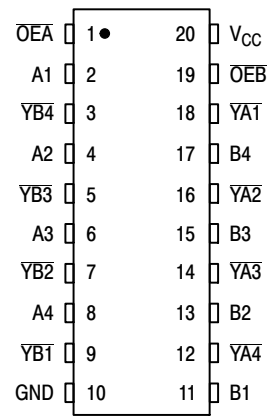


Figure 2. Pin Assignment

## FUNCTION TABLE

| INPUTS   |      | OUTPUTS |
|----------|------|---------|
| OEA, OEB | A, B | YA, YB  |
| L        | L    | H       |
| L        | H    | L       |
| H        | X    | Z       |

## MAXIMUM RATINGS

| Symbol    | Parameter  | Value                                     | Unit |
|-----------|--|---|------|
| $V_{CC}$  | DC Supply Voltage  | - 0.5 to + 7.0                            | V    |
| $V_{in}$  | DC Input Voltage   | - 0.5 to + 7.0                            | V    |
| $V_{out}$ | DC Output Voltage<br>Output in 3-State<br>High or Low State        | - 0.5 to + 7.0<br>- 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{IK}$  | Input Diode Current  | - 20                                      | mA   |
| $I_{OK}$  | Output Diode Current ( $V_{OUT} < GND$ ; $V_{OUT} > V_{CC}$ )      | $\pm 20$                                  | mA   |
| $I_{out}$ | DC Output Current, per Pin   | $\pm 25$                                  | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                           | $\pm 75$                                  | mA   |
| $P_D$     | Power Dissipation in Still Air,<br>SOIC Package†<br>TSSOP Package† | 500<br>450                                | mW   |
| $T_{stg}$ | Storage Temperature  | - 65 to + 150                             | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating - SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol     | Parameter   | Min    | Max             | Unit |
|------------|---|--------|-----------------|------|
| $V_{CC}$   | DC Supply Voltage   | 4.5    | 5.5             | V    |
| $V_{in}$   | DC Input Voltage  | 0      | 5.5             | V    |
| $V_{out}$  | DC Output Voltage<br>Output in 3-State<br>High or Low State | 0<br>0 | 5.5<br>$V_{CC}$ | V    |
| $T_A$      | Operating Temperature                                       | - 40   | + 85            | °C   |
| $t_r, t_f$ | Input Rise and Fall Time<br>$V_{CC} = 5.0V \pm 0.5V$        | 0      | 20              | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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## DC ELECTRICAL CHARACTERISTICS

| Symbol             | Parameter   | Test Conditions   | V <sub>CC</sub><br>V | T <sub>A</sub> = 25°C |     |        | T <sub>A</sub> = - 40 to 85°C |       | Unit |
|--------------------|---|---|----------------------|-----------------------|-----|--------|-------------------------------|-------|------|
|                    |   |   |                      | Min                   | Typ | Max    | Min                           | Max   |      |
| V <sub>IH</sub>    | Minimum High-Level Input Voltage  |   | 4.5 to 5.5           | 2.0                   |     |        | 2.0                           |       | V    |
| V <sub>IL</sub>    | Maximum Low-Level Input Voltage   |   | 4.5 to 5.5           |                       |     | 0.8    |                               | 0.8   | V    |
| V <sub>OH</sub>    | Minimum High-Level Output Voltage<br>V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OH</sub> = - 50μA  | 4.5                  | 4.4                   | 4.5 |        | 4.4                           |       | V    |
|                    |   | I <sub>OH</sub> = - 8mA   | 4.5                  | 3.94                  |     |        | 3.80                          |       |      |
| V <sub>OL</sub>    | Maximum Low-Level Output Voltage<br>V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  | I <sub>OL</sub> = 50μA  | 4.5                  |                       | 0.0 | 0.1    |                               | 0.1   | V    |
|                    |   | I <sub>OL</sub> = 8mA   | 4.5                  |                       |     | 0.36   |                               | 0.44  |      |
| I <sub>in</sub>    | Maximum Input Leakage Current   | V <sub>in</sub> = 5.5 V or GND  | 0 to 5.5             |                       |     | ± 0.1  |                               | ± 1.0 | μA   |
| I <sub>oz</sub>    | Maximum 3-State Leakage Current   | V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>V <sub>out</sub> = V <sub>CC</sub> or GND | 5.5                  |                       |     | ± 0.25 |                               | ± 2.5 | μA   |
| I <sub>CC</sub>    | Maximum Quiescent Supply Current  | V <sub>in</sub> = V <sub>CC</sub> or GND  | 5.5                  |                       |     | 4.0    |                               | 40.0  | μA   |
| I <sub>CC(T)</sub> | Quiescent Supply Current  | Per Input: V <sub>IN</sub> = 3.4V<br>Other Input: V <sub>CC</sub> or GND                          | 5.5                  |                       |     | 1.35   |                               | 1.50  | mA   |
| I <sub>OPD</sub>   | Output Leakage Current  | V <sub>OUT</sub> = 5.5V   | 0                    |                       |     | 0.5    |                               | 5.0   | μA   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns)

| Symbol                                   | Parameter   | Test Conditions  | T <sub>A</sub> = 25°C |            |              | T <sub>A</sub> = - 40 to 85°C |              | Unit |
|--|---|--|-----------------------|------------|--------------|-------------------------------|--------------|------|
|  |   |  | Min                   | Typ        | Max          | Min                           | Max          |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub>   | Maximum Propagation Delay<br>A to $\bar{Y}$ A or B to $\bar{Y}$ B                           | V <sub>CC</sub> = 5.0 ± 0.5V<br>C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF |                       | 5.6<br>6.1 | 7.8<br>8.8   | 1.0<br>1.0                    | 9.0<br>10.0  | ns   |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub>   | Output Enable Time<br>$\bar{O}E\bar{A}$ to $\bar{Y}$ A or $\bar{O}E\bar{B}$ to $\bar{Y}$ B  | V <sub>CC</sub> = 5.0 ± 0.5V<br>R <sub>L</sub> = 1kΩ<br>C <sub>L</sub> = 50pF  |                       | 7.7<br>8.2 | 10.4<br>11.4 | 1.0<br>1.0                    | 12.0<br>13.0 | ns   |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub>   | Output Disable Time<br>$\bar{O}E\bar{A}$ to $\bar{Y}$ A or $\bar{O}E\bar{B}$ to $\bar{Y}$ B | V <sub>CC</sub> = 5.0 ± 0.5V<br>R <sub>L</sub> = 1kΩ                           |                       | 8.8        | 11.4         | 1.0                           | 13.0         | ns   |
| t <sub>OSLH</sub> ,<br>t <sub>OSHL</sub> | Output to Output Skew   | V <sub>CC</sub> = 5.0 ± 0.5V<br>(Note 1)<br>C <sub>L</sub> = 50pF              |                       |            | 1.0          |                               | 1.0          | ns   |
| C <sub>in</sub>                          | Maximum Input Capacitance   |  |                       | 4          | 10           |                               | 10           | pF   |
| C <sub>out</sub>                         | Maximum Three-State Output Capacitance (Output in High-Impedance State)                     |  |                       | 9          |              |                               |              | pF   |

| C <sub>PD</sub> | Power Dissipation Capacitance (Note 2) | Typical @ 25°C, V <sub>CC</sub> = 5.0V |  | Unit |
|-----------------|--|--|--|------|
|                 |  | 19                                     |  |      |
|                 |  |  |  | pF   |

- Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|.
- C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/8 (per bit). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## NOISE CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3.0ns, C<sub>L</sub> = 50pF, V<sub>CC</sub> = 5.0V)

| Symbol           | Parameter                                    | T <sub>A</sub> = 25°C |       | Unit |
|------------------|--|-----------------------|-------|------|
|                  |  | Typ                   | Max   |      |
| V <sub>OLP</sub> | Quiet Output Maximum Dynamic V <sub>OL</sub> | 0.9                   | 1.1   | V    |
| V <sub>OLV</sub> | Quiet Output Minimum Dynamic V <sub>OL</sub> | - 0.9                 | - 1.1 | V    |
| V <sub>IHD</sub> | Minimum High Level Dynamic Input Voltage     |                       | 2.0   | V    |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage      |                       | 0.8   | V    |

# MC74VHCT240A

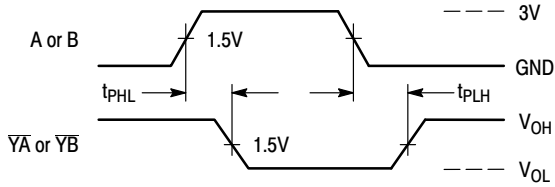


Figure 3. Switching Waveform

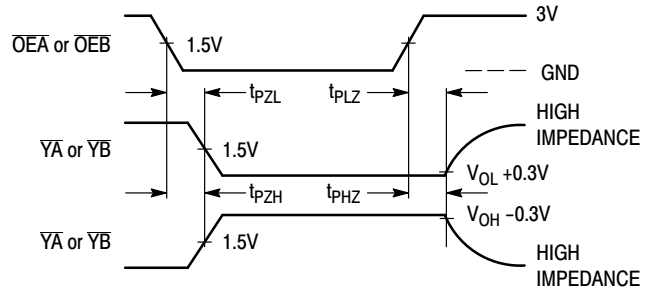
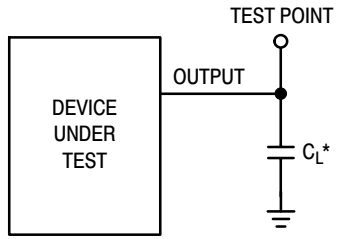
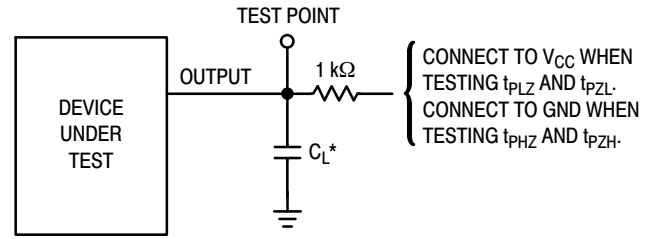


Figure 4. Switching Waveform



\*Includes all probe and jig capacitance

Figure 5. Test Circuit



\*Includes all probe and jig capacitance

Figure 6. Test Circuit

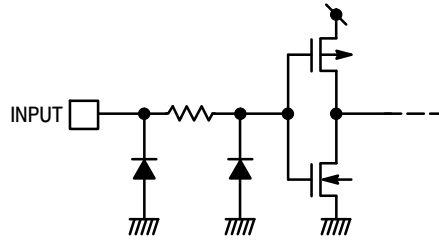


Figure 7. Input Equivalent Circuit

## ORDERING INFORMATION

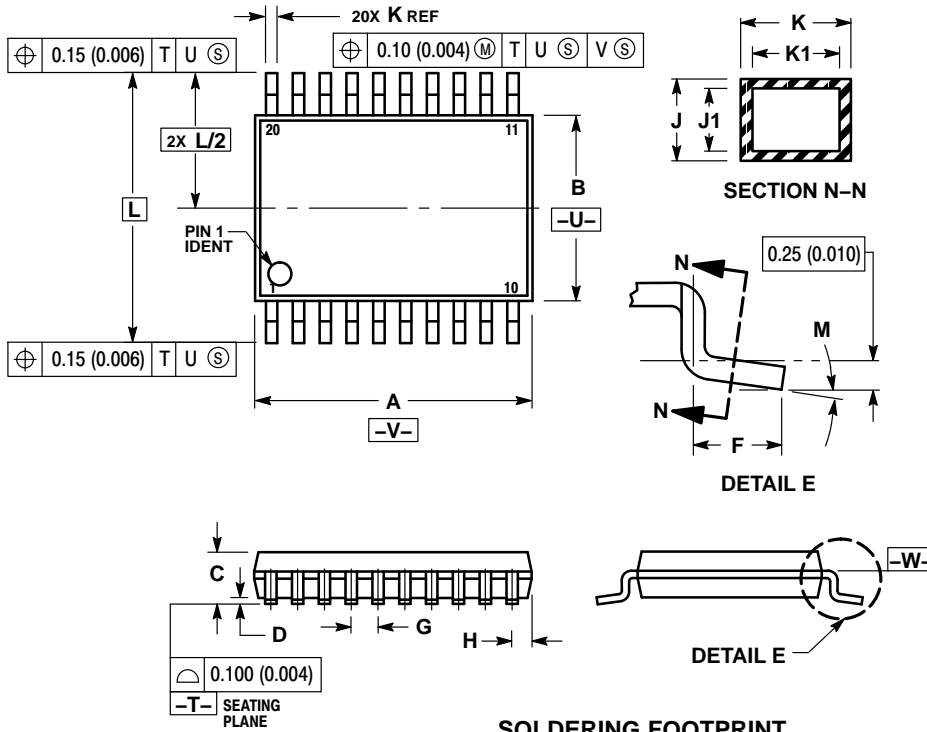
| Device           | Package                | Shipping†          |
|------------------|------------------------|--------------------|
| MC74VHCT240ADWRG | SOIC-20WB<br>(Pb-Free) | 1000 / Tape & Reel |
| MC74VHCT240ADTRG | TSSOP-20<br>(Pb-Free)  | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MC74VHCT240A

## PACKAGE DIMENSIONS

TSSOP-20  
CASE 948E-02  
ISSUE C

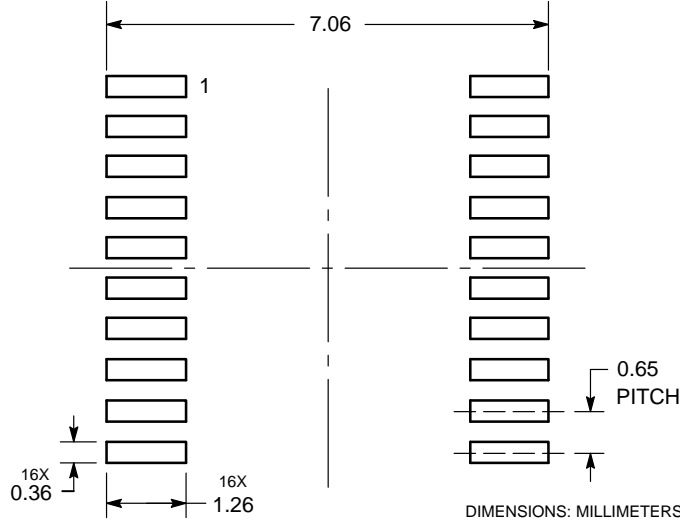


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 6.40        | 6.60 | 0.252     | 0.260 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.27        | 0.37 | 0.011     | 0.015 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

### SOLDERING FOOTPRINT

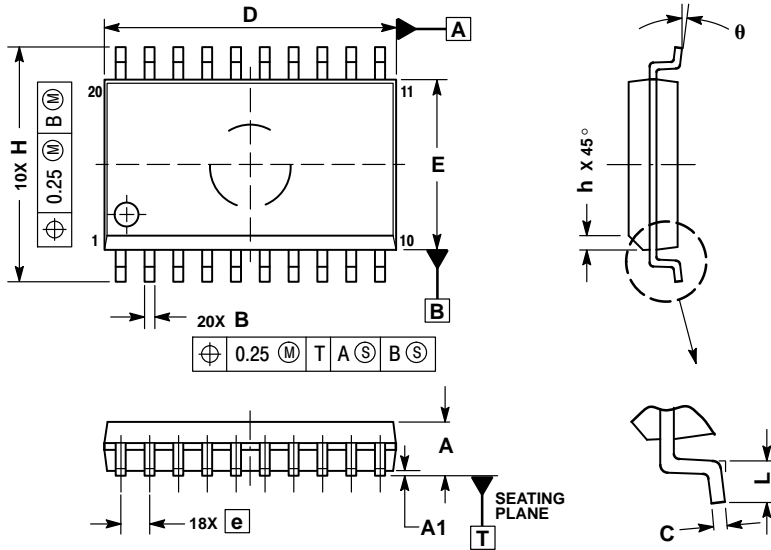


DIMENSIONS: MILLIMETERS

# MC74VHCT240A

## PACKAGE DIMENSIONS

SOIC-20 WB  
DW SUFFIX  
CASE 751D-05  
ISSUE G



### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM   | MILLIMETERS |       |
|-------|-------------|-------|
|       | MIN         | MAX   |
| A     | 2.35        | 2.65  |
| A1    | 0.10        | 0.25  |
| B     | 0.35        | 0.49  |
| C     | 0.23        | 0.32  |
| D     | 12.65       | 12.95 |
| E     | 7.40        | 7.60  |
| e     | 1.27 BSC    |       |
| H     | 10.05       | 10.55 |
| h     | 0.25        | 0.75  |
| L     | 0.50        | 0.90  |
| theta | 0°          | 7°    |

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