

Octal Bus Buffer/Line Driver Inverting with 3-State Outputs

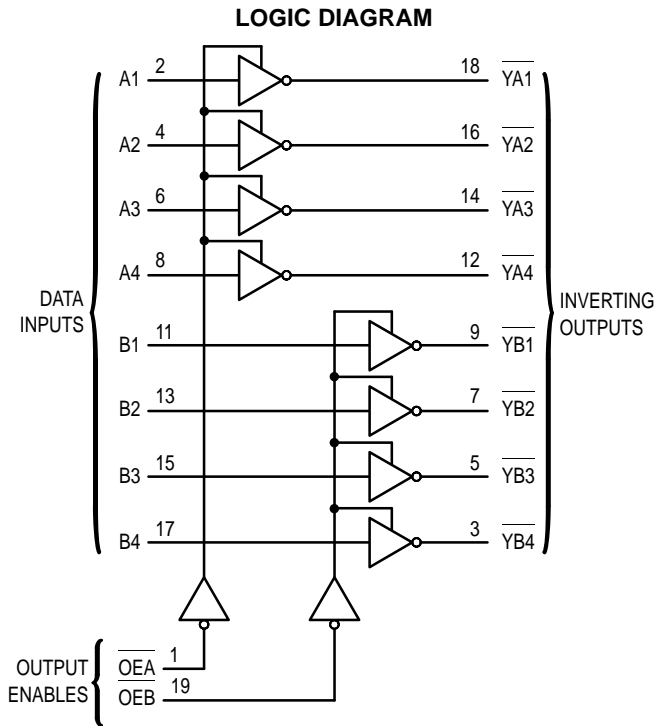
The MC74VHCT240A is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHCT240A is an inverting 3-state buffer, and has two active-low output enables. This device is designed to be used with 3-state memory address drivers, etc.

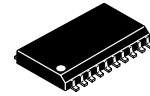
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3V to 5.0V, because it has full 5V CMOS level output swings.

The VHCT240A input and output (when disabled) structures provide protection when voltages between 0V and 5.5V are applied, regardless of the supply voltage. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

- High Speed: $t_{pD} = 5.6ns$ (Typ) at $V_{CC} = 5V$
- Low Power Dissipation: $I_{CC} = 4\mu A$ (Max) at $T_A = 25^\circ C$
- TTL-Compatible Inputs: $V_{IL} = 0.8V$; $V_{IH} = 2.0V$
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 4.5V to 5.5V Operating Range
- Low Noise: $V_{OLP} = 1.1V$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 110 FETs or 27.5 Equivalent Gates



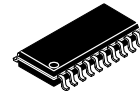
MC74VHCT240A



DW SUFFIX
20-LEAD SOIC PACKAGE
CASE 751D-04



DT SUFFIX
20-LEAD TSSOP PACKAGE
CASE 948E-02

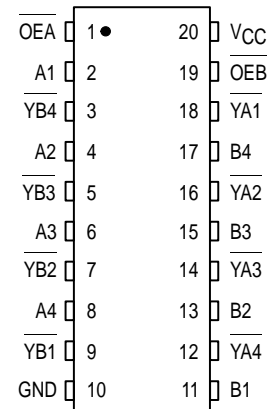


M SUFFIX
20-LEAD SOIC EIAJ PACKAGE
CASE 967-01

ORDERING INFORMATION

| | |
|----------------|-----------|
| MC74VHCTXXXADW | SOIC |
| MC74VHCTXXXADT | TSSOP |
| MC74VHCTXXXAM | SOIC EIAJ |

PIN ASSIGNMENT



FUNCTION TABLE

| INPUTS | | OUTPUTS |
|----------|------|---------|
| OEA, OEB | A, B | YA, YB |
| L | L | H |
| L | H | L |
| H | X | Z |



MC74VHCT240A

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|------------------|--|--|------|
| V _{CC} | DC Supply Voltage | - 0.5 to + 7.0 | V |
| V _{in} | DC Input Voltage | - 0.5 to + 7.0 | V |
| V _{out} | DC Output Voltage Output in 3-State High or Low State | - 0.5 to + 7.0 - 0.5 to V _{CC} + 0.5 | V |
| I _{IK} | Input Diode Current | - 20 | mA |
| I _{OK} | Output Diode Current (V _{OUT} < GND; V _{OUT} > V _{CC}) | ± 20 | mA |
| I _{out} | DC Output Current, per Pin | ± 25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ± 75 | mA |
| P _D | Power Dissipation in Still Air, SOIC Packages† TSSOP Package† | 500 450 | mW |
| T _{stg} | Storage Temperature | - 65 to + 150 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

† Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---------------------------------|---|--------|------------------------|------|
| V _{CC} | DC Supply Voltage | 4.5 | 5.5 | V |
| V _{in} | DC Input Voltage | 0 | 5.5 | V |
| V _{out} | DC Output Voltage Output in 3-State High or Low State | 0 0 | 5.5 V _{CC} | V |
| T _A | Operating Temperature | - 40 | + 85 | °C |
| t _r , t _f | Input Rise and Fall Time V _{CC} = 5.0V ± 0.5V | 0 | 20 | ns/V |

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} V | T _A = 25°C | | | T _A = - 40 to 85°C | | Unit |
|-----------------|---|---|----------------------|-----------------------|-----|--------|-------------------------------|-------|------|
| | | | | Min | Typ | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 4.5 to 5.5 | 2.0 | | | 2.0 | | V |
| V _{IL} | Maximum Low-Level Input Voltage | | 4.5 to 5.5 | | | 0.8 | | 0.8 | V |
| V _{OH} | Minimum High-Level Output Voltage V _{in} = V _{IH} or V _{IL} | I _{OH} = - 50μA | 4.5 | 4.4 | 4.5 | | 4.4 | | V |
| | | I _{OH} = - 8mA | 4.5 | 3.94 | | | 3.80 | | |
| V _{OL} | Maximum Low-Level Output Voltage V _{in} = V _{IH} or V _{IL} | I _{OL} = 50μA | 4.5 | | 0.0 | 0.1 | | 0.1 | V |
| | | I _{OL} = 8mA | 4.5 | | | 0.36 | | 0.44 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = 5.5 V or GND | 0 to 5.5 | | | ± 0.1 | | ± 1.0 | μA |
| I _{OZ} | Maximum 3-State Leakage Current | V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND | 5.5 | | | ± 0.25 | | ± 2.5 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{in} = V _{CC} or GND | 5.5 | | | 4.0 | | 40.0 | μA |

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} V | T _A = 25°C | | | T _A = -40 to 85°C | | Unit |
|-------------------|--------------------------|--|----------------------|-----------------------|-----|------|------------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | |
| I _{CC} T | Quiescent Supply Current | Per Input: V _{IN} = 3.4V Other Input: V _{CC} or GND | 5.5 | | | 1.35 | | 1.50 | mA |
| I _{OP} D | Output Leakage Current | V _{OUT} = 5.5V | 0 | | | 0.5 | | 5.0 | μA |

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A = -40 to 85°C | | Unit |
|---|---|--|-----------------------|------------|--------------|------------------------------|--------------|------|
| | | | Min | Typ | Max | Min | Max | |
| t _{PL} H, t _{PH} L | Maximum Propagation Delay A to YA or B to YB | V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF | | 5.6 6.1 | 7.8 8.8 | 1.0 1.0 | 9.0 10.0 | ns |
| t _{PZ} L, t _{PZ} H | Output Enable Time OEA to YA or OEB to YB | V _{CC} = 5.0 ± 0.5V R _L = 1kΩ C _L = 50pF | | 7.7 8.2 | 10.4 11.4 | 1.0 1.0 | 12.0 13.0 | ns |
| t _{PL} Z, t _{PH} Z | Output Disable Time OEA to YA or OEB to YB | V _{CC} = 5.0 ± 0.5V R _L = 1kΩ C _L = 50pF | | 8.8 | 11.4 | 1.0 | 13.0 | ns |
| t _{OS} LH, t _{OS} HL | Output to Output Skew | V _{CC} = 5.0 ± 0.5V C _L = 50pF (Note 1.) | | | 1.0 | | 1.0 | pF |
| C _{in} | Maximum Input Capacitance | | | 4 | 10 | | 10 | pF |
| C _{out} | Maximum Three-State Output Capacitance (Output in High-Impedance State) | | | 9 | | | | pF |

| | | | | |
|-----------------|---|--|--|----|
| C _{PD} | Power Dissipation Capacitance (Note 2.) | Typical @ 25°C, V _{CC} = 5.0V | | pF |
| | | 19 | | |

- Parameter guaranteed by design. t_{OS}LH = |t_{PL}H_m - t_{PL}H_n|, t_{OS}HL = |t_{PH}L_m - t_{PH}L_n|.
- C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC}(OPR) = C_{PD} • V_{CC} • f_{in} + I_{CC}/8 (per bit). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

| Symbol | Parameter | T _A = 25°C | | Unit |
|-------------------------------|--|-----------------------|------|------|
| | | Typ | Max | |
| V _{OL} P | Quiet Output Maximum Dynamic V _{OL} | 0.9 | 1.1 | V |
| V _{OL} V | Quiet Output Minimum Dynamic V _{OL} | -0.9 | -1.1 | V |
| V _I H _D | Minimum High Level Dynamic Input Voltage | | 2.0 | V |
| V _I L _D | Maximum Low Level Dynamic Input Voltage | | 0.8 | V |

SWITCHING WAVEFORMS

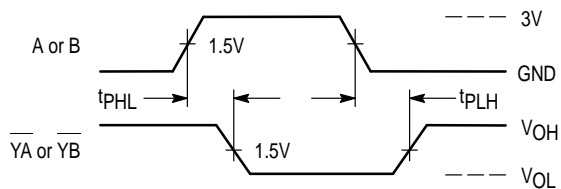


Figure 1.

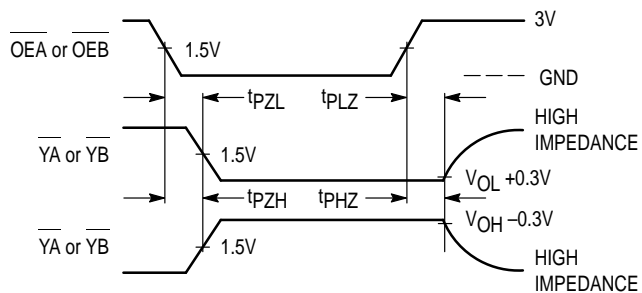
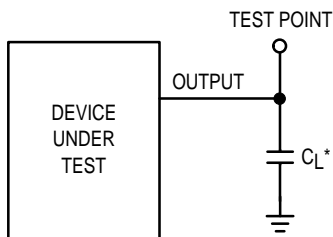


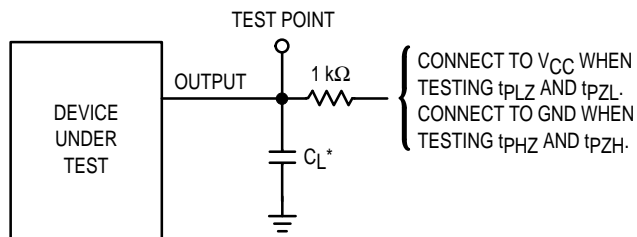
Figure 2.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 3. Test Circuit



* Includes all probe and jig capacitance

Figure 4. Test Circuit

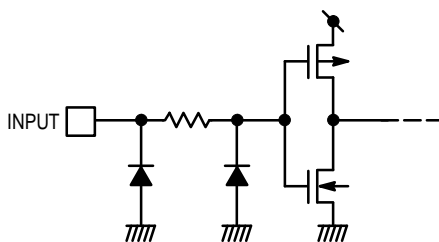
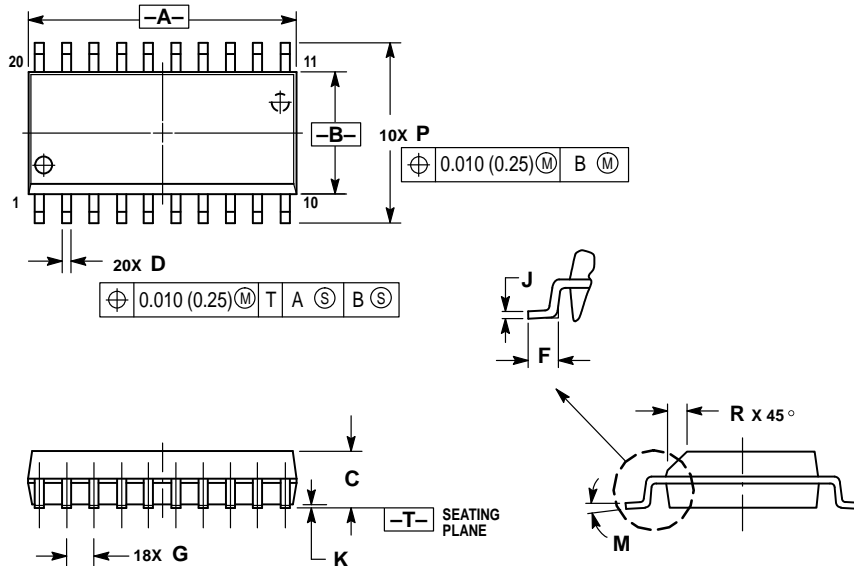


Figure 5. Input Equivalent Circuit

OUTLINE DIMENSIONS

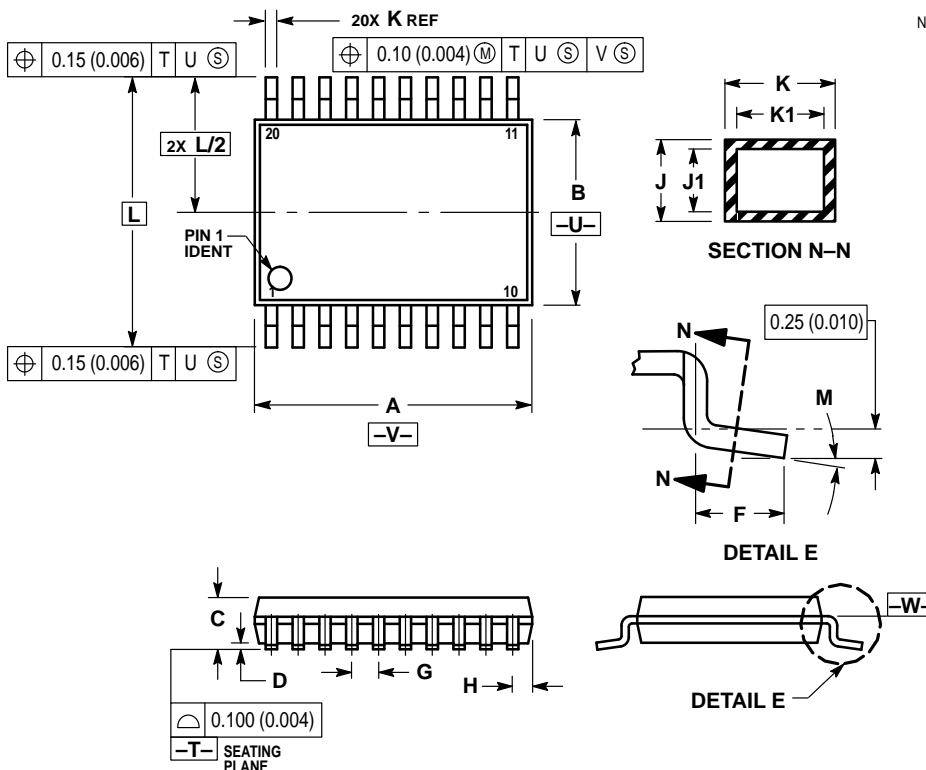
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-04
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 12.65 | 12.95 | 0.499 | 0.510 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.50 | 0.90 | 0.020 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.25 | 0.32 | 0.010 | 0.012 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E-02
ISSUE A

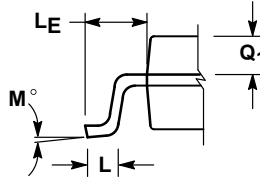
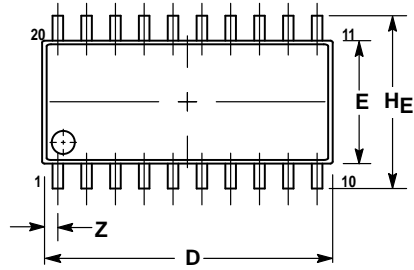


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

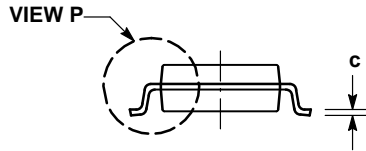
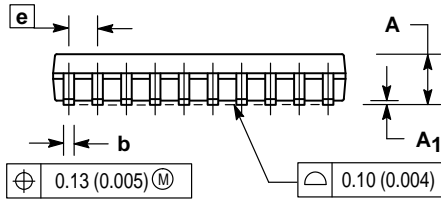
| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | — | 1.20 | — | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

OUTLINE DIMENSIONS

M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 967-01
ISSUE O




DETAIL P



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | — | 2.05 | — | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 12.35 | 12.80 | 0.486 | 0.504 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° | 10° | 0° | 10° |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | — | 0.81 | — | 0.032 |

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