MC74VHC595

8-Bit Shift Register with Output Storage Register
(3-State)

The MC74VHC595 is an advanced high speed 8−bit shift register with an output storage register fabricated with silicon gate CMOS technology.

It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC595 contains an 8−bit static shift register which feeds an 8−bit storage register.

Shift operation is accomplished on the positive going transition of the Shift Clock input (SCK). The output register is loaded with the contents of the shift register on the positive going transition of the Register Clock input (RCK). Since the RCK and SCK signals are independent, parallel outputs can be held stable during the shift operation. And, since the parallel outputs are 3−state, the VHC595 can be directly connected to an 8−bit bus. This register can be used in serial−to−parallel conversion, data receivers, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.
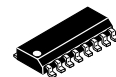
Features

- High Speed: f_{max} = 185 MHz (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 1.0 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
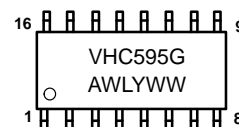- These Devices are Pb−Free and are RoHS Compliant

ON Semiconductor®

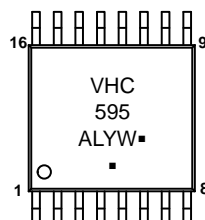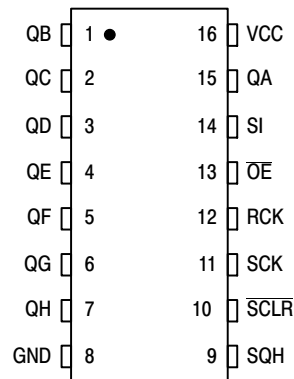### MARKING DIAGRAMS

SOIC−16
D SUFFIX
CASE 751B

```
16            9
VHC595G
AWLYWW
1             8
```

TSSOP−16
DT SUFFIX
CASE 948F

```
16            9
VHC
595
ALYW■
1             8
```

A	= Assembly Location
WL	= Wafer Lot
Y	= Year
W, WW	= Work Week
G or ■	= Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT

QB	1 ●	16	VCC
QC	2	15	QA
QD	3	14	SI
QE	4	13	$\overline{OE}$
QF	5	12	RCK
QG	6	11	SCK
QH	7	10	$\overline{SCLR}$
GND	8	9	SQH

ORDERING INFORMATION

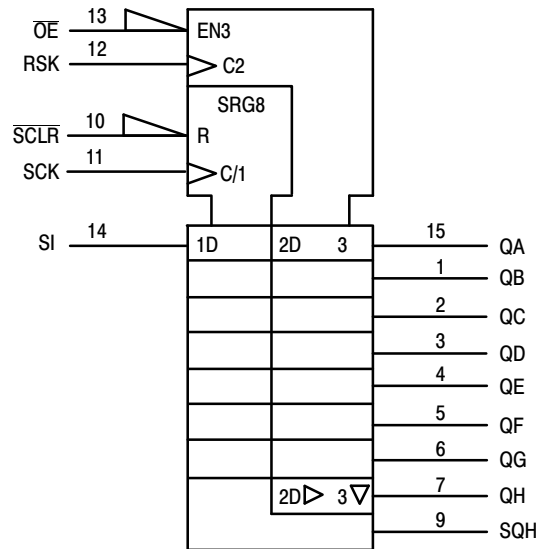| Device	Package	Shipping[†]
MC74VHC595DR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74VHC595DTR2G, NLV74VHC595DTR2G	TSSOP−16 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
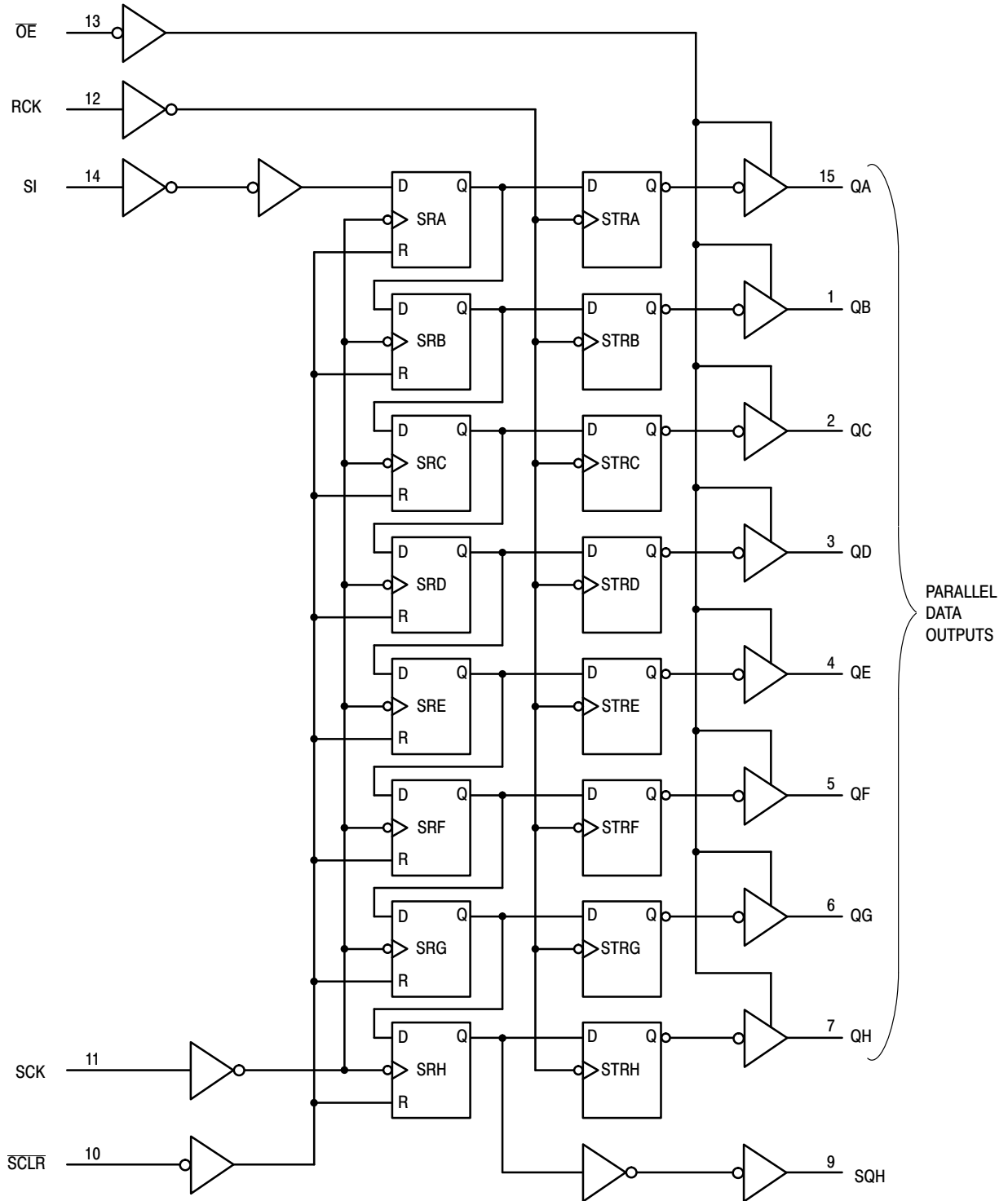
MC74VHC595

LOGIC DIAGRAM

SERIAL DATA INPUT { SI — 14

SHIFT REGISTER

STORAGE REGISTER

15 QA
1 QB
2 QC
3 QD
4 QE
5 QF
6 QG
7 QH

PARALLEL DATA OUTPUTS

SCK — 11

$\overline{SCLR}$ — 10

RCK — 12

$\overline{OE}$ — 13

9 SQH } SERIAL DATA OUTPUT

IEC LOGIC SYMBOL

$\overline{OE}$ — 13 — EN3

RSK — 12 — C2

SRG8

$\overline{SCLR}$ — 10 — R

SCK — 11 — C/1

SI — 14 — 1D   2D   3

15 QA
1 QB
2 QC
3 QD
4 QE
5 QF
6 QG

2D   3   7 QH
9 SQH
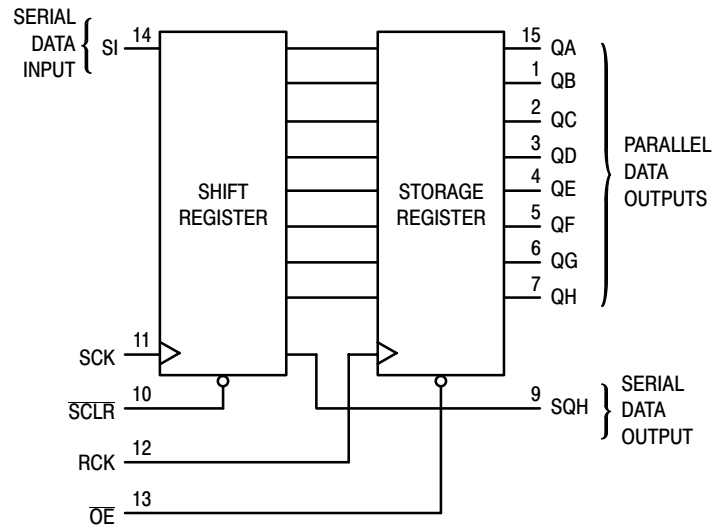
MC74VHC595

EXPANDED LOGIC DIAGRAM

PARALLEL
DATA
OUTPUTS

www.onsemi.com

3

MC74VHC595

FUNCTION TABLE

Operation	Inputs					Resulting Function			
	Reset ($\overline{\text{SCLR}}$)	Serial Input (SI)	Shift Clock (SCK)	Reg Clock (RCK)	Output Enable ($\overline{\text{OE}}$)	Shift Register Contents	Storage Register Contents	Serial Output (SQH)	Parallel Outputs (QA – QH)
Clear shift register	L	X	X	L, H, ↓	L	L	U	L	U
Shift data into shift register	H	D	↑	L, H, ↓	L	D→SR$_A$; SR$_N$→SR$_{N+1}$	U	SR$_G$→SR$_H$	U
Registers remains unchanged	H	X	L, H, ↓	X	L	U	**	U	**
Transfer shift register contents to storage register	H	X	L, H, ↓	↑	L	U	SR$_N$→STR$_N$	*	SR$_N$
Storage register remains unchanged	X	X	X	L, H, ↓	L	*	U	*	U
Enable parallel outputs	X	X	X	X	L	*	**	*	Enabled
Force outputs into high impedance state	X	X	X	X	H	*	**	*	Z

SR = shift register contents   D = data (L, H) logic level   ↓ = High–to–Low   * = depends on Reset and Shift Clock inputs
STR = storage register contents   U = remains unchanged   ↑ = Low–to–High   ** = depends on Register Clock input

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
                 TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{in}	DC Input Voltage	0	5.5	V
V_{out}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0
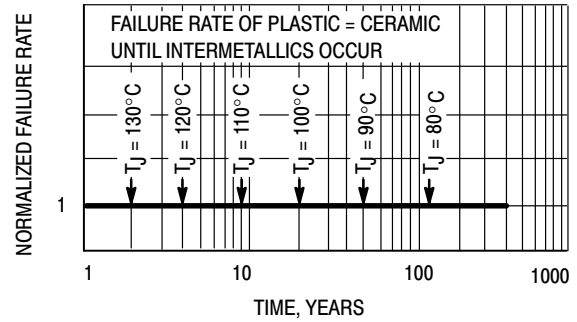
Figure 1. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	$T_A = 25°C$ Min	Typ	Max	$T_A = \leq 85°C$ Min	Max	$T_A = \leq 125°C$ Min	Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 4.5 5.5			0.59 0.9 1.35 1.65		0.59 0.9 1.35 1.65		0.59 0.9 1.35 1.65	V
V_{OH}	Minimum High–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -50\ \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4\ mA$ $I_{OH} = -8\ mA$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V_{OL}	Maximum Low–Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 50\ \mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OL} = 4\ mA$ $I_{OL} = 8\ mA$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I_{IN}	Maximum Input Leakage Current	$V_{IN} = 5.5\ V$ or GND	0 to 5.5			± 0.1		± 1.0		± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND	5.5			4.0		40.0		40.0	μA
I_{OZ}	Three–State Output Off–State Current	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5			± 0.25		± 2.5		± 2.5	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$			$T_A = \leq 85°C$		$T_A = \leq 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 3.3 \pm 0.3$ V		80	150		70		70		MHz
		$V_{CC} = 5.0 \pm 0.5$ V		135	185		115		115		
t_{PLH}, t_{PHL}	Propagation Delay, SCK to SQH	$V_{CC} = 3.3 \pm 0.3$ V	$C_L = 15$pF $C_L = 50$pF		8.8 11.3	13.0 16.5	1.0 1.0	15.0 18.5	1.0 1.0	15.0 18.5	ns
		$V_{CC} = 5.0 \pm 0.5$ V	$C_L = 15$pF $C_L = 50$pF		6.2 7.7	8.2 10.2	1.0 1.0	9.4 11.4	1.0 1.0	9.4 11.4	
t_{PHL}	Propagation Delay, $\overline{CPLR}$ to SQH	$V_{CC} = 3.3 \pm 0.3$ V	$C_L = 15$pF $C_L = 50$pF		8.4 10.9	12.8 16.3	1.0 1.0	13.7 17.2	1.0 1.0	13.7 17.2	ns
		$V_{CC} = 5.0 \pm 0.5$ V	$C_L = 15$pF $C_L = 50$pF		5.9 7.4	8.0 10.0	1.0 1.0	9.1 11.1	1.0 1.0	9.1 11.1	
t_{PLH}, t_{PHL}	Propagation Delay, RCK to QA–QH	$V_{CC} = 3.3 \pm 0.3$ V	$C_L = 15$pF $C_L = 50$pF		7.7 10.2	11.9 15.4	1.0 1.0	13.5 17.0	1.0 1.0	13.5 17.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V	$C_L = 15$pF $C_L = 50$pF		5.4 6.9	7..4 9.4	1.0 1.0	8.5 10.5	1.0 1.0	8.5 10.5	
t_{PZL}, t_{PZH}	Output Enable Time, $\overline{OE}$ to QA–QH	$V_{CC} = 3.3 \pm 0.3$ V $R_L = 1$ kΩ	$C_L = 15$pF $C_L = 50$pF		7.5 9.0	11.5 15.0	1.0 1.0	13.5 17.0	1.0 1.0	13.5 17.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V $R_L = 1$ kΩ	$C_L = 15$pF $C_L = 50$pF		4.8 8.3	8.6 10.6	1.0 1.0	10.0 12.0	1.0 1.0	10.0 12.0	
t_{PLZ}, t_{PHZ}	Output Disable Time, $\overline{OE}$ to QA–QH	$V_{CC} = 3.3 \pm 0.3$ V $R_L = 1$ kΩ	$C_L = 50$pF		12.1	15.7	1.0	16.2	1.0	16.2	ns
		$V_{CC} = 5.0 \pm 0.5$ V $R_L = 1$ kΩ	$C_L = 50$pF		7.6	10.3	1.0	11.0	1.0	11.0	
C_{IN}	Input Capacitance				4	10		10		10	pF
C_{OUT}	Three–State Output Capacitance (Output in High–Impedance State), QA–QH				6			10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0$V	
C_{PD}	Power Dissipation Capacitance (Note 1)	87	pF

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 5.0$V)

Symbol	Characteristic	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.8	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.8	– 1.0	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

MC74VHC595

TIMING REQUIREMENTS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	V_{CC} V	T_A = 25°C		T_A = − 40 to 85°C	T_A = − 55 to 125°C	Unit
			Typ	Limit	Limit	Limit	
t_{su}	Setup Time, SI to SCK	3.3 5.0		3.5 3.0	3.5 3.0	3.5 3.0	ns
$t_{su(H)}$	Setup Time, SCK to RCK	3.3 5.0		8.0 5.0	8.5 5.0	8.5 5.0	ns
$t_{su(L)}$	Setup Time, $\overline{SCLR}$ to RCK	3.3 5.0		8.0 5.0	9.0 5.0	9.0 5.0	ns
t_h	Hold Time, SI to SCK	3.3 5.0		1.5 2.0	1.5 2.0	1.5 2.0	ns
$t_{h(L)}$	Hold Time, $\overline{SCLR}$ to RCK	3.3 5.0		0 0	0 0	1.0 1.0	ns
t_{rec}	Recovery Time, $\overline{SCLR}$ to SCK	3.3 5.0		3.0 2.5	3.0 2.5	3.0 2.5	ns
t_w	Pulse Width, SCK or RCK	3.3 5.0		5.0 5.0	5.0 5.0	5.0 5.0	ns
$t_{w(L)}$	Pulse Width, $\overline{SCLR}$	3.3 5.0		5.0 5.0	5.0 5.0	5.0 5.0	ns

SWITCHING WAVEFORMS
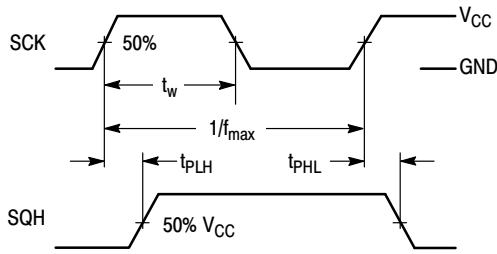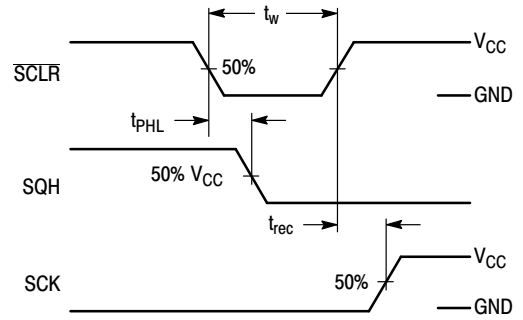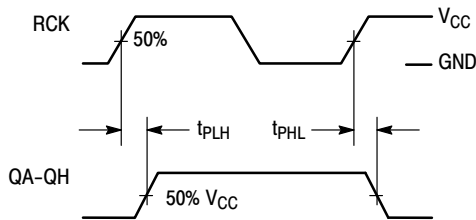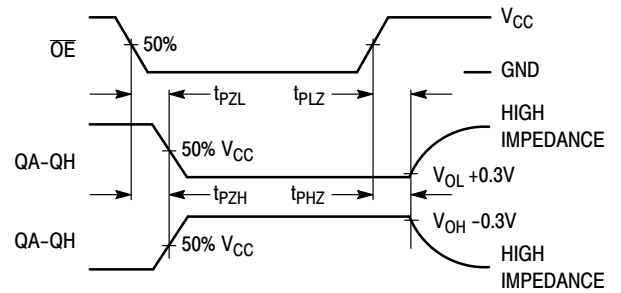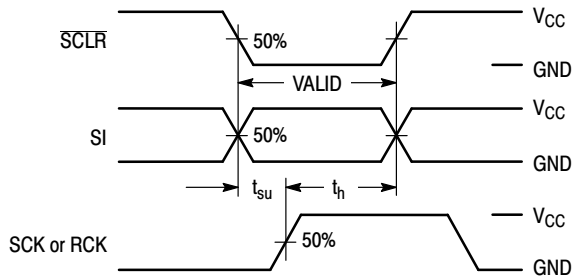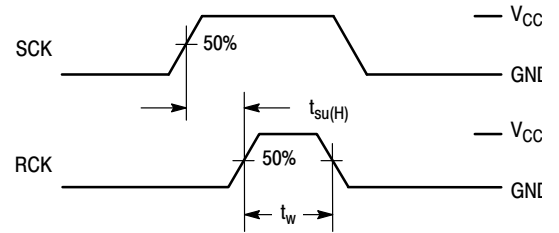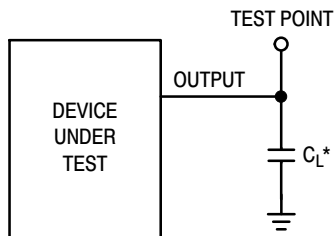
SCK
50%
V_{CC}
GND
t_w
$1/f_{max}$
t_{PLH}
t_{PHL}
SQH
50% V_{CC}

Figure 2.

t_w
$\overline{SCLR}$
50%
V_{CC}
GND
t_{PHL}
SQH
50% V_{CC}
t_{rec}
SCK
50%
V_{CC}
GND

Figure 3.

RCK
50%
V_{CC}
GND
t_{PLH}
t_{PHL}
QA–QH
50% V_{CC}

Figure 4.

$\overline{OE}$
50%
V_{CC}
GND
t_{PZL}
t_{PLZ}
HIGH IMPEDANCE
QA–QH
50% V_{CC}
V_{OL} +0.3V
t_{PZH}
t_{PHZ}
V_{OH} –0.3V
QA–QH
50% V_{CC}
HIGH IMPEDANCE

Figure 5.

$\overline{SCLR}$
50%
V_{CC}
GND
VALID
V_{CC}
SI
50%
GND
t_{su}
t_h
V_{CC}
SCK or RCK
50%
GND

Figure 6.

SCK
50%
V_{CC}
GND
$t_{su(H)}$
V_{CC}
RCK
50%
GND
t_w

Figure 7.

TEST CIRCUITS

TEST POINT
OUTPUT
DEVICE UNDER TEST
C_L*

*Includes all probe and jig capacitance

Figure 8.

TEST POINT
OUTPUT
1 kΩ
DEVICE UNDER TEST
C_L*
CONNECT TO V_{CC} WHEN TESTING t_{PLZ} AND t_{PZL}.
CONNECT TO GND WHEN TESTING t_{PHZ} AND t_{PZH}.
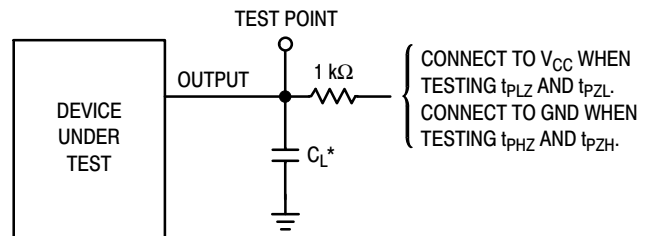
*Includes all probe and jig capacitance

Figure 9.

MC74VHC595

TIMING DIAGRAM
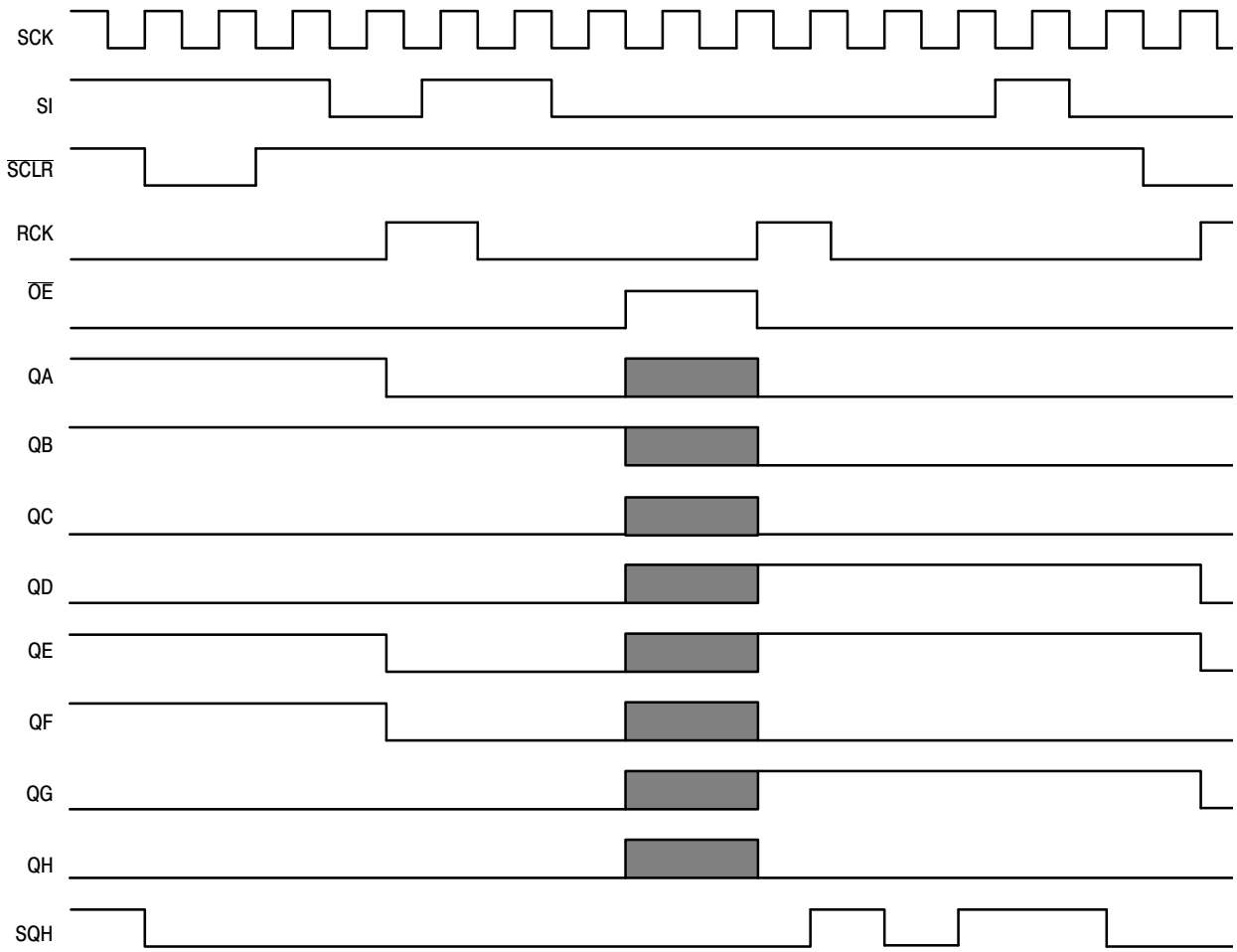
NOTE: ▊ output is in a high−impedance state.

INPUT EQUIVALENT CIRCUIT
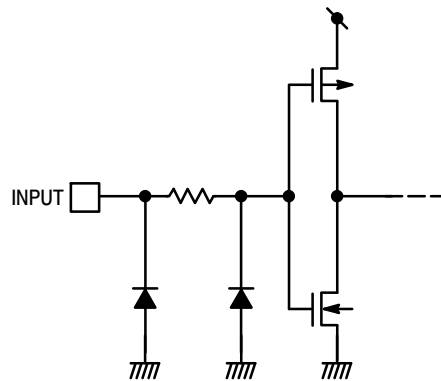
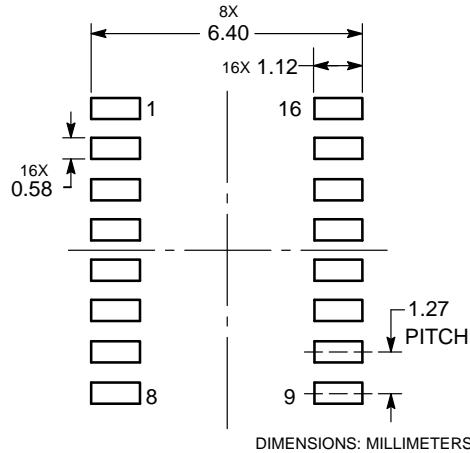# MC74VHC595

PACKAGE DIMENSIONS

TSSOP−16
CASE 948F
ISSUE B
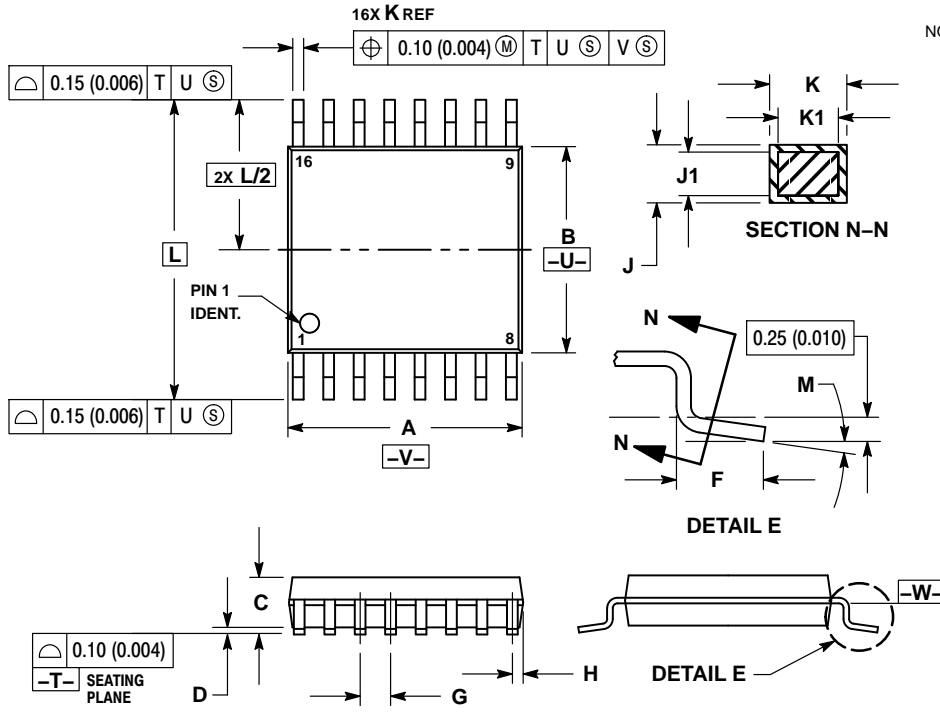
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*
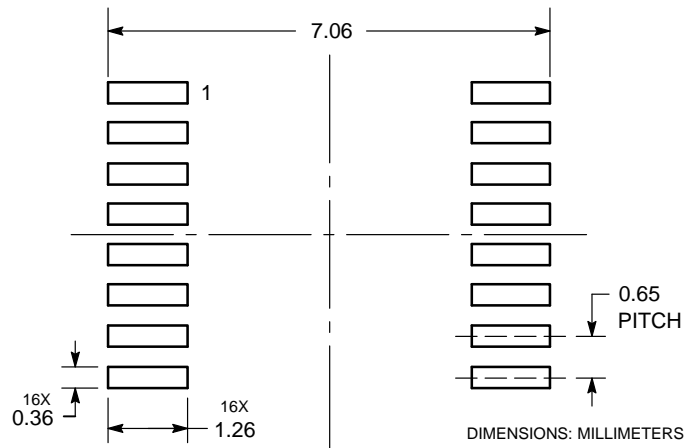
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74VHC595

PACKAGE DIMENSIONS

SOIC–16
CASE 751B–05
ISSUE K
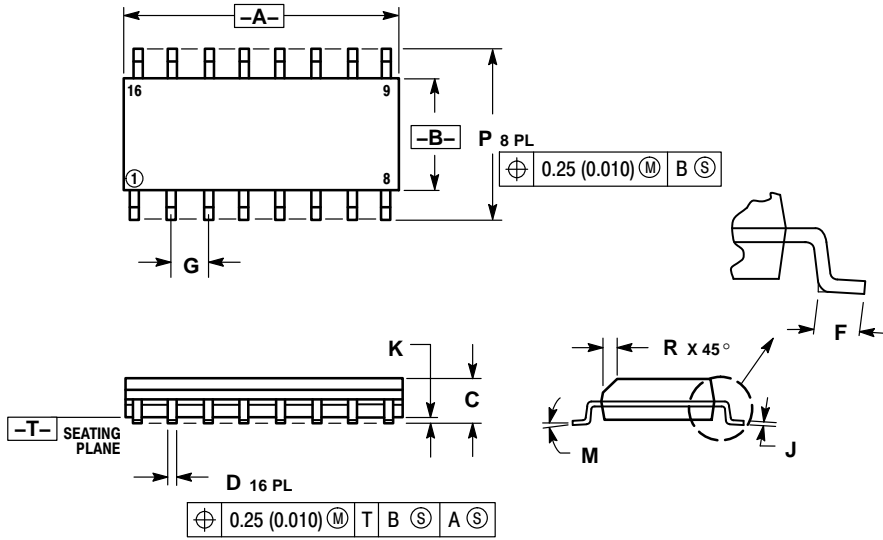
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74VHC595/D