# **Octal Bus Buffer**

# Inverting

The MC74VHC540 is an advanced high speed CMOS inverting octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC540 features inputs and outputs on opposite sides of the package and two AND-ed active-low output enables. When either OE1 or OE2 are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

#### **Features**

- High Speed:  $t_{PD} = 3.7 \text{ ns}$  (Typ) at  $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 4.0 \mu A$  (Max) at  $T_A = 25^{\circ}C$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: V<sub>OLP</sub> = 1.2 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 124 FETs or 31 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

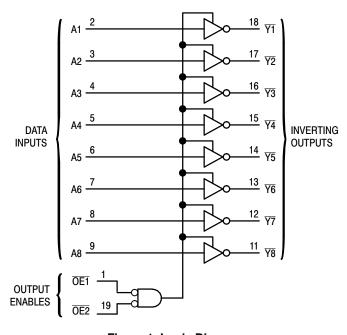


Figure 1. Logic Diagram



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#### **MARKING DIAGRAMS**









2

= Assembly Location WL, L = Wafer Lot

YY, Y = Year WW, W = Work Week G or ■ = Pb-Free Package

#### **PIN ASSIGNMENT**

OE1	1●	20	] v <sub>cc</sub>
A1 [	2	19	OE2
A2 [	3	18	] <u>Y1</u>
A3 [	4	17	] <u>Y2</u>
A4 [	5	16	] <u>Y3</u>
A5 [	6	15	□ <u>Y4</u>
A6 [	7	14	] Y5
A7 [	8	13	□ <u>Y</u> 6
A8 [	9	12	] <del>Y</del> 7
GND [	10	11	] <u>Y8</u>

## **FUNCTION TABLE**

	Inputs		Output <del>Y</del>
OE1	OE2	Α	Output 1
L	L	L	Н
L	L	Н	L.
Н	X	Х	Z
X	Н	Х	Z

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

#### **MAXIMUM RATINGS\***

Symbol	Parameter	r	Value	Unit
V <sub>CC</sub>	DC Supply Voltage		- 0.5 to + 7.0	V
V <sub>in</sub>	DC Input Voltage		- 0.5 to + 7.0	V
V <sub>out</sub>	DC Output Voltage	- 0.5 to V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input Diode Current	- 20	mA	
I <sub>OK</sub>	Output Diode Current	± 20	mA	
I <sub>out</sub>	DC Output Current, per Pin		± 25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GN	ID Pins	± 75	mA
P <sub>D</sub>	Power Dissipation in Still Air,	SOIC Packages† TSSOP Package†	500 450	mW
T <sub>stg</sub>	Storage Temperature		- 65 to + 150	°C

<sup>\*</sup> Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C TSSOP Package: – 6.1 mW/°C from 65° to 125°C

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter			Max	Unit
V <sub>CC</sub>	DC Supply Voltage		2.0	5.5	V
V <sub>in</sub>	DC Input Voltage			5.5	V
V <sub>out</sub>	DC Output Voltage			$V_{CC}$	V
T <sub>A</sub>	Operating Temperature, All Package Types			+ 125	°C
t <sub>r</sub> , t <sub>f</sub>	•	$V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	0	100 20	ns/V

### DC ELECTRICAL CHARACTERISTICS

			V <sub>CC</sub>	V <sub>CC</sub> T <sub>A</sub> = 25°C		;	T <sub>A</sub> = - 55	to 125°C	
Symbol	Parameter	Test Conditions	V	Min	Тур	Max	Min	Max	Unit
V <sub>IH</sub>	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 V <sub>CC</sub> x 0.7			1.50 V <sub>CC</sub> x 0.7		٧
V <sub>IL</sub>	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 V <sub>CC</sub> x 0.3		0.50 V <sub>CC</sub> x 0.3	٧
V <sub>OH</sub>	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		٧
		$V_{in} = V_{IH} \text{ or } V_{IL} \\ I_{OH} = -4mA \\ I_{OH} = -8mA$	3.0 4.5	2.58 3.94			2.48 3.80		
V <sub>OL</sub>	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu A$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	٧
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5			0.36 0.36		0.44 0.44	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range GND  $\leq$  ( $V_{in}$  or  $V_{out}$ )  $\leq$   $V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

#### DC ELECTRICAL CHARACTERISTICS

		V <sub>cc</sub>		V <sub>20</sub> T <sub>A</sub> = 25°C		T <sub>A</sub> = - 55 to 125°C			
Symbol	Parameter	Test Conditions	v	Min	Тур	Max	Min	Max	Unit
l <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μА
l <sub>OZ</sub>	Maximum Three-State Leakage Current	$V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	5.5			± 0.25		± 2.5	μА
Icc	Maximum Quiescent Supply Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5			4.0		40.0	μА

#### AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}$ )

					T <sub>A</sub> = 25°C		T <sub>A</sub> = - 55	5 to 125°C	
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to \( \overline{Y} \)	$V_{CC} = 3.3 \pm 0.3 V$	$C_L = 15pF$ $C_L = 50pF$		4.8 7.3	7.0 10.5	1.0 1.0	8.5 12.0	ns
	(Figures 1 and 3)	$V_{CC} = 5.0 \pm 0.5 V$	$C_L = 15pF$ $C_L = 50pF$		3.7 5.2	5.0 7.0	1.0 1.0	6.0 8.0	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time, OEn to Y	$\begin{aligned} V_{CC} &= 3.3 \pm 0.3 V \\ R_L &= 1 k \Omega \end{aligned}$	$C_L = 15pF$ $C_L = 50pF$		6.8 9.3	10.5 14.0	1.0 1.0	12.5 16.0	ns
	(Figures 2 and 4)	$V_{CC} = 5.0 \pm 0.5V$ $R_L = 1k\Omega$	$C_L = 15pF$ $C_L = 50pF$		4.7 6.2	7.2 9.2	1.0 1.0	8.5 10.5	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time, OEn to Y	$\begin{aligned} V_{CC} &= 3.3 \pm 0.3 V \\ R_L &= 1 k \Omega \end{aligned}$	C <sub>L</sub> = 50pF		11.2	15.4	1.0	17.5	ns
	(Figures 2 and 4)	$V_{CC} = 5.0 \pm 0.5V$ $R_L = 1k\Omega$	C <sub>L</sub> = 50pF		6.0	8.8	1.0	10.0	
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output to Output Skew	V <sub>CC</sub> = 3.3 ± 0.3V (Note 1)	C <sub>L</sub> = 50pF			1.5			ns
		V <sub>CC</sub> = 5.0 ± 0.5V (Note 1)	C <sub>L</sub> = 50pF			1.0			ns
C <sub>in</sub>	Maximum Input Capacitance				4	10		10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High Impedance State)				6				pF

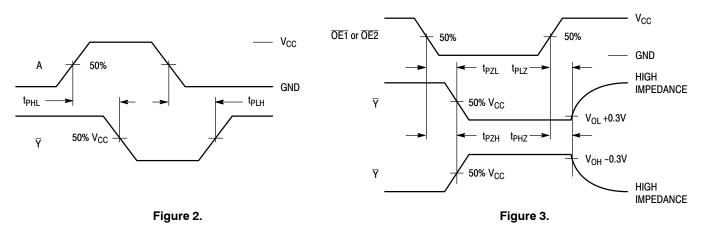
		Typical @ 25°C, V <sub>CC</sub> = 5.0V	
$C_{PD}$	Power Dissipation Capacitance (Note 2)	17	pF

# **NOISE CHARACTERISTICS** (Input $t_r = t_f = 3.0 \text{ns}$ , $C_L = 50 \text{pF}$ , $V_{CC} = 5.0 \text{V}$ )

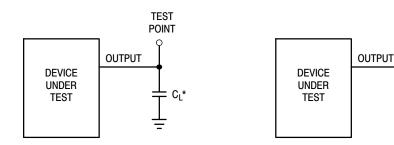
		T <sub>A</sub> = 25°C		
Symbol	Parameter	Тур	Max	Unit
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.9	1.2	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	- 0.9	- 1.2	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		3.5	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		1.5	V

Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|.
 C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/8 (per bit). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

#### **SWITCHING WAVEFORMS**



# **TEST CIRCUITS**



\*Includes all probe and jig capacitance

Figure 4.

\*Includes all probe and jig capacitance

 $\text{1k}\Omega$ 

 $C_{\mathsf{L}}^{\star}$ 

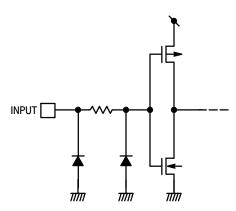
TEST POINT

Figure 5.

CONNECT TO  $V_{CC}$  WHEN TESTING  $t_{PLZ}$  AND  $t_{PZL}$ . CONNECT TO GND WHEN

TESTING  $t_{PHZ}$  AND  $t_{PZH}$ .

# **INPUT EQUIVALENT CIRCUIT**



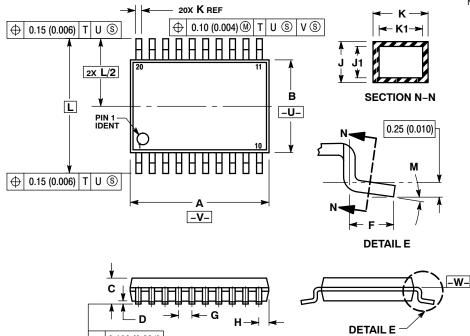
# **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC74VHC540DWR2G	SOIC-20 (Pb-Free)	1000 Units / Tape & Reel
MC74VHC540DTR2G	TSSOP-20 (Pb-Free)	2500 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

#### TSSOP-20 **DT SUFFIX** CASE 948E-02 **ISSUE C**



☐ 0.100 (0.004)

-T- SEATING PLANE

- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION:

  - 2. CONTHOLLING DIMENSION.
    MILLIMETER.
    3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
    MOLD FLASH OR GATE BURRS SHALL NOT

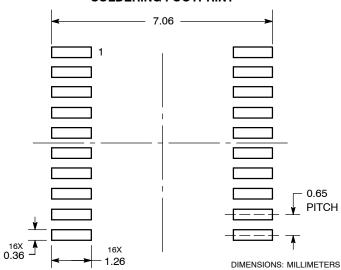
  - MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
    4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
    5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  - CONDITION.

    6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

    7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

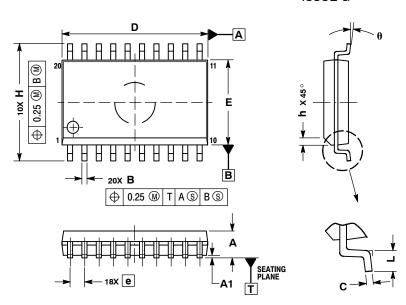
	MILLIMETERS		INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	6.40	6.60	0.252	0.260	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.27	0.37	0.011	0.015	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L		6.40 BSC		BSC	
M	0°	8°	0°	8°	

#### **SOLDERING FOOTPRINT**



#### PACKAGE DIMENSIONS

#### SOIC-20 **DW SUFFIX** CASE 751D-05 ISSUE G



#### NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
- PROTHUSION.

  MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  DIMENSION B DOES NOT INCLUDE DAMBAR
  PROTRUSION. ALLOWABLE PROTRUSION SHALL
  BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS				
DIM	MIN	MAX			
Α	2.35	2.65			
A1	0.10	0.25			
В	0.35	0.49			
С	0.23	0.32			
D	12.65	12.95			
Е	7.40	7.60			
е	1.27	BSC			
Н	10.05	10.55			
h	0.25	0.75			
L	0.50	0.90			
θ	0 °	7 °			

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