

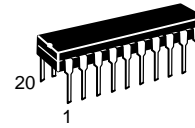
Octal 3-State Inverting Buffer/ Line Driver/Line Receiver with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC74HCT240A is identical in pinout to the LS240. This device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT240A is an octal inverting buffer line driver line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has inverting outputs and two active-low output enables.

The HCT240A is the inverting version of the HCT244. See also HCT241.

- Output Drive Capability: 15 LSTTL Loads
- TTL NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 110 FETs or 27.5 Equivalent Gates

MC74HCT240A



N SUFFIX
PLASTIC PACKAGE
CASE 738-03



DW SUFFIX
SOIC PACKAGE
CASE 751D-04



SD SUFFIX
SSOP PACKAGE
CASE 940C-03

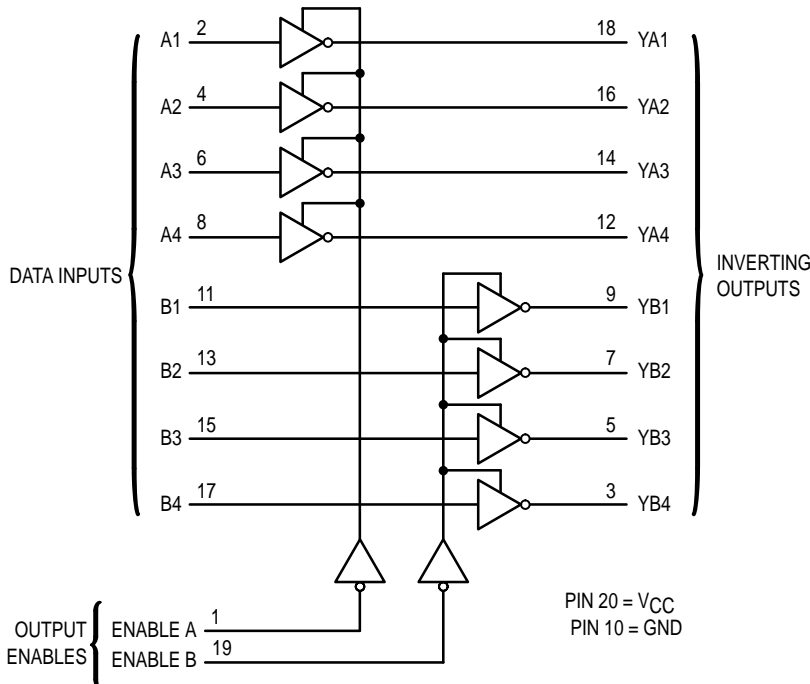


DT SUFFIX
TSSOP PACKAGE
CASE 948E-02

ORDERING INFORMATION

MC74HCTXXXAN	Plastic
MC74HCTXXXADW	SOIC
MC74HCTXXXASD	SSOP
MC74HCTXXXADT	TSSOP

LOGIC DIAGRAM



PIN ASSIGNMENT

ENABLE A	1 ●	20	V _{CC}
A1	2	19	ENABLE B
YB4	3	18	YA1
A2	4	17	B4
YB3	5	16	YA2
A3	6	15	B3
YB2	7	14	YA3
A4	8	13	B2
YB1	9	12	YA4
GND	10	11	B1

FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	H
L	H	L
H	X	Z

Z = High Impedance

X = Don't Care



MC74HCT240A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 35	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 75	mA
P _D	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP or SSOP Package†	750	mW
		500	
		450	
T _{stg}	Storage Temperature	- 65 to + 150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, TSSOP or SSOP Package)	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

TSSOP or SSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	- 55	+ 125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	0	500	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5	2	2	2	V
			5.5	2	2	2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 6 mA	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	4.5	0.26	0.33	0.4	μA
			5.5	± 0.1	± 1.0	± 1.0	
I _{OZ}	Maximum Three State Leakage Current	Output in High-Impedance State V _{in} = V _{IL} or V _{IH} V _{out} = V _{CC} or GND	5.5	± 0.5	± 5.0	± 10	μA

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	5.5	4	40	160	μA
ΔI _{CC}	Additional Quiescent Supply Current	V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs I _{out} = 0 μA	5.5	≥ -55°C	25°C to 125°C		mA
				2.9	2.4		

NOTES:

- Information on typical parametric values along with frequency or heavy load considerations can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Total Supply Current = I_{CC} + ΣΔI_{CC}.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 10%, C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	Guaranteed Limit			Unit
		- 55 to 25°C	≤ 85°C	≤ 125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 3)	20	25	30	ns
t _{PLZ} , t _{PHZ}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	28	35	42	ns
t _{PZL} , t _{PZH}	Maximum Propagation Delay, Output Enable to YA or YB (Figures 2 and 4)	25	31	38	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	12	15	18	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Enabled Output)*	Typical @ 25°C, V _{CC} = 5.0 V		pF
		55		

* Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

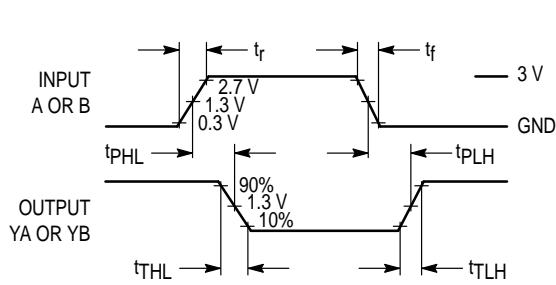


Figure 1.

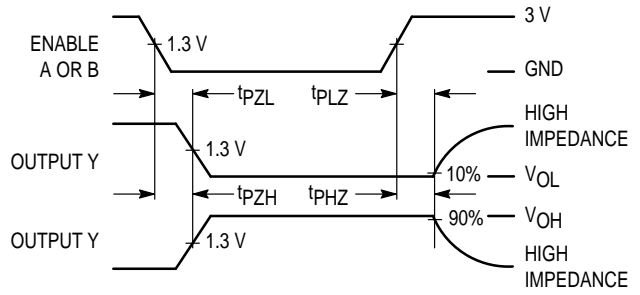
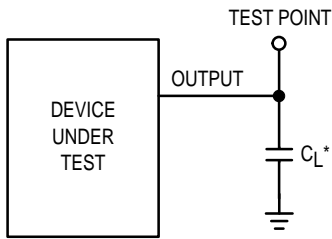
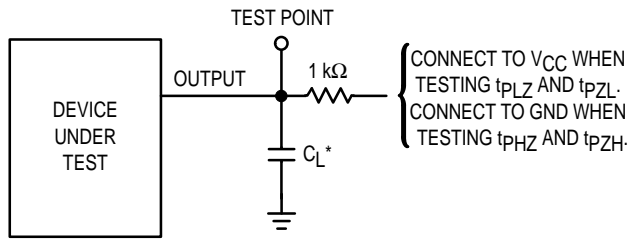


Figure 2.



* Includes all probe and jig capacitance

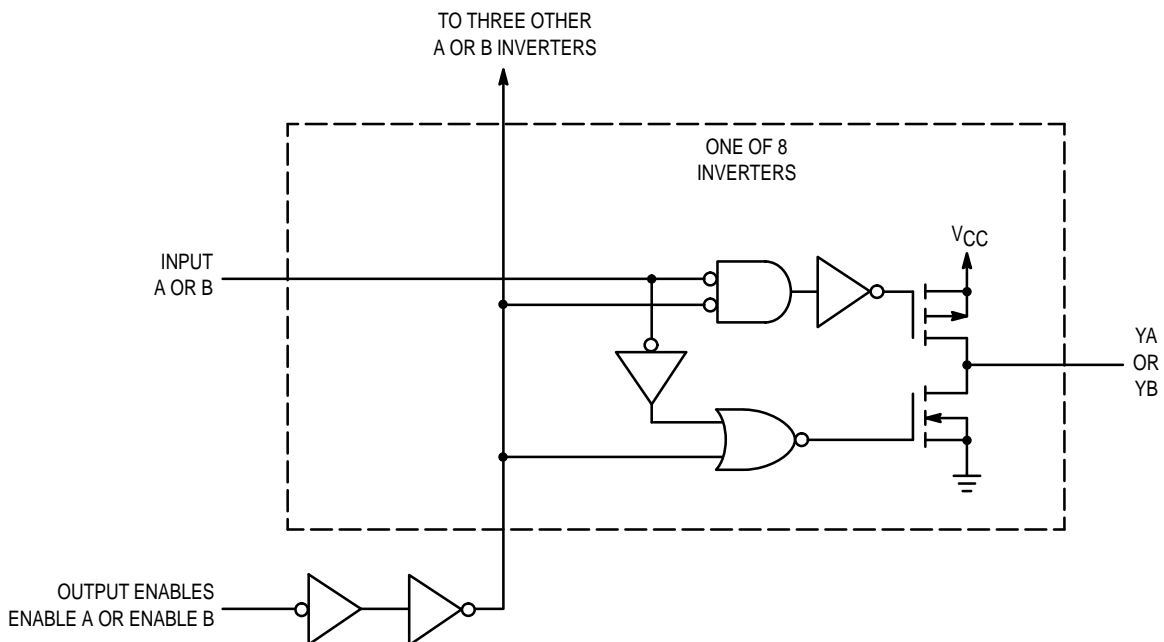
Figure 3. Test Circuit



* Includes all probe and jig capacitance

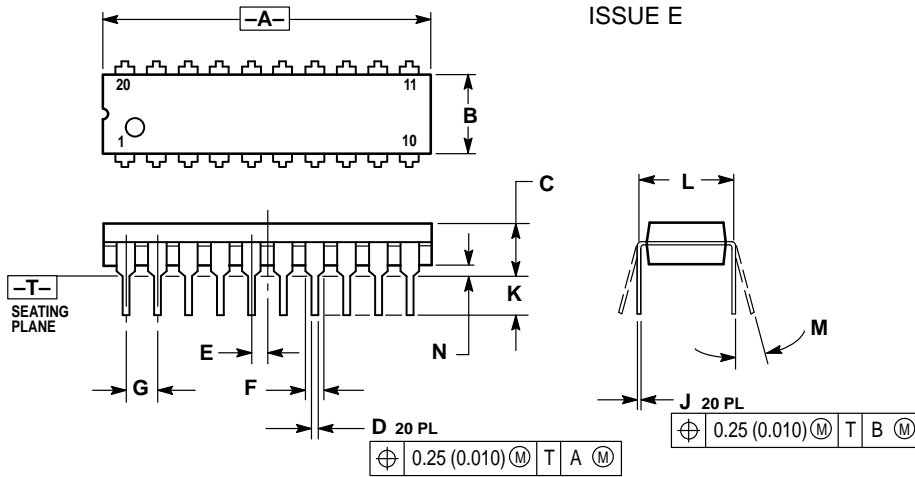
Figure 4. Test Circuit

LOGIC DETAIL



OUTLINE DIMENSIONS

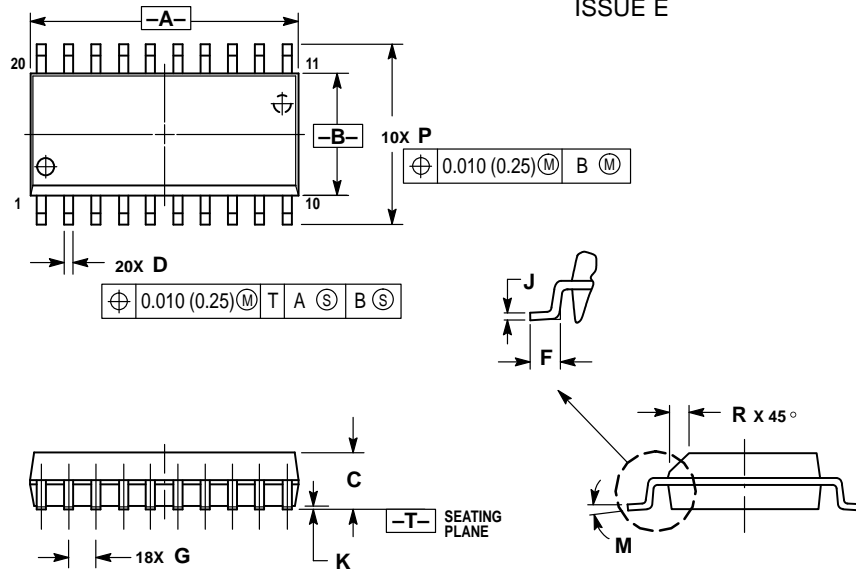
N SUFFIX
PLASTIC PACKAGE
CASE 738-03
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0° - 15°		0° - 15°	
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-04
ISSUE E

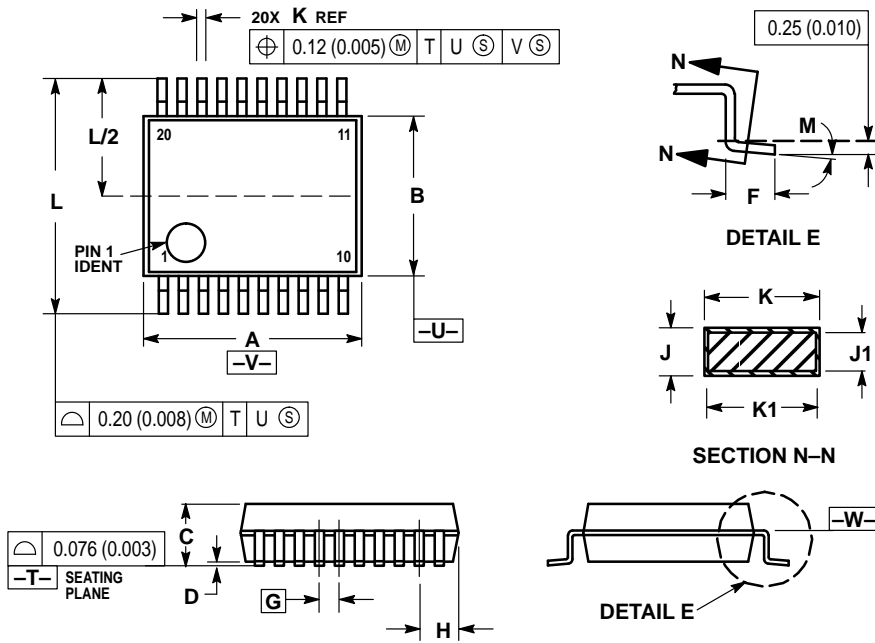


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0° - 7°		0° - 7°	
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

OUTLINE DIMENSIONS

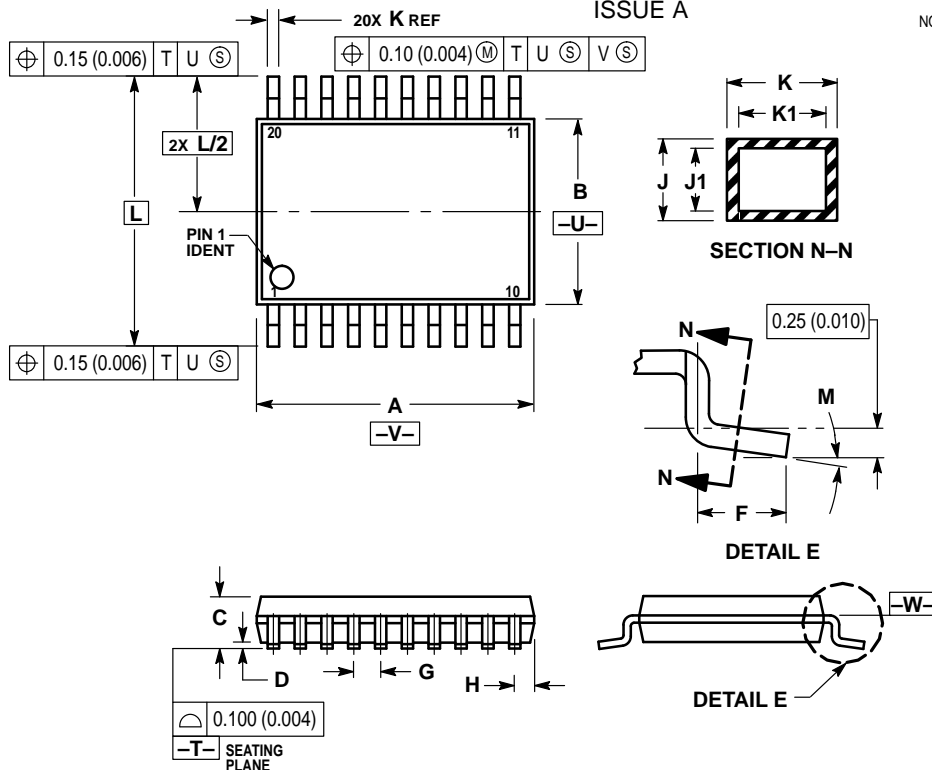
SD SUFFIX
PLASTIC SSOP PACKAGE
CASE 940C-03
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.07	7.33	0.278	0.288
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.59	0.75	0.023	0.030
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E-02
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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