# MC74HC273A

## Octal D Flip-Flop with Common Clock and Reset
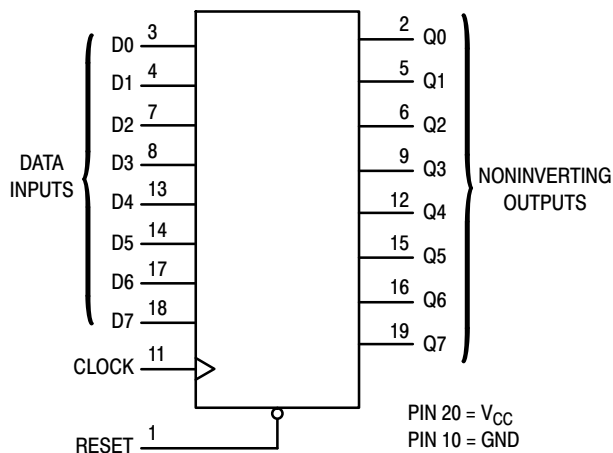
### High−Performance Silicon−Gate CMOS

The MC74HC273A is identical in pinout to the LS273. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of eight D flip−flops with common Clock and Reset inputs. Each flip−flop is loaded with a low−to−high transition of the Clock input. Reset is asynchronous and active low.

**Features**

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 264 FETs or 66 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

## ON Semiconductor®
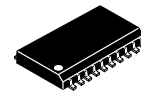
www.onsemi.com

SOIC−20
DW SUFFIX
CASE 751D

TSSOP−20
DT SUFFIX
CASE 948E

### PIN ASSIGNMENT

| | | | |
|---|---|---|---|
| RESET | 1• | 20 | V_CC |
| Q0 | 2 | 19 | Q7 |
| D0 | 3 | 18 | D7 |
| D1 | 4 | 17 | D6 |
| Q1 | 5 | 16 | Q6 |
| Q2 | 6 | 15 | Q5 |
| D2 | 7 | 14 | D5 |
| D3 | 8 | 13 | D4 |
| Q3 | 9 | 12 | Q4 |
| GND | 10 | 11 | CLOCK |

### MARKING DIAGRAMS

20

HC273A
AWLYYWWG

SOIC−20

20

HC
273A
ALYW∎
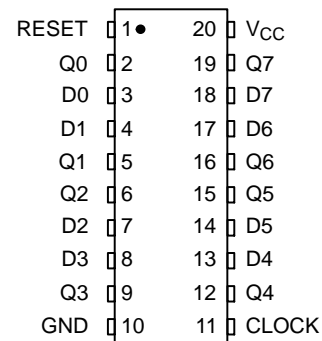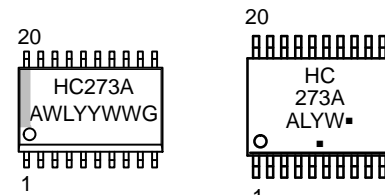
TSSOP−20

| | | |
|---|---|---|
| A | = | Assembly Location |
| WL, L | = | Wafer Lot |
| YY, Y | = | Year |
| WW, W | = | Work Week |
| G or ∎ | = | Pb−Free Package |

(Note: Microdot may be in either location)

### LOGIC DIAGRAM



PIN 20 = V_CC
PIN 10 = GND

| Design Criteria | Value | Units |
|---|---|---|
| Internal Gate Count* | 66 | ea |
| Internal Gate Propagation Delay | 1.5 | ns |
| Internal Gate Power Dissipation | 5.0 | μW |
| Speed Power Product | .0075 | pJ |

*Equivalent to a two−input NAND gate.

### FUNCTION TABLE

| Inputs | | | Output |
|---|---|---|---|
| Reset | Clock | D | Q |
| L | X | X | L |
| H | ⤒ | H | H |
| H | ⤒ | L | L |
| H | L | X | No Change |
| H | ⤓ | X | No Change |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# MC74HC273A

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | −0.5 to +7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | −0.5 to $V_{CC}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | −0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±50 | mA |
| $P_D$ | Power Dissipation in Still Air,          SOIC Package† TSSOP Package† | 500 450 | mW |
| $T_{stg}$ | Storage Temperature | −65 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds          SOIC or TSSOP Package | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
†Derating: SOIC Package: −7 mW/°C from 65° to 125°C
         TSSOP Package: −6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|--------|-----------|-----|-----|------|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1)       $V_{CC}$ = 2.0 V $V_{CC}$ = 4.5 V $V_{CC}$ = 6.0 V | 0 0 0 | 1000 500 400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit −55 to 25°C | ≤ 85°C | ≤ 125°C | Unit |
|--------|-----------|-----------------|-----------|------------------------------|--------|---------|------|
| $V_{IH}$ | Minimum High−Level Input Voltage | $V_{out}$ = $V_{CC}$ − 0.1 V \|$I_{out}$\| ≤ 20 μA | 2.0 3.0 4.5 6.0 | 1.5 2.1 3.15 4.2 | 1.5 2.1 3.15 4.2 | 1.5 2.1 3.15 4.2 | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | $V_{out}$ = 0.1 V \|$I_{out}$\| ≤ 20 μA | 2.0 3.0 4.5 6.0 | 0.5 0.9 1.35 1.8 | 0.5 0.9 1.35 1.8 | 0.5 0.9 1.35 1.8 | V |
| $V_{OH}$ | Minimum High−Level Output Voltage | $V_{in}$ = $V_{IH}$ \|$I_{out}$\| ≤ 20 μA | 2.0 4.5 6.0 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | 1.9 4.4 5.9 | V |
| | | $V_{in}$ = $V_{IH}$       \|$I_{out}$\| ≤ 2.4 mA                 \|$I_{out}$\| ≤ 6.0 mA                 \|$I_{out}$\| ≤ 7.8 mA | 3.0 4.5 6.0 | 2.48 3.98 5.48 | 2.34 3.84 5.34 | 2.2 3.7 5.2 | |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_{in}$ = $V_{IL}$ \|$I_{out}$\| ≤ 20 μA | 2.0 4.5 6.0 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | 0.1 0.1 0.1 | V |
| | | $V_{in}$ = $V_{IL}$       \|$I_{out}$\| ≤ 2.4 mA                 \|$I_{out}$\| ≤ 6.0 mA                 \|$I_{out}$\| ≤ 7.8 mA | 3.0 4.5 6.0 | 0.26 0.26 0.26 | 0.33 0.33 0.33 | 0.4 0.4 0.4 | |

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**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit −55 to 25°C | ≤ 85°C | ≤ 125°C | Unit |
|---|---|---|---|---|---|---|---|
| $I_{in}$ | Maximum Input Leakage Current | $V_{in} = V_{CC}$ or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC}$ or GND $I_{out} = 0$ μA | 6.0 | 4.0 | 40 | 160 | μA |

**AC ELECTRICAL CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6.0 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit −55 to 25°C | ≤ 85°C | ≤ 125°C | Unit |
|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4) | 2.0 3.0 4.5 6.0 | 6.0 15 30 35 | 5.0 10 24 28 | 4.0 8.0 20 24 | MHz |
| $t_{PLH}$ $t_{PHL}$ | Maximum Propagation Delay, Clock to Q (Figures 1 and 4) | 2.0 3.0 4.5 6.0 | 145 90 29 25 | 180 120 36 31 | 220 140 44 38 | ns |
| $t_{PHL}$ | Maximum Propagation Delay, Reset to Q (Figures 2 and 4) | 2.0 3.0 4.5 6.0 | 145 90 29 25 | 180 120 36 31 | 220 140 44 38 | ns |
| $t_{TLH}$ $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 4) | 2.0 3.0 4.5 6.0 | 75 27 15 13 | 95 32 19 16 | 110 36 22 19 | ns |
| $C_{in}$ | Maximum Input Capacitance | | 10 | 10 | 10 | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Enabled Output)* | 48 | pF |

* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

**TIMING REQUIREMENTS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6.0 ns)

| Symbol | Parameter | Figure | $V_{CC}$ Volts | Guaranteed Limit −55 to 25°C Min | Max | ≤ 85°C Min | Max | ≤ 125°C Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{su}$ | Minimum Setup Time, Data to Clock | 3 | 2.0 3.0 4.5 6.0 | 60 23 12 10 | | 75 27 15 13 | | 90 32 18 15 | | ns |
| $t_h$ | Minimum Hold Time, Clock to Data | 3 | 2.0 3.0 4.5 6.0 | 3.0 3.0 3.0 3.0 | | 3.0 3.0 3.0 3.0 | | 3.0 3.0 3.0 3.0 | | ns |
| $t_{rec}$ | Minimum Recovery Time, Reset Inactive to Clock | 2 | 2.0 3.0 4.5 6.0 | 5.0 5.0 5.0 5.0 | | 5.0 5.0 5.0 5.0 | | 5.0 5.0 5.0 5.0 | | ns |
| $t_w$ | Minimum Pulse Width, Clock | 1 | 2.0 3.0 4.5 6.0 | 60 23 12 10 | | 75 27 15 13 | | 90 32 18 15 | | ns |

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**TIMING REQUIREMENTS** ($C_L$ = 50 pF, Input $t_r$ = $t_f$ = 6.0 ns)

| Symbol | Parameter | Figure | $V_{CC}$ Volts | Min | Max | Min | Max | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_w$ | Minimum Pulse Width, Reset | 2 | 2.0 | 60 | | 75 | | 90 | | ns |
| | | | 3.0 | 23 | | 27 | | 32 | | |
| | | | 4.5 | 12 | | 15 | | 18 | | |
| | | | 6.0 | 10 | | 13 | | 15 | | |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times | 1 | 2.0 | | 1000 | | 1000 | | 1000 | ns |
| | | | 3.0 | | 800 | | 800 | | 800 | |
| | | | 4.5 | | 500 | | 500 | | 500 | |
| | | | 6.0 | | 400 | | 400 | | 400 | |

# MC74HC273A

## SWITCHING WAVEFORMS
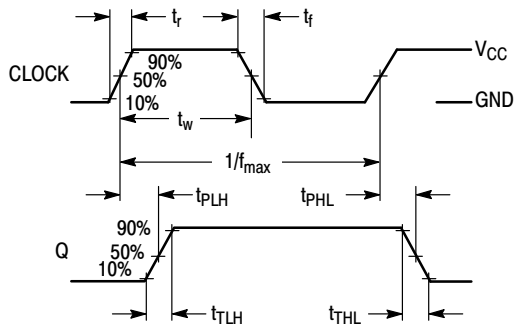


**Figure 1.**
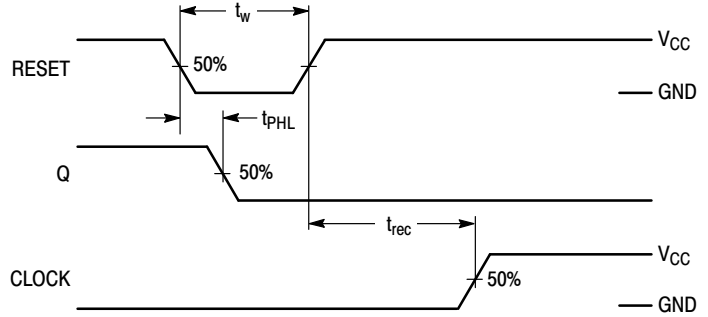


**Figure 2.**
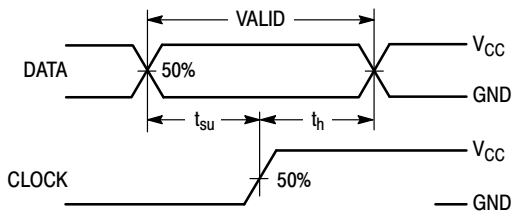


**Figure 3.**
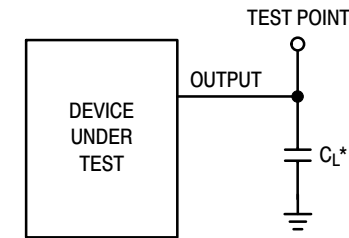


*Includes all probe and jig capacitance

**Figure 4. Test Circuit**
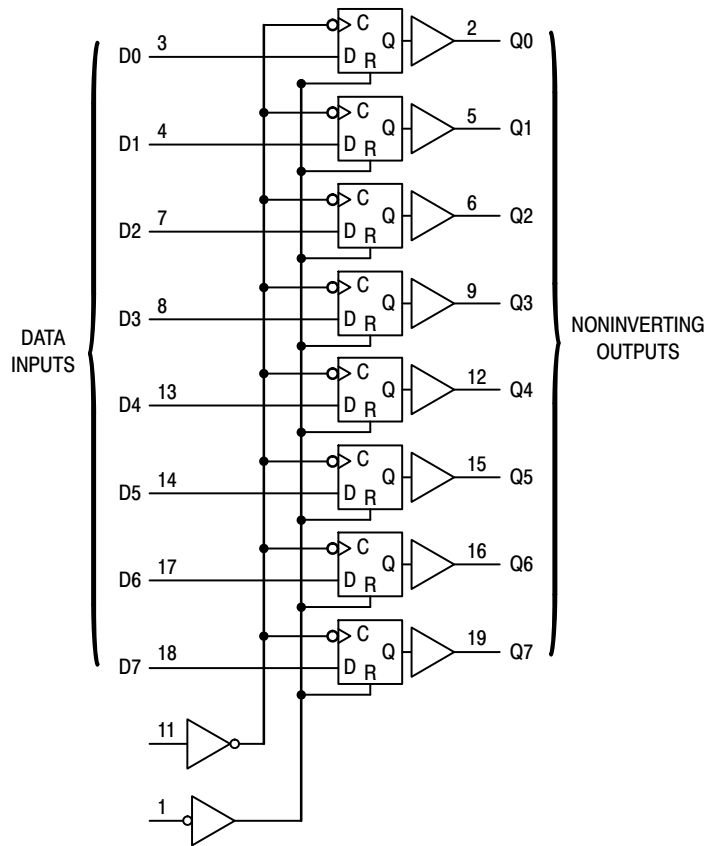


**Figure 5. Expanded Logic Diagram**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC74HC273ADWG | SOIC−20 WB (Pb−Free) | 38 Units / Rail |
| MC74HC273ADWR2G | SOIC−20 WB (Pb−Free) | 1000 / Tape & Reel |
| NLV74HC273ADWR2G* | SOIC−20 WB (Pb−Free) | 1000 / Tape & Reel |
| MC74HC273ADTG | TSSOP−20 (Pb−Free) | 75 Units / Rail |
| MC74HC273ADTR2G | TSSOP−20 (Pb−Free) | 2500 / Tape & Reel |
| NLV74HC273ADTR2G* | TSSOP−20 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

# MC74HC273A

## PACKAGE DIMENSIONS

**TSSOP−20**
**DT SUFFIX**
CASE 948E−02
ISSUE C
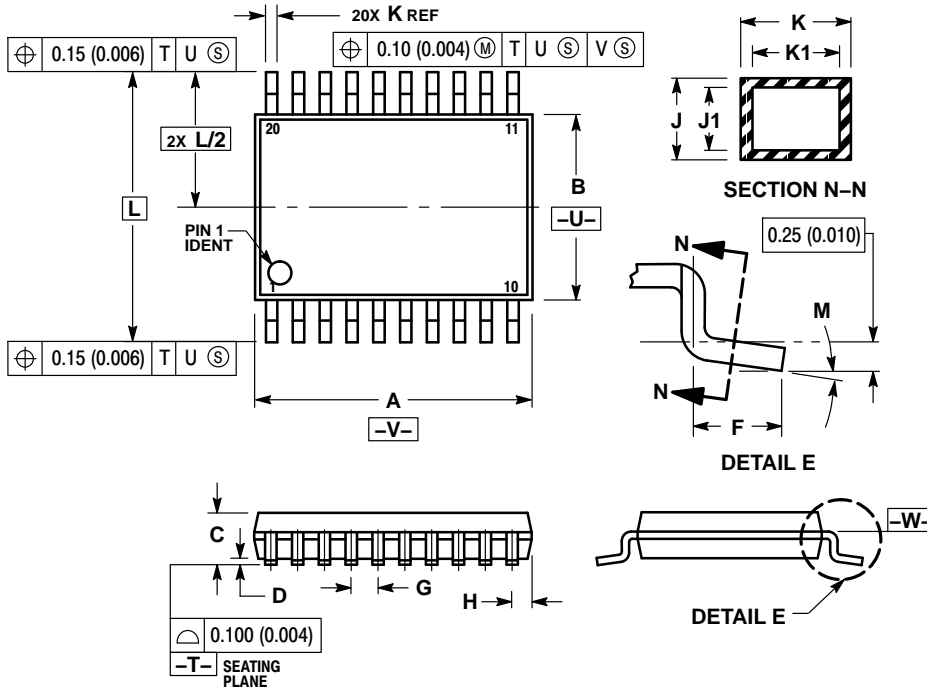
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
|-----|------|------|------|------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

**SECTION N−N**

**DETAIL E**

**SOLDERING FOOTPRINT\***

7.06

0.65 PITCH

16X 0.36

16X 1.26

DIMENSIONS: MILLIMETERS
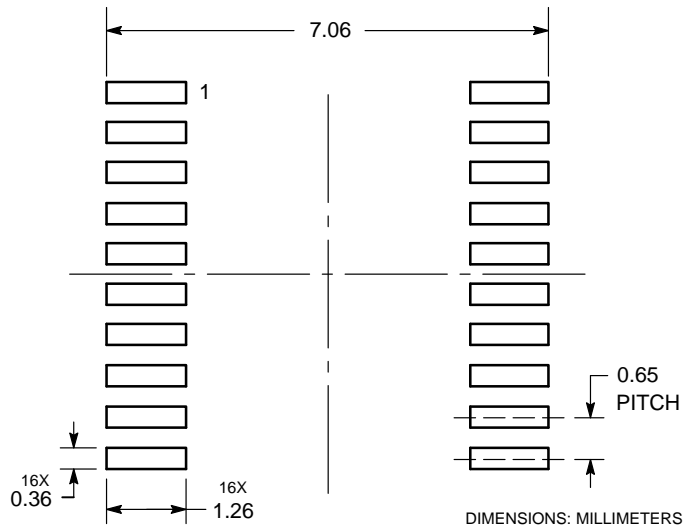
\*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74HC273A

## PACKAGE DIMENSIONS

**SOIC−20**
**DW SUFFIX**
CASE 751D−05
ISSUE G
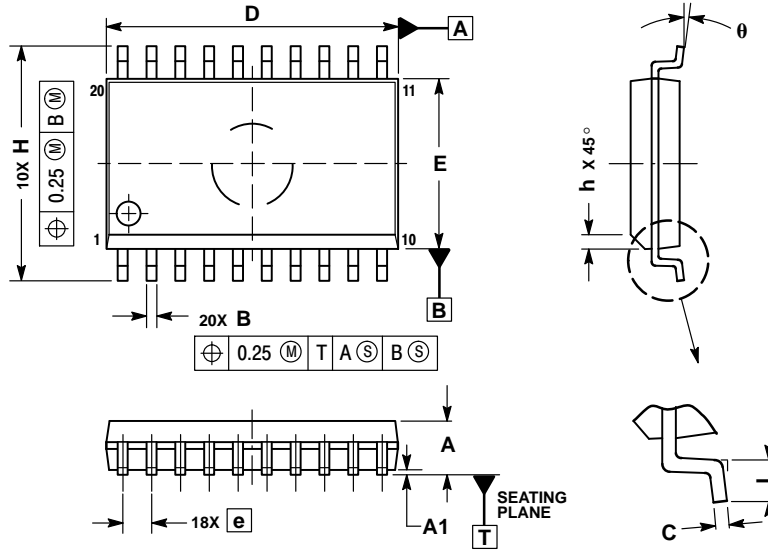
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS MIN | MILLIMETERS MAX |
|-----|-----|-----|
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0 ° | 7 ° |

**MC74HC273A/D**