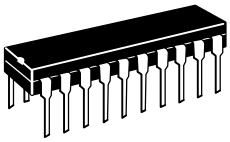
MC74AC323
MC74ACT323

8-INPUT UNIVERSAL SHIFT/ STORAGE REGISTER WITH SYNCHRONOUS RESET AND COMMON I/O PINS

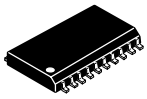
8-Input Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

The MC74AC323/74ACT323 is an 8-bit universal shift/storage register with3-state outputs. Its function is similar to the MC74AC299/74ACT299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

- Common Parallel I/O for Reduced Pin Count
- Additional Serial Inputs and Outputs for Expansion
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- ′ACT323 Has TTL Compatible Inputs



N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-04
PLASTIC

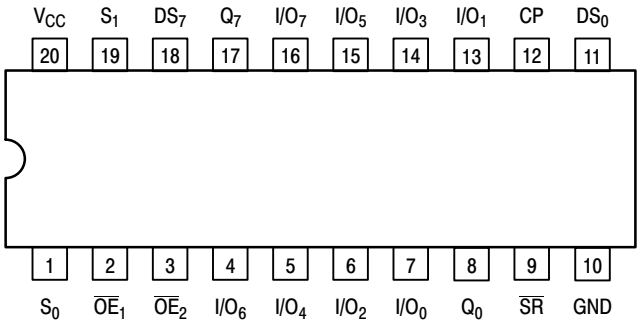


Figure 1. Pinout: 20–Lead Packages Conductors
(Top View)

PIN NAMES

CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{SR}$	Synchronous Master Reset
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs
I/O_0–I/O_7	Multipled Parallel Data Inputs or 3-State Parallel Data Outputs
Q_0, Q_7	Serial Outputs

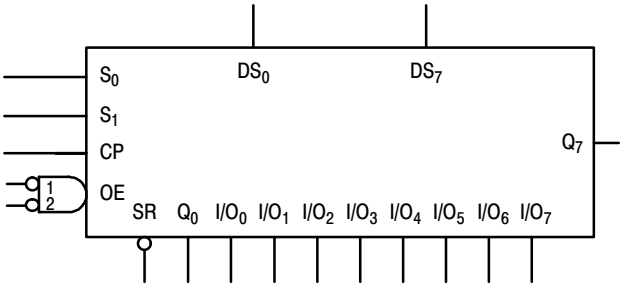
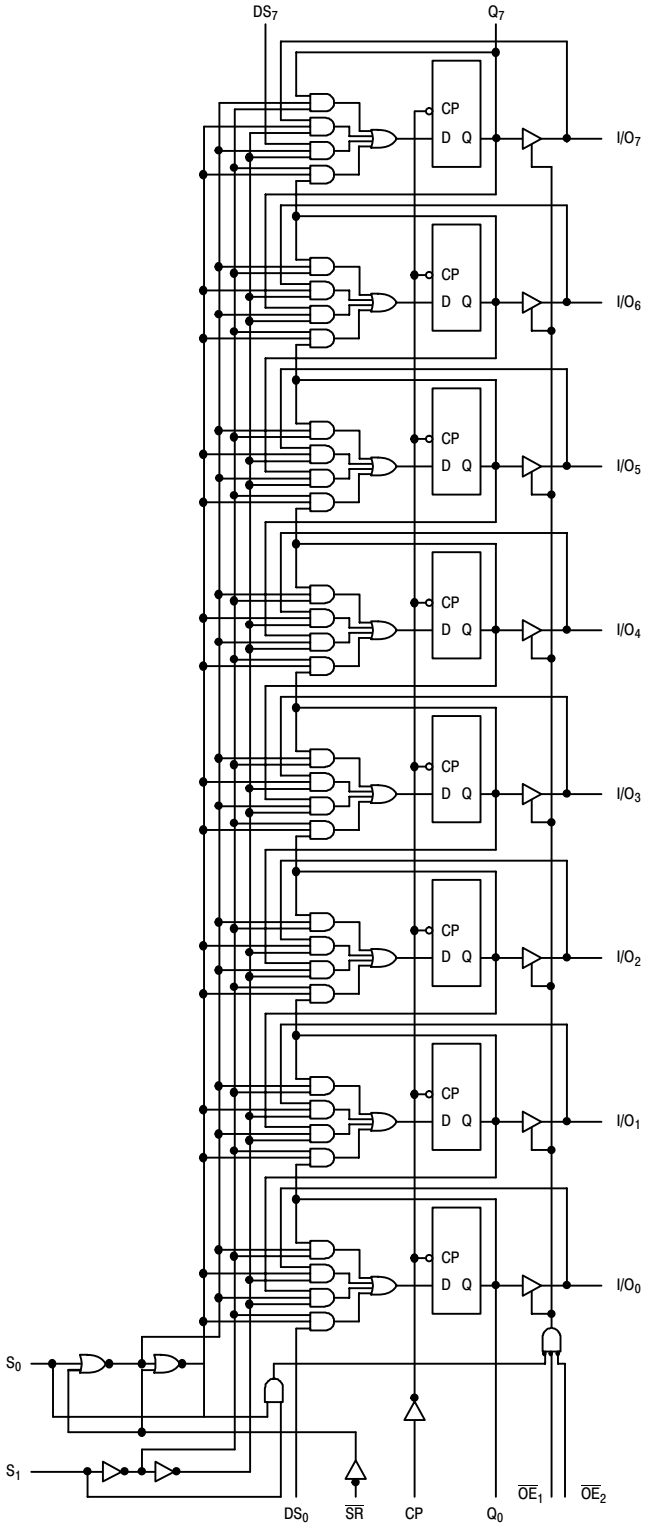


Figure 2. LOGIC SYMBOL



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. LOGIC DIAGRAM

FUNCTIONAL DESCRIPTION

The MC74AC323/74ACT323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3 state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

TRUTH TABLE

Inputs				Response
$\overline{SR}$	S_1	S_0	CP	
L	X	X	⎍	Synchronous Reset; $Q_0 – Q_7$ = LOW
H	H	H	⎍	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⎍	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⎍	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level ⎍ = LOW-to-HIGH Clock Transition

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V		150		ns/V
		V_{CC} @ 4.5 V		40		
		V_{CC} @ 5.5 V		25		
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V		10		ns/V
		V_{CC} @ 5.5 V		8.0		
T_J	Junction Temperature (PDIP)				140	°C
T_A	Operating Ambient Temperature Range		–40	25	85	°C
I_{OH}	Output Current — High				–24	mA
I_{OL}	Output Current — Low				24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC T_A = –40°C to +85°C		Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I_{OUT} = –50 μA
		3.0 4.5 5.5		2.56 3.86 4.86	2.46 3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} –12 mA I_{OH} –24 mA –24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I_{OUT} = 50 μA
		3.0 4.5 5.5		0.36 0.36 0.36	0.44 0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OZT}	Maximum 3-State Current	5.5		±0.6	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5			–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V_{IN} = V_{CC} or GND

* All outputs loaded; thresholds on input associated with output under test.
† Maximum test duration 2.0 ms, one output loaded at a time.
Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF		74AC T_A = –40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	3.3 5.0					MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	3.3 5.0					ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	3.3 5.0					ns	3-6
t_{PLH}	Propagation Delay CP to I/O_n	3.3 5.0					ns	3-6
t_{PHL}	Propagation Delay CP to I/O_n	3.3 5.0					ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0					ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0					ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0					ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0					ns	3-8

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF		74AC T_A = –40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0				ns	3-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0				ns	3-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	3.3 5.0				ns	3-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	3.3 5.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0				ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0				ns	3-6

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT		74ACT	Unit	Conditions
			T_A = +25°C		T_A = –40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = –50 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} –24 mA –24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OZT}	Maximum 3-State Current	5.5		±0.6	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} – 2.1 V
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5			–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V_{IN} = V_{CC} or GND

* All outputs loaded; thresholds on input associated with output under test.
† Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = –40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Input Frequency	5.0	120	125		110		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	5.0	5.0	9.0	12.5	4.0	14	ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	5.0	5.0	9.0	13.5	4.5	15	ns	3-6
t_{PLH}	Propagation Delay CP to I/O_n	5.0	5.0	8.5	12.5	4.5	14.5	ns	3-6
t_{PHL}	Propagation Delay CP to I/O_n	5.0	6.0	10	14.5	5.0	16	ns	3-6
t_{PZH}	Output Enable Time	5.0	3.5	7.5	11	3.0	12.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	3.5	7.5	11.5	3.0	13	ns	3-8
t_{PHZ}	Output Disable Time	5.0	4.0	8.5	12.5	3.0	13.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	3.0	8.0	11.5	2.5	12.5	ns	3-8

* Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF		74ACT T_A = –40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	2.0	5.0	5.0	ns	3-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	0	1.5	1.5	ns	3-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	1.0	4.0	4.5	ns	3-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	0	1.0	1.0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	1.0	2.5	2.5	ns	3-9
t_h	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	0	1.0	1.0	ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns	3-6

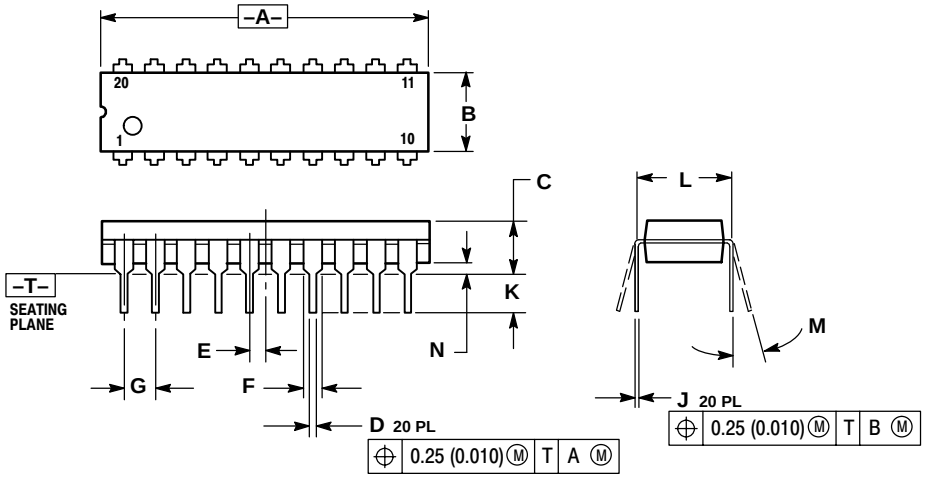
* Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	170	pF	V_{CC} = 5.0 V

OUTLINE DIMENSIONS

N SUFFIX
PLASTIC DIP PACKAGE
CASE 738–03
ISSUE E

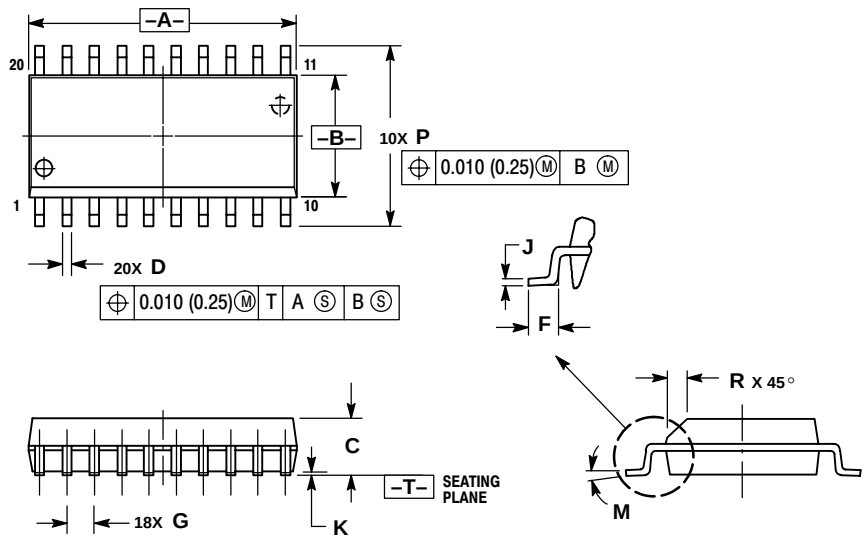


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Notes

Notes

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