

8-Bit Serial or Parallel-Input/ Serial-Output Shift Register with Input Latch

High-Performance Silicon-Gate CMOS

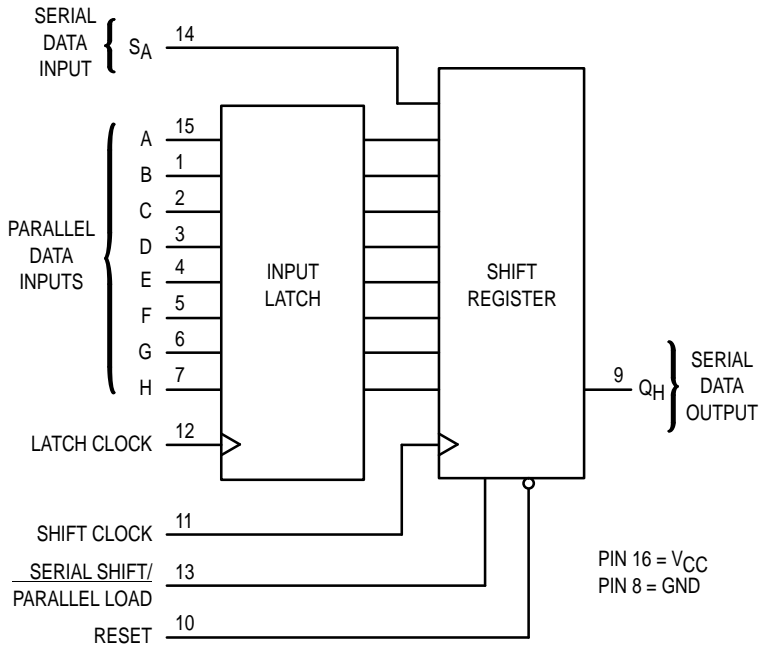
The MC54/74HC597 is identical in pinout to the LS597. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of an 8-bit input latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table).

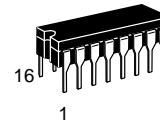
The HC597 is similar in function to the HC589, which is a 3-state device.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 516 FETs or 129 Equivalent Gates

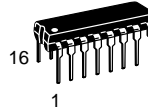
LOGIC DIAGRAM



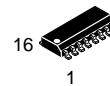
MC54/74HC597



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-08



D SUFFIX
SOIC PACKAGE
CASE 751B-05

ORDERING INFORMATION

MC54HCXXXJ	Ceramic
MC74HCXXXN	Plastic
MC74HCXXXD	SOIC

PIN ASSIGNMENT

B	1	16	V _{CC}
C	2	15	A
D	3	14	S _A
E	4	13	SERIAL SHIFT/ PARALLEL LOAD
F	5	12	LATCH CLOCK
G	6	11	SHIFT CLOCK
H	7	10	RESET
GND	8	9	Q _H



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	- 1.5 to $V_{CC} + 1.5$	V
V_{out}	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
T_{stg}	Storage Temperature	- 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C
Ceramic DIP: - 10 mW/°C from 100° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V	
T_A	Operating Temperature, All Package Types	- 55	+ 125	°C	
t_r, t_f	Input Rise and Fall Time (Figure 1)	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				- 55 to 25°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
V_{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
			$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	3.98	3.84	
V_{OL}	Maximum Low-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
			$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 4.0 \text{ mA}$ $ I_{out} \leq 5.2 \text{ mA}$	4.5	0.26	0.33	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC} \text{ or } GND$	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 8)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Latch Clock to Q _H (Figures 1 and 8)	2.0	210	265	315	ns
		4.5	42	53	63	
		6.0	36	45	54	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Shift Clock to Q _H (Figures 2 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PHL}	Maximum Propagation Delay, Reset to Q _H (Figures 3 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q _H (Figures 4 and 8)	2.0	175	220	265	ns
		4.5	35	44	53	
		6.0	30	37	45	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 8)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

- For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).
- Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance (Per Package)*	Typical @ 25°C, V _{CC} = 5.0 V		pF
		50		

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

PIN DESCRIPTIONS**DATA INPUTS****A, B, C, D, E, F, G, H (Pins 15, 1, 2, 3, 4, 5, 6, 7)**

Parallel data inputs. Data on these inputs is stored in the input latch on the rising edge of the Latch Clock input.

S_A (Pin 14)

Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/Parallel Load is high. Data on this input is ignored when Serial Shift/Parallel Load is low.

CONTROL INPUTS**Serial Shift/Parallel Load (Pin 13)**

Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the input latch, and serial shifting is inhibited.

Reset (Pin 10)

Asynchronous, Active-low shift register reset. A low level applied to this input resets the shift register to a low level, but does not change the data in the input latch.

Shift Clock (Pin 11)

Serial shift register clock. A low-to-high transition on this input shifts data on the Serial Data Input into the shift register and data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.

Latch Clock (Pin 12)

Latch clock. A low-to-high transition on this input loads the parallel data on inputs A–H into the input latch.

OUTPUT**Q_H (Pin 9)**

Serial data output. This pin is the output from the last stage of the shift register.

TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Parallel Data inputs A–H to Latch Clock (Figure 5)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Serial Data Input S_A to Shift Clock (Figure 6)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_{su}	Minimum Setup Time, Serial Shift/Parallel Load to Shift Clock (Figure 7)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_h	Minimum Hold Time, Latch Clock to Parallel Data Inputs A–H (Figure 5)	2.0 4.5 6.0	25 5 5	30 6 6	40 8 7	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input S_A (Figure 6)	2.0 4.5 6.0	5 5 5	5 5 5	5 5 5	ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Shift Clock (Figure 3)	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t_w	Minimum Pulse Width, Latch Clock and Shift Clock (Figures 1 and 2)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Reset (Figure 3)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_w	Minimum Pulse Width, Serial Shift/Parallel Load (Figure 4)	2.0 4.5 6.0	80 16 14	100 20 17	120 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 1)	2.0 4.5 6.0	1000 500 400	1000 500 400	1000 500 400	ns

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Reset	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S_A	Parallel Inputs A–H	Latch Contents	Shift Register Contents	Output Q_H
Reset shift register	L	X	L, H, $\bar{\text{L}}$	X	X	X	U	L	L
Reset shift register; load parallel data into data latch	L	X	$\bar{\text{L}}$	X	X	a–h	a–h	L	L
Load parallel data into data latch	H	H	$\bar{\text{L}}$	L, H, $\bar{\text{L}}$	X	a–h	a–h	U	U
Transfer latch contents to shift register	H	L	L, H, $\bar{\text{L}}$	X	X	X	U	$LR_N \rightarrow SR_N$	LR_H
Contents of data latch and shift register are unchanged	H	H	L, H, $\bar{\text{L}}$	L, H, $\bar{\text{L}}$	X	X	U	U	U
Load parallel data into data latch and shift register	H	L	$\bar{\text{L}}$	X	X	a–h	a–h	a–h	h
Shift serial data into shift register	H	H	X	$\bar{\text{L}}$	D	X	*	$SR_A = D;$ $SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$
Load parallel data into data latch and shift serial data into shift register	H	H	$\bar{\text{L}}$	$\bar{\text{L}}$	D	a–h	a–h	$SR_A = D;$ $SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$

LR = latch register contents
 SR = shift register contents
 * = depends on latch clock input

a–h = data at parallel data inputs A–H
 D = data (L, H) at serial data input S_A

U = remains unchanged
 X = don't care

SWITCHING WAVEFORMS

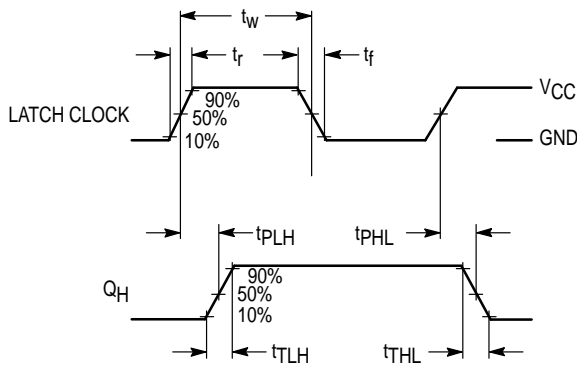


Figure 1. (Serial Shift/Parallel Load = L)

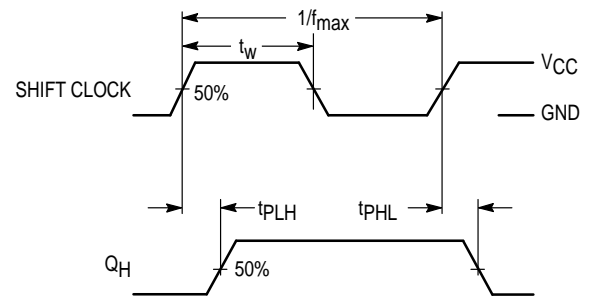


Figure 2. (Serial Shift/Parallel Load = H)

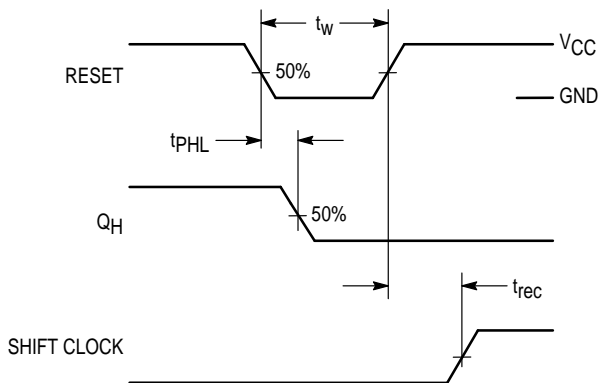


Figure 3.

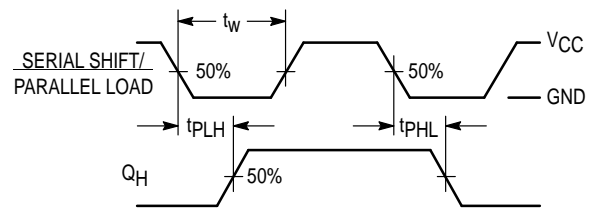


Figure 4.

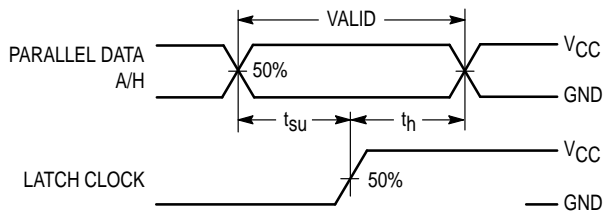


Figure 5.

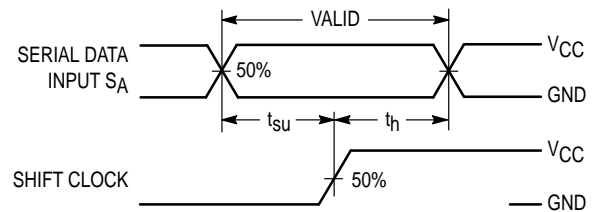


Figure 6.

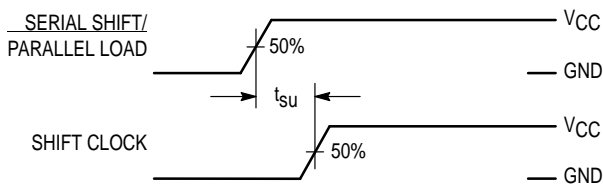
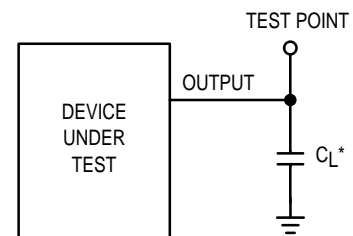


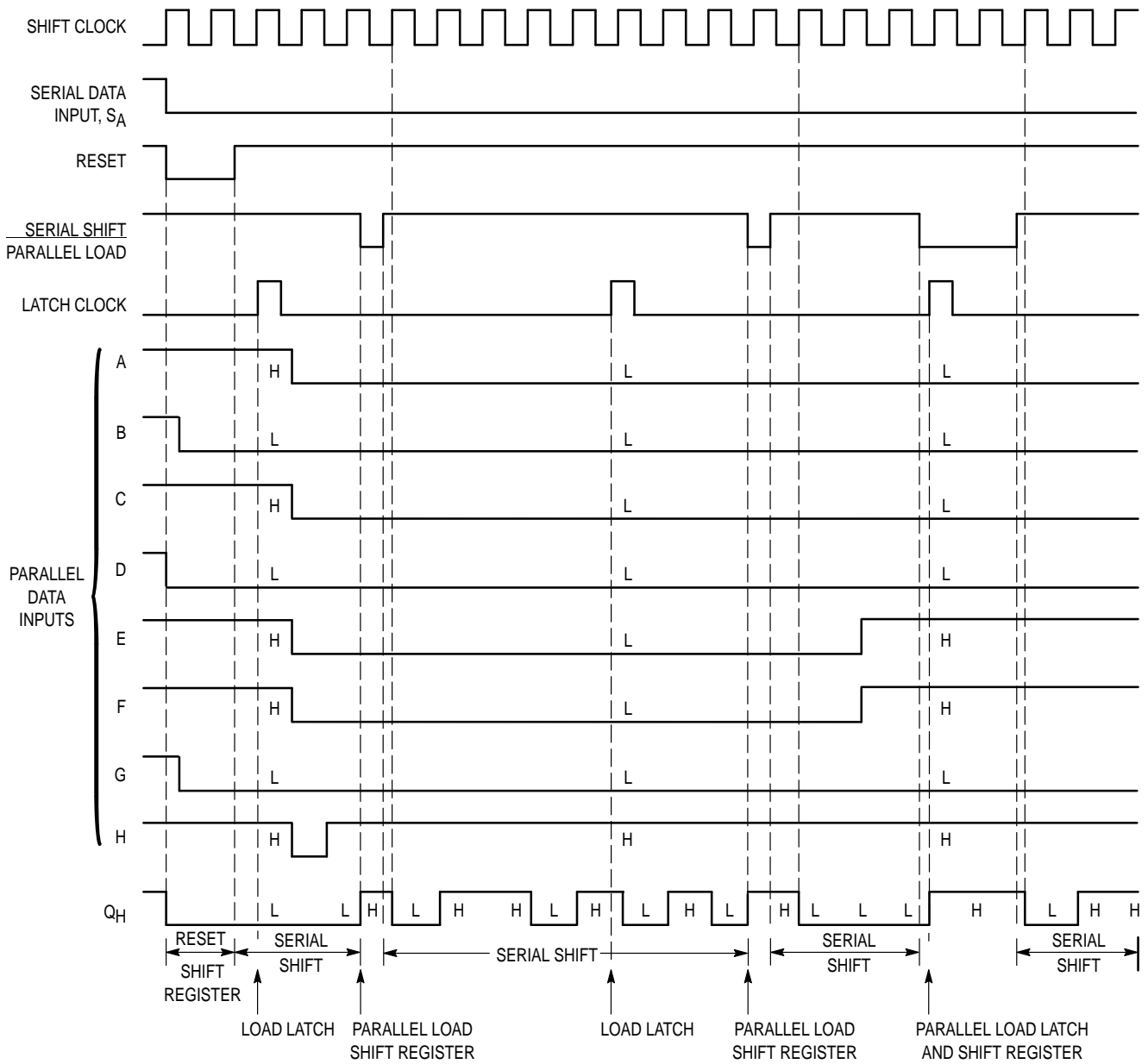
Figure 7.




* Includes all probe and jig capacitance

Figure 8. Test Circuit

TIMING DIAGRAM



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