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**Document:MC74F283 (5) VIEW**

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# 4-BIT BINARY FULL ADDER (With Fast Carry)

The MC54/74F283 high-speed 4-bit binary full adder with internal carry lookahead, accepts two 4-bit binary words ( $A_0-A_3$ ,  $B_0-B_3$ ) and a Carry input ( $C_0$ ). It generates the binary Sum outputs ( $S_0-S_3$ ) and the Carry output ( $C_4$ ) from the most significant bit. The F283 will operate with either active-HIGH or active-LOW operands (positive or negative logic).

### FUNCTIONAL DESCRIPTION

The F283 adds two 4-bit binary words ( $A$  plus  $B$ ) plus the incoming carry  $C_0$ . The binary sum appears on the Sum ( $S_0-S_3$ ) and outgoing carry ( $C_4$ ) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

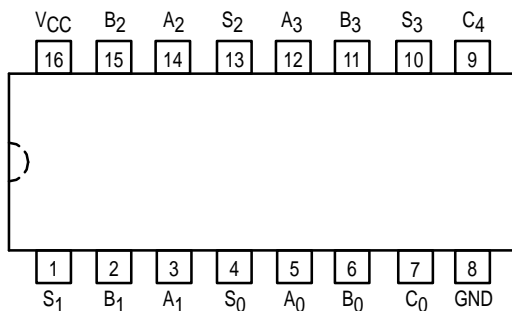
$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus  $C_0$ ,  $A_0$ ,  $B_0$  can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See Figure A. Note that if  $C_0$  is not used it must be tied LOW for active-HIGH logic or tied HIGH for active-LOW logic.

Due to pin limitations, the intermediate carries of the F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. Figure B shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder ( $A_3$ ,  $B_3$ ) LOW makes  $S_3$  dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, Figure C shows a way of dividing the F283 into a 2-bit and a 1-bit adder. The third stage adder ( $A_2$ ,  $B_2$ ,  $S_2$ ) is used merely as a means of getting a carry ( $C_{10}$ ) signal into the fourth stage (via  $A_2$  and  $B_2$ ) and bringing out the carry from the second stage on  $S_2$ . Note that as long as  $A_2$  and  $B_2$  are the same, whether HIGH or LOW, they do not influence  $S_2$ . Similarly, when  $A_2$  and  $B_2$  are the same the carry into the third stage does not influence the carry out of the third stage. Figure D shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs  $S_0$ ,  $S_1$  and  $S_2$  present a binary number equal to the number of inputs  $I_1-I_5$  that are true. Figure E shows one method of implementing a 5-input majority gate. When three or more of the inputs  $I_1-I_5$  are true, the output  $M_5$  is true.

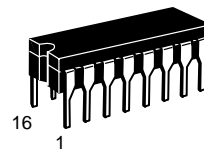
### CONNECTION DIAGRAM



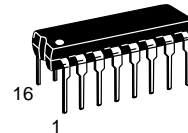
## MC54/74F283

### 4-BIT BINARY FULL ADDER (With Fast Carry)

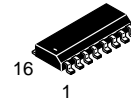
FAST™ SCHOTTKY TTL



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08

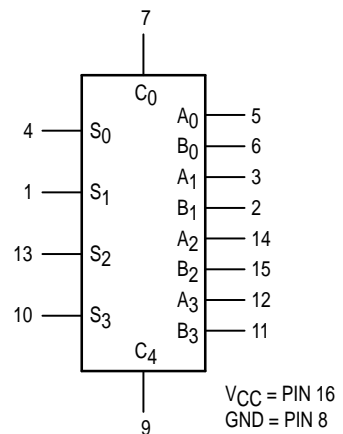


**D SUFFIX**  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

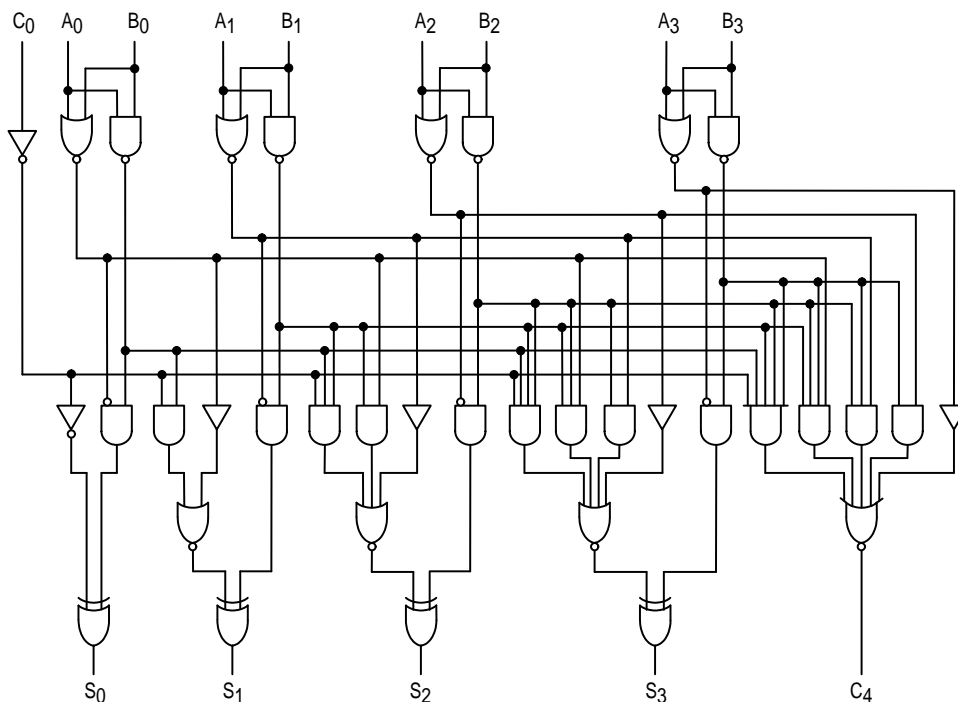
MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

### LOGIC SYMBOL



# MC54/74F283

## LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54, 74	4.5	5.0	5.5	V
T <sub>A</sub>	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I <sub>OH</sub>	Output Current — High	54, 74	—	—	-1.0	mA
I <sub>OL</sub>	Output Current — Low	54, 74	—	—	20	mA

Figure A. Active-HIGH versus Active-LOW Interpretation

	C <sub>0</sub>	A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	C <sub>4</sub>
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16      Active LOW: 1 + 5 + 6 = 12 + 0

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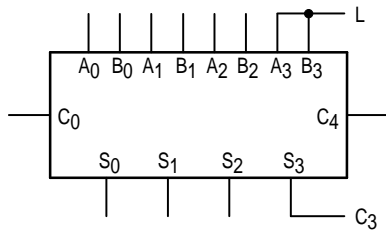


Figure B. 3-Bit Adder

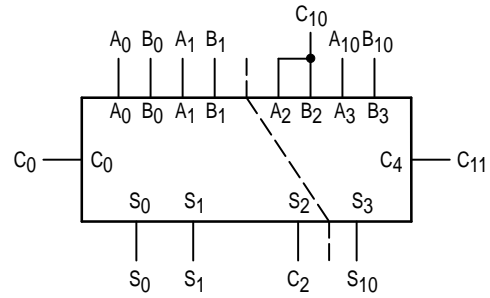


Figure C. 2-Bit and 1-Bit Adders

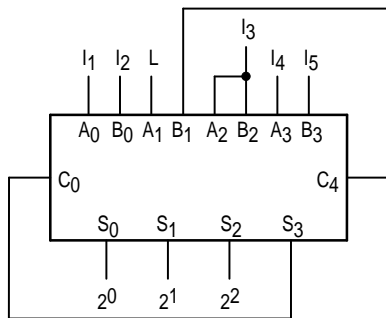


Figure D. 5-Input Encoder

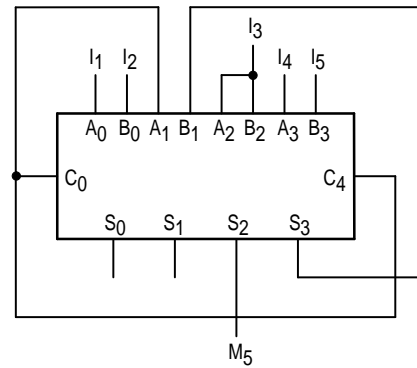


Figure E. 5-Input Majority Gate

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V <sub>IK</sub>	Input Clamp Diode Voltage			-1.2	V	I <sub>IN</sub> = -18 mA	V <sub>CC</sub> = MIN
V <sub>OH</sub>	Output HIGH Voltage	54, 74	2.5	3.4	V	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 4.5 V
		74	2.7	3.4	V	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 4.75 V
V <sub>OL</sub>	Output LOW Voltage		0.35	0.5	V	I <sub>OL</sub> = 20 mA	V <sub>CC</sub> = MIN
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>IN</sub> = 2.7 V	V <sub>CC</sub> = MAX
				100	μA	V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current C <sub>0</sub> Input			-0.6	mA	V <sub>IN</sub> = 0.5 V	V <sub>CC</sub> = MAX
	A and B Inputs			-1.2	mA		
I <sub>OS</sub>	Output Short Circuit Current (Note 2)	-60		-150	mA	V <sub>OUT</sub> = 0 V	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current		36	55	mA	Inputs = 4.5 V	V <sub>CC</sub> = MAX

NOTES:

- For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

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## AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0 V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55 to +125°C V <sub>CC</sub> = 5.0 V ±10% C <sub>L</sub> = 50 pF		T <sub>A</sub> = 0 to +70°C V <sub>CC</sub> = 5.0 V ±10% C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C <sub>0</sub> to S <sub>n</sub>	3.5 4.0	7.0 7.0	9.5 9.5	3.5 4.0	14 14	3.5 4.0	10.5 10.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A <sub>n</sub> or B <sub>n</sub> to S <sub>n</sub>	3.0 3.5	7.0 7.0	9.5 9.5	3.0 3.5	14 14	3.0 3.5	10.5 10.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C <sub>0</sub> to C <sub>4</sub>	3.5 3.0	5.7 5.4	7.5 7.0	3.5 3.0	10.5 10	3.5 3.0	8.5 8.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation A <sub>n</sub> or B <sub>n</sub> to C <sub>4</sub>	3.0 3.0	5.7 5.3	7.5 7.0	3.0 3.0	10.5 10	3.0 3.0	8.5 8.0	ns