

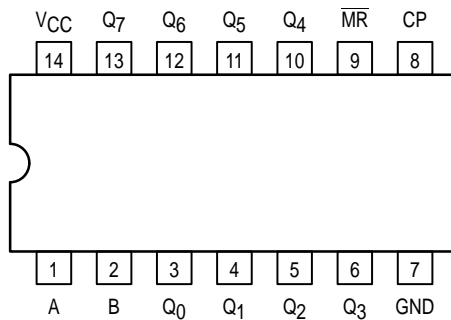


8-BIT SERIAL-IN, PARALLEL-OUT SHIFT REGISTER

The MC54/74F164 is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the LOW-to-HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock.

- Typical Shift Frequency of 90 MHz
- Asynchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers

CONNECTION DIAGRAM



MODE SELECT TABLE

Operating Mode	Inputs			Outputs	
	\overline{MR}	A	B	Q ₀	Q ₁ -Q ₇
Reset (Clear)	L	X	X	L	L-L
Shift	H	l	l	L	q ₀ -q ₆
	H	l	h	L	q ₀ -q ₆
	H	h	l	L	q ₀ -q ₆
	H	h	h	H	q ₀ -q ₆

H(h) = HIGH Voltage Levels

L(l) = LOW Voltage Levels

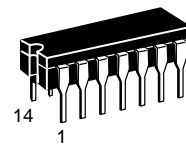
X = Don't Care

q_n = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

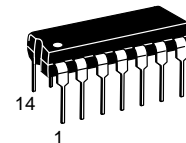
MC54/74F164

8-BIT SERIAL-IN, PARALLEL-OUT SHIFT REGISTER

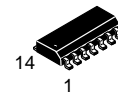
FAST™ SHOTTKY TTL



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

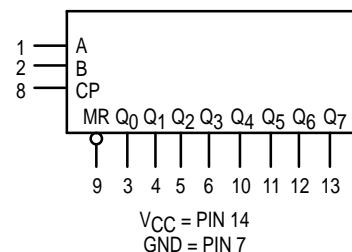


D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

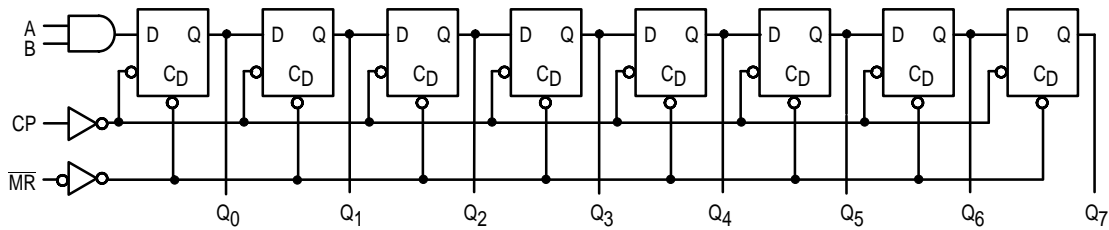
MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

LOGIC SYMBOL



MC54/74F164

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The F164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW-to-HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q₀ the logical AND of the two data inputs (A • B) that existed before the rising clock edge. A LOW level on the Master Reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			-1.2	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54, 74	2.5		V	I _{OH} = -1.0 mA, V _{CC} = MIN
		74	2.7		V	I _{OH} = -1.0 mA, V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.5	V	I _{OL} = 20 mA, V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current		35	55	mA	A, B = GND, V _{CC} = MAX CP = HIGH, MR = GND

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F164

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	80	90		70		80		MHz
t _{PLH}	Propagation Delay	3.0	6.0	8.0	3.0	11	3.0	9.0	ns
t _{PHL}	CP to Q _n	5.0	7.5	10	5.0	13	5.0	11	
t _{PHL}	Propagation Delay MR to Q _n	5.5	10.5	13	5.5	16	5.5	14	ns

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V			T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10%		T _A = 0°C to +70°C V _{CC} = +5.0 V ± 10%		
		Min	Typ	Max	Min	Max	Min	Max	
t _{S(H)}	Setup Time, HIGH or LOW	7.0			7.0		7.0		ns
t _{S(L)}	D _n to CP	7.0			7.0		7.0		
t _{H(H)}	Hold Time, HIGH or LOW	1.0			1.0		1.0		
t _{H(L)}	D _n to CP	1.0			1.0		1.0		ns
t _{W(H)}	CP Pulse Width, HIGH or LOW	4.0			4.0		4.0		
t _{W(L)}		7.0			7.0		7.0		
t _{W(L)}	MR Pulse Width, LOW	7.0			7.0		7.0		ns
t _{rec}	Recovery Time, MR to CP	7.0			7.0		7.0		ns