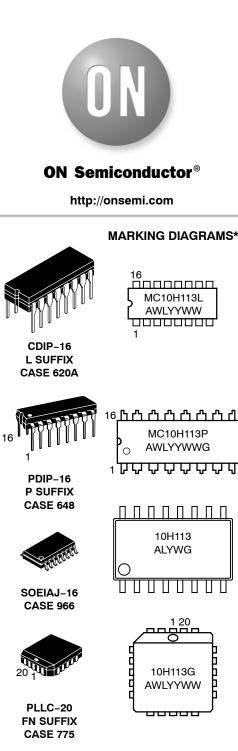
Quad Exclusive OR Gate

Description

The MC10H113 is a Quad Exclusive OR Gate with an enable common to all four gates. The outputs may be wire–ORed together to perform a 4–bit comparison function (A = B). The enable is active LOW.

Features

- Propagation Delay, 1.3 ns Typical
- Power Dissipation 175 mW Typ/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10KTM Compatible
- Pb-Free Packages are Available*



A = Assembly Location WL, L = Wafer Lot YY, Y = Year WW, W = Work Week G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

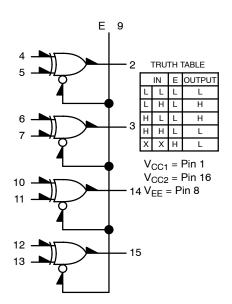
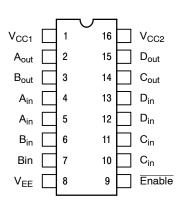


Figure 1. Logic Diagram



Pin assignment is for Dual-in-Line Package.

Figure 2. Pin Assignment

Table 1. MAXIMUM RATINGS

Symbol	Characteristic	Rating	Unit	
V_{EE}	Power Supply ($V_{CC} = 0$)		-8.0 to 0	Vdc
VI	Input Voltage (V _{CC} = 0)		0 to V _{EE}	Vdc
l _{out}	Output Current	Continuous Surge	50 100	mA
T _A	Operating Temperature Range		0 to +75	°C
T _{stg}	Storage Temperature Range	Plastic Ceramic	–55 to +150 −55 to +165	°C ℃

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

		0 °		25 °		75 °		
Symbol	Characteristic	Min	Max	Min	Max	Min	Max	Unit
Ι _Ε	Power Supply Current	-	46	-	42	-	46	mA
l _{inH}	Input Current High Pins 5, 7, 11, 13 Pins 4, 6, 10, 12 Pin 9	- - -	430 510 1100	- - -	270 320 740	- - -	270 320 740	μΑ
I _{inL}	Input Current Low	0.5	-	0.5	-	0.3	-	μΑ
V _{OH}	High Output Voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V _{OL}	Low Output Voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V _{IH}	High Input Voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V _{IL}	Low Input Voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Table 2. ELECTRICAL CHARACTERISTICS (V_{EE} = $-5.2 \text{ V} \pm 5\%$) (Note 1)

1. Each MECL 10H[™] series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to −2.0 V.

Table 3. AC CHARACTERISTICS

		0 °		25 °		75 °		
Symbol	Characteristic	Min	Мах	Min	Max	Min	Max	Unit
t _{pd}	Propagation Delay Data Enable	0.4 0.5	1.7 2.3	0.4 0.5	1.8 2.4	0.5 0.6	1.9 2.5	ns
t _r	Rise Time	0.5	1.8	0.6	1.9	0.6	2.0	ns
t _f	Fall Time	0.5	1.8	0.6	1.9	0.6	2.0	ns

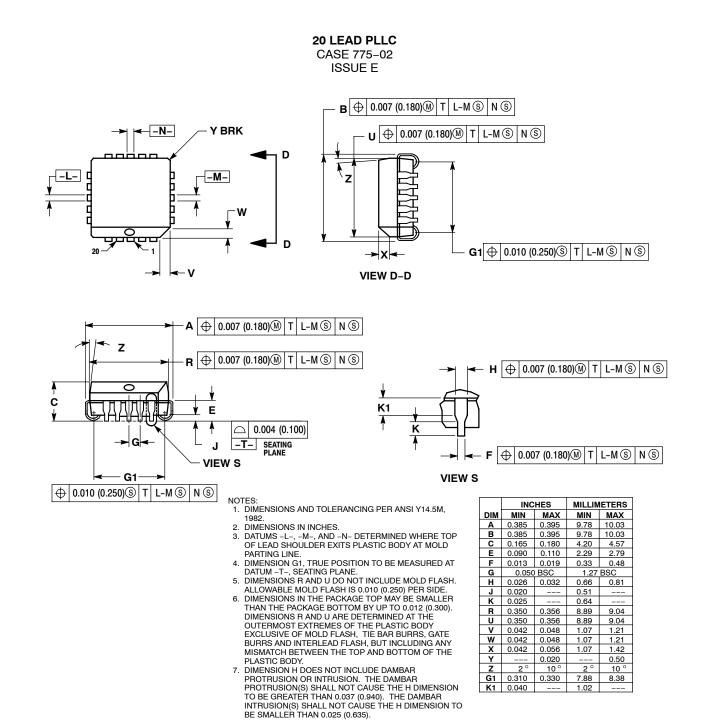
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

ORDERING INFORMATION

Device	Package	Shipping [†]
MC10H113FN	PLLC-20	46 Units / Rail
MC10H113FNG	PLLC-20 (Pb-Free)	46 Units / Rail
MC10H113FNR2	PLLC-20	500 / Tape & Reel
MC10H113FNR2G	PLLC-20 (Pb-Free)	500 / Tape & Reel
MC10H113L	CDIP-16	25 Unit / Rail
MC10H113M	SOEIAJ-16	50 Unit / Rail
MC10H113MG	SOEIAJ-16 (Pb-Free)	50 Unit / Rail
MC10H113MEL	SOEIAJ-16	2000 / Tape & Reel
MC10H113MELG SOEIAJ-16 (Pb-Free)		2000 / Tape & Reel
MC10H113P	PDIP-16	25 Unit / Rail
MC10H113PG	PDIP-16 (Pb-Free)	25 Unit / Rail

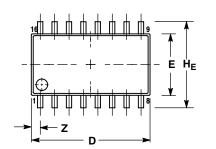
+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

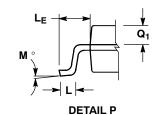
PACKAGE DIMENSIONS

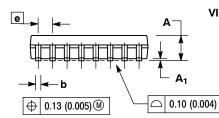


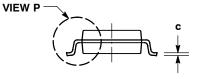
PACKAGE DIMENSIONS

SOEIAJ-16 CASE 966-01 **ISSUE A**







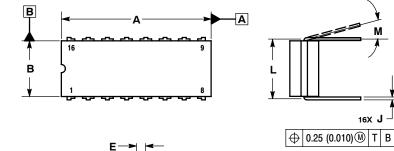


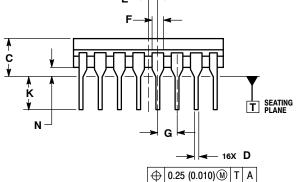
- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018). TO BE 0.46 (0.018).

	MILLIN	IETERS	INCHES				
DIM	MIN MAX		MIN	MAX			
Α		2.05		0.081			
A ₁	0.05	0.20	0.002	0.008			
p	0.35	0.50	0.014	0.020			
C	0.10	0.20	0.007	0.011			
D	9.90	10.50	0.390	0.413			
Е	5.10	5.45	0.201	0.215			
e	1.27	BSC	0.050 BSC				
HE	7.40	8.20	0.291	0.323			
L	0.50	0.85	0.020	0.033			
LΕ	1.10	1.50	0.043	0.059			
М	0 °	10 °	0 °	10 °			
Q1	0.70	0.90	0.028	0.035			
Ζ		0.78		0.031			

CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620A-01 **ISSUE O**





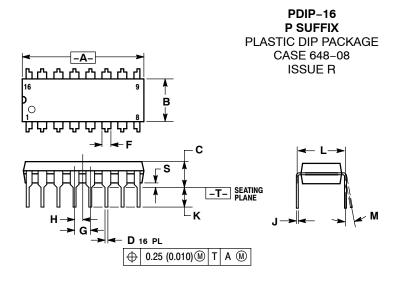
NOTES:

16X J

- 1. DIMENSIONING AND TOLERANCING PER
- 2. 3.
- DIMENSIONING AND TOLEHANCING PER ASME Y14.5M, 1994. CONTROLLING DIMENSION: INCH. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC 4.
- BODY. THIS DRAWING REPLACES OBSOLETE CASE OUTLINE 620-10. 5

	INCHES MILLIMETERS							
			MILLIMETERS MIN MAX					
DIM	MIN	MIN MAX		MAX				
Α	0.750	0.785	19.05	19.93				
В	0.240	0.295	6.10	7.49				
С		0.200		5.08				
D	0.015	0.015 0.020		0.50				
Е	0.050 BSC		1.27 BSC					
F	0.055	0.065	1.40	1.65				
G	0.100	BSC	2.54 BSC					
Н	0.008	0.015	0.21	0.38				
К	0.125	0.170	3.18	4.31				
L	0.300 BSC		7.62	BSC				
М	0 °	15 °	0 °	15°				
Ν	0.020	0.040	0.51	1.01				

PACKAGE DIMENSIONS



NOTES:

DIMENSIONING AND TOLERANCING PER ANSI Y14.5M. 1982.

CONTROLLING DIMENSION: INCH.

DIMENSION L TO CENTER OF LEADS WHEN 3

FORMED PARALLEL DIMENSION B DOES NOT INCLUDE MOLD FLASH. ROUNDED CORNERS OPTIONAL. 5.

	INC	HES	MILLIMETERS		
DIM	MIN MAX		MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.145 0.175		4.44	
D	0.015 0.021		0.39	0.53	
F	0.040 0.70		1.02	1.77	
G	0.100 BSC		2.54 BSC		
н	0.050	BSC	1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.295 0.305		7.74	
M	0°	10 °	0 °	10 °	
S	0.020	0.020 0.040		1.01	

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