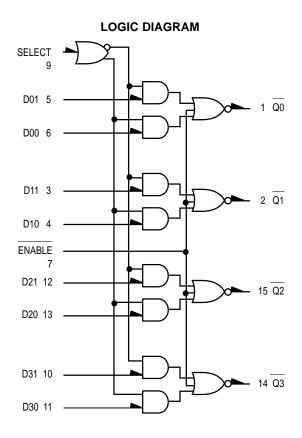
Quad 2-Input Multiplexer (Inverting)

The MC10159 is a quad two channel multiplexer with enable. It incorporates common enable and common data select inputs. The select input determines which data inputs are enabled. A high (H) level enables data inputs D00, D10, D20, and D30. A low (L) level enables data inputs D01, D11, D21, and D31. Any change on the data inputs will be reflected at the outputs while the enable is low. Input levels are inverted at the output.

 $\begin{array}{rll} P_D = & 218 \text{ mW typ/pkg (No Load)} \\ t_{pd} = & 2.5 \text{ ns typ (Data to Q)} \\ & 3.2 \text{ ns typ (Select to Q)} \\ t_r, t_f = & 2.5 \text{ ns typ (20\%-80\%)} \end{array}$



TRUTH TABLE

L

L

Н

Н

Х

D0 D1

Х

X H L

L

HXL

X X L

L

ХН

Q

Н

Enable

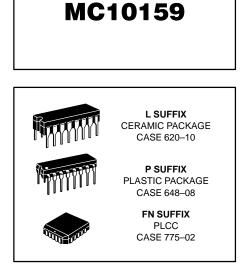
L

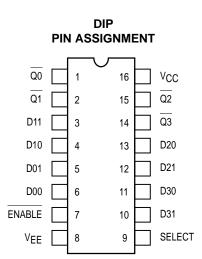
L

L

Н

VCC	=	PIN	16
VFF			





Pin assignment is for Dual–in–Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6–11 of the Motorola MECL Data Book (DL122/D).

ELECTRICAL CHARACTERISTICS

			Test Limits							
		Pin Under	–30°C		+25°C			+85°C		
Characteristic	Symbol	Test	Min	Max	Min	Тур	Max	Min	Max	Unit
Power Supply Drain Current	١E	8		58		42	53		58	mAdc
Input Current	l _{inH}	9 5		360 400			225 250		225 250	μAdc
	l _{inL}	5	0.5		0.5			0.3		μAdc
Output Voltage Logic 1	∨он	1	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
Output Voltage Logic 0	VOL	1	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
Threshold Voltage Logic 1	VOHA	1	-1.080		-0.980			-0.910		Vdc
Threshold Voltage Logic 0	VOLA	1		-1.655			-1.630		-1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Data Input Delay Select Input Enable Input	^t 5+1– ^t 9+1– ^t 7+1–	1 1 1	1.1 1.5 1.4	3.8 5.3 5.3	1.2 1.5 1.5	2.5 3.2 2.5	3.3 5.0 5.0	1.1 1.5 1.4	3.8 5.3 5.3	
Rise Time (20 to 80%) Fall Time (20 to 80%)	t ₁₊ t ₁₋	1 1	1.0 1.0	3.7 3.7	1.1 1.1	2.5 2.5	3.5 3.5	1.0 1.0	3.7 3.7	

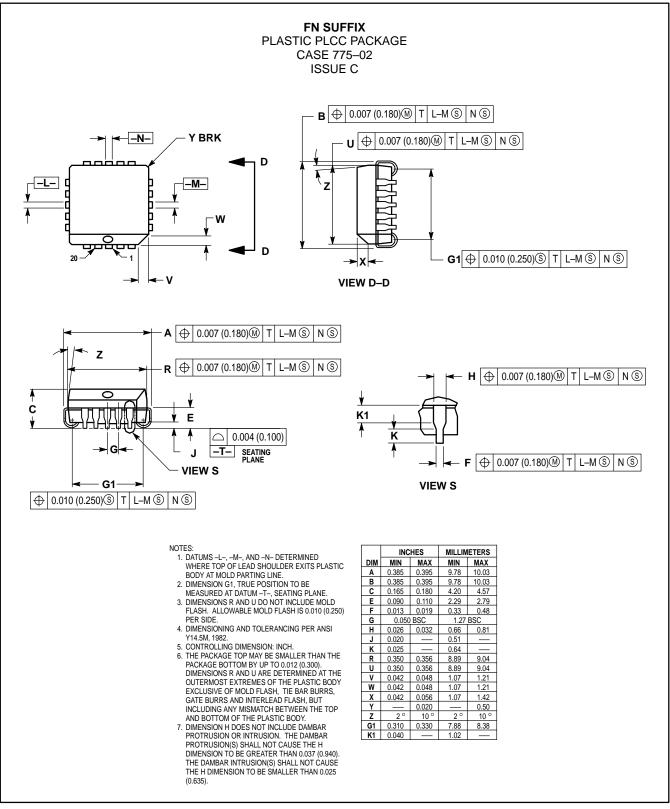
ELECTRICAL CHARACTERISTICS (continued)

				TEST VOLTAGE VALUES (Volts)						
		@ Test Te	mperature	V _{IHmax}	V _{ILmin}	V _{IHAmin}	VILAmax	VEE		
			–30°C	-0.890	-1.890	-1.205	-1.500	-5.2		
			+25°C	-0.810	-1.850	-1.105	-1.475	-5.2		
			+85°C	-0.700	-1.825	-1.035	-1.440	-5.2		
			Pin							
		Under Test	VIHmax	V _{ILmin}	VIHAmin	VILAmax	VEE	(V _{CC}) Gnd		
Power Supply Drain Cu	urrent	١E	8					8	16	
Input Current		l _{inH}	9 5	9 5				8 8	16 16	
		l _{inL}	5		5			8	16	
Output Voltage	Logic 1	VOH	1					8	16	
Output Voltage	Logic 0	VOL	1	5				8	16	
Threshold Voltage	Logic 1	VOHA	1	9			6	8	16	
Threshold Voltage	Logic 0	VOLA	1	9		6		8	16	
Switching Times	(50 Ω Load)			+1.11V	+0.31V	Pulse In	Pulse Out	–3.2 V	+2.0 V	
Propagation Delay	Data Input Select Input Enable Input	^t 5+1– ^t 9+1– ^t 7+1–	1 1 1	6 3, 12		5 9 7	1 1 1	8 8	16 16	
Rise Time	(20 to 80%)	t ₁₊	1	9		5	1	8	16	
Fall Time	(20 to 80%)	t ₁₋	1	9		5	1	8	16	

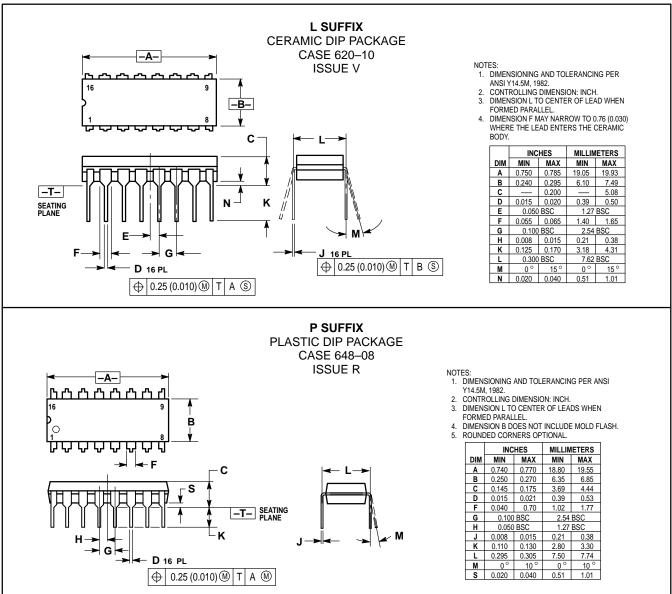
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

MC10159

OUTLINE DIMENSIONS



OUTLINE DIMENSIONS



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