

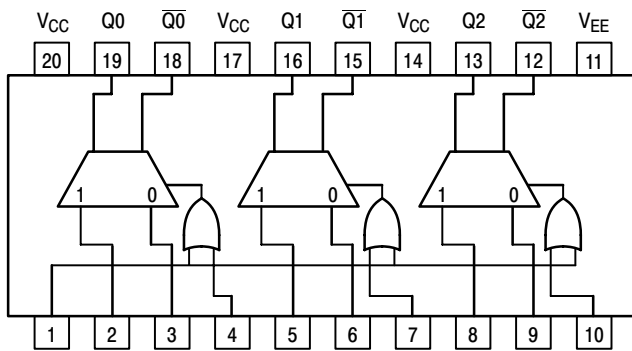
# MC100EL59

## 5V ECL Triple 2:1 Multiplexer

The MC100EL59 is a triple 2:1 multiplexer with differential outputs. The output data of the multiplexers can be controlled individually via the select inputs or as a group via the common select input. The flexible selection scheme makes the device useful for both data path and random logic applications.

- Individual or Common Select Controls
- 500 ps Typical Propagation Delays
- ESD Protection: >2 KV HBM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 4.2\text{ V to }5.7\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -4.2\text{ V to }-5.7\text{ V}$
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at  $V_{EE}$
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 182 devices

### Logic Diagram and Pinout: 20-Lead SOIC (Top View)



COM\_SEL D0a D0b SEL0 D1a D1b SEL1 D2a D2b SEL2

Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

### PIN DESCRIPTION

Pins	Function
D0a–D2a	ECL Input Data a*
D0b–D2b	ECL Input Data b*
SEL0–SEL2	ECL Individual Select Input*
COM_SEL	ECL Common Select Input*
Q0–Q2; $\overline{Q0}$ – $\overline{Q2}$	ECL Differential Outputs
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply

### TRUTH TABLE

SEL*	Data
H	a
L	b

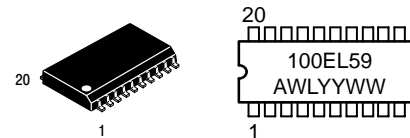
\* Pins will default low when left open.



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### MARKING DIAGRAM\*



SO-20  
DW SUFFIX  
CASE 751D

A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

\*For additional information, see Application Note AND8002/D

### ORDERING INFORMATION

Device	Package	Shipping
MC100EL59DW	SO-20	38 Units/Rail
MC100EL59DWR2	SO-20	1000 Units/Reel

# MC100EL59

## MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		8 to 0	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-8 to 0	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub> V <sub>I</sub> ≥ V <sub>EE</sub>	6 to 0 -6 to 0	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	90 60	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)	std bd	20 SOIC	30 to 35	°C/W
T <sub>sol</sub>	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

## PECL DC CHARACTERISTICS V<sub>CC</sub>= 5.0 V; V<sub>EE</sub>= 0.0 V (Note 1)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		27	32		27	32		27	32	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
V <sub>IH</sub>	Input HIGH Voltage	3835		4120	3835		4120	3835		4120	mV
V <sub>IL</sub>	Input LOW Voltage	3190		3525	3190		3525	3190		3525	mV
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

- Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.8 V / -0.5 V.
- Outputs are terminated through a 50 ohm resistor to V<sub>CC</sub>-2 volts.

## NECL DC CHARACTERISTICS V<sub>CC</sub>= 0.0 V; V<sub>EE</sub>= -5.0 V (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I <sub>EE</sub>	Power Supply Current		27	32		27	32		27	32	mA
V <sub>OH</sub>	Output HIGH Voltage (Note 2.)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
V <sub>OL</sub>	Output LOW Voltage (Note 2.)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
V <sub>IH</sub>	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	mV
V <sub>IL</sub>	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	mV
I <sub>IH</sub>	Input HIGH Current			150			150			150	μA
I <sub>IL</sub>	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

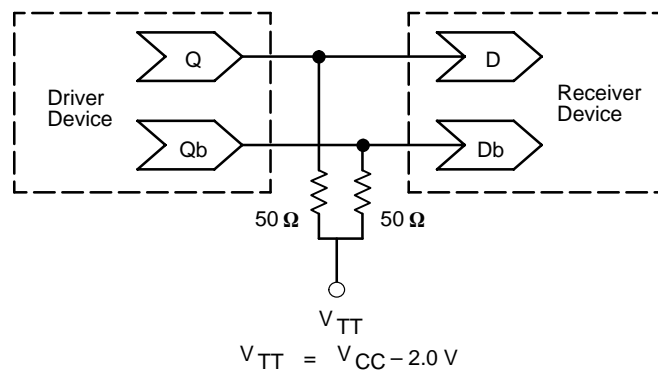
- Input and output parameters vary 1:1 with V<sub>CC</sub>. V<sub>EE</sub> can vary +0.8 V / -0.5 V.
- Outputs are terminated through a 50 ohm resistor to V<sub>CC</sub>-2 volts.

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**AC CHARACTERISTICS**  $V_{CC}= 5.0\text{ V}$ ;  $V_{EE}= 0.0\text{ V}$  or  $V_{CC}= 0.0\text{ V}$ ;  $V_{EE}= -5.0\text{ V}$  (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay DATA to Q/ $\bar{Q}$ SEL to Q/ $\bar{Q}$ COM_SEL to Q/ $\bar{Q}$	340 340 340		690 690 690	340 340 340		690 690 690	340 340 340		690 690 690	ps
$t_{skew}$	Output-Output Skew Any $D_n$ , $D_m$ to Q			100			100			100	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$t_r$ $t_f$	Output Rise/Fall Times Q (20% - 80%)	200		540	200		540	200		540	ps

1.  $V_{EE}$  can vary +0.8 V / -0.5 V.



**Figure 1. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

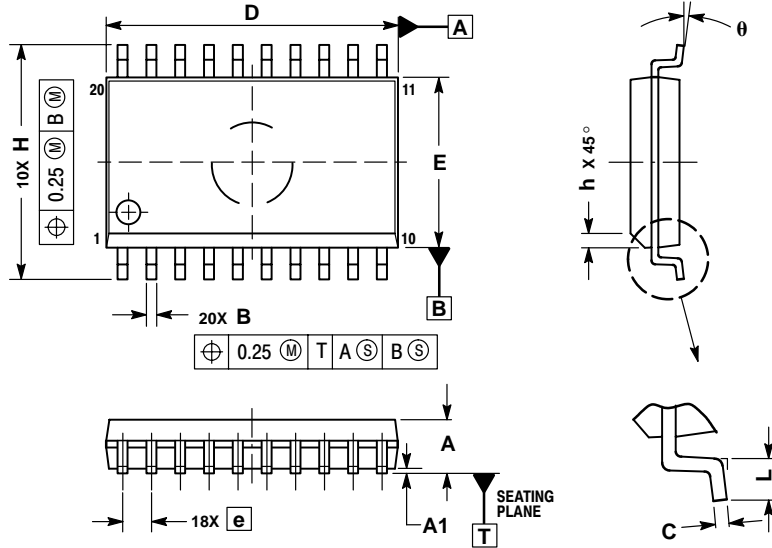
## Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

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## PACKAGE DIMENSIONS


SO-20  
DW SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751D-05  
ISSUE F



### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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