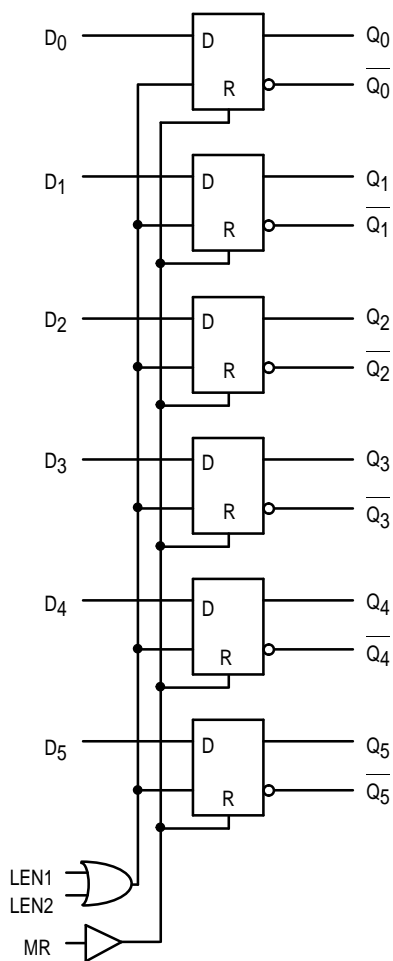


## 6-Bit D Latch

The MC10E100E150 contains six D-type latches with differential outputs. When both Latch Enables (LEN1, LEN2) are LOW, the latch is transparent and input data transitions propagate through to the output. A logic HIGH on either LEN1 or LEN2 (or both) latches the data. The Master Reset (MR) overrides all other controls to set the Q outputs low.

- 800ps Max. Propagation Delay
- Extended 100E V<sub>EE</sub> Range of - 4.2V to - 5.46V
- 75kΩ Input Pulldown Resistors

### LOGIC DIAGRAM

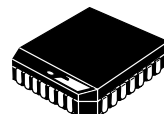


### PIN NAMES

Pin	Function
D <sub>0</sub> – D <sub>5</sub>	Data Inputs
LEN1, LEN2	Latch Enables
MR	Master Reset
$\overline{Q_0} - \overline{Q_5}$	True Outputs
Q <sub>0</sub> – Q <sub>5</sub>	Inverting Outputs

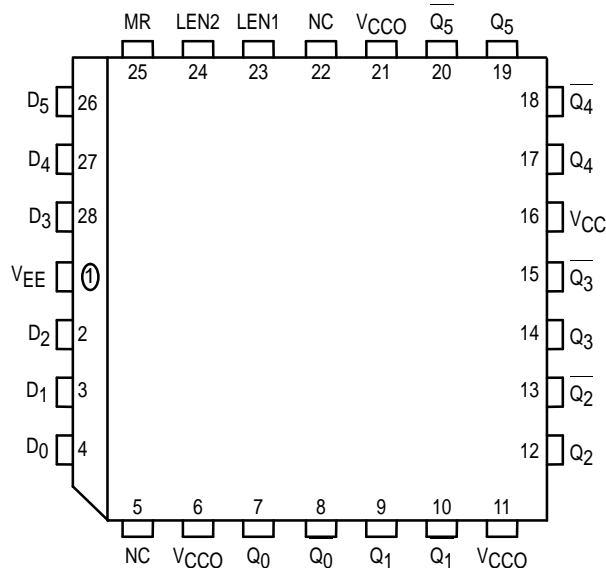
**MC10E150**  
**MC100E150**

**6-BIT D LATCH**



**FN SUFFIX**  
PLASTIC PACKAGE  
CASE 776-02

### Pinout: 28-Lead PLCC (Top View)



\* All V<sub>CC</sub> and V<sub>CCO</sub> pins are tied together on the die.



MC10E150 MC100E150

**DC CHARACTERISTICS** ( $V_{EE} = V_{EE}(\text{min})$  to  $V_{EE}(\text{max})$ ;  $V_{CC} = V_{CCO} = \text{GND}$ )

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
$I_{IH}$	Input HIGH Current										$\mu\text{A}$	
	D			200			200			200		
	LEN, MR			150			150			150		
$I_{EE}$	Power Supply Current										mA	
	10E		52	62		52	62		52	62		
	100E		52	62		52	62		60	72		

**AC CHARACTERISTICS** ( $V_{EE} = V_{EE}(\text{min})$  to  $V_{EE}(\text{max})$ ;  $V_{CC} = V_{CCO} = \text{GND}$ )

Symbol	Characteristic	0°C			25°C			85°C			Unit	Condition
		min	typ	max	min	typ	max	min	typ	max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output										ps	
	D	250	375	550	250	375	550	250	375	550		
	LEN	375	500	700	375	500	700	375	500	700		
	MR	450	625	750	450	625	750	450	625	750		
$t_s$	Setup Time										ps	
	D	200	50		200	50		200	50			
$t_h$	Hold Time										ps	
	D	200	- 50		200	- 50		200	- 50			
$t_{RR}$	Reset Recovery Time	750	650		750	650		750	650		ps	ps
$t_{PW}$	Minimum Pulse Width										ps	
	MR	400			400			400				
$t_{SKEW}$	Within-Device Skew		50			50			50		ps	1
$t_r$ $t_f$	Rise/Fall Times										ps	
	20 - 80%	300	450	650	300	450	650	300	450	650		

1. Within-device skew is defined as identical transitions on similar paths through a device.

OUTLINE DIMENSIONS


FN SUFFIX  
 PLASTIC PLCC PACKAGE  
 CASE 776-02  
 ISSUE D



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°		10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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