32-bit RISC Microcontroller

CMOS

FR30 MB91101 Series

MB91101/MB91101A

■ DESCRIPTION

The MB91101 and MB91101A are a standard single-chip microcontroller constructed around the 32-bit RISC CPU (FR* family) core with abundant I/O resources and bus control functions optimized for high-performance/ high-speed CPU processing for embedded controller applications. To support the vast memory space accessed by the 32-bit CPU, the MB91101 and MB91101A normally operate in the external bus access mode and executes instructions on the internal 1 Kbyte cache memory and 2 Kbytes RAM for enhanced performance.

The MB91101 and MB91101A are optimized for applications requiring high-performance CPU processing such as navigation systems, high-performance FAXs and printer controllers.

*: FR Family stands for FUJITSU RISC controller.

■ FEATURES

FR CPU
• 32-bit RISC, load/store architecture, 5-stage pipeline
• Operating clock frequency: Internal 50 MHz/external 25 MHz (PLL used at source oscillation 12.5 MHz)
• General purpose registers: 32 bits × 16
• 16-bit fixed length instructions (basic instructions), 1 instruction/1 cycle
• Memory to memory transfer, bit processing, barrel shifter processing: Optimized for embedded applications
• Function entrance/exit instructions, multiple load/store instructions of register contents, instruction systems supporting high level languages
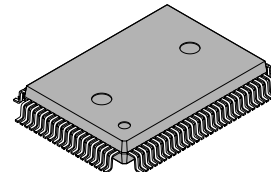
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■ PACKAGES

100-pin Plastic LQFP

100-pin Plastic QFP

(FPT-100P-M05)

(FPT-100P-M06)

FUJITSU
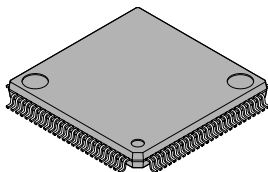
• Register interlock functions, efficient assembly language coding
• Branch instructions with delay slots: Reduced overhead time in branch executions
• Internal multiplier/supported at instruction level
  Signed 32-bit multiplication: 5 cycles
  Signed 16-bit multiplication: 3 cycles
• Interrupt (push PC and PS): 6 cycles, 16 priority levels

External bus interface
• Clock doubler: Internal 50 MHz, external bus 25 MHz operation
• 25-bit address bus (32 Mbytes memory space)
• 8/16-bit data bus
• Basic external bus cycle: 2 clock cycles
• Chip select outputs for setting down to a minimum memory block size of 64 Kbytes: 6
• Interface supported for various memory technologies
  DRAM interface (area 4 and 5)
• Automatic wait cycle insertion: Flexible setting, from 0 to 7 for each area
• Unused data/address pins can be configured as input/output ports.
• Little endian mode supported (Select 1 area from area 1 to 5)

DRAM interface
• 2 banks independent control (area 4 and 5)
• Normal mode (double CAS DRAM)/high-speed page mode (single CAS DRAM)/Hyper DRAM
• Basic bus cycle: Normally 5 cycles, 2-cycle access possible in high-speed page mode
• Programmable waveform: Automatic 1-cycle wait insertion to RAS and CAS cycles
• DRAM refresh
  CBR refresh (interval time configurable by 6-bit timer)
  Self-refresh mode
• Supports 8/9/10/12-bit column address width
• 2CAS/1WE, 2WE/1CAS selective

Cache memory
• 1-Kbyte instruction cache memory
• 32 block/way, 4 entry(4 word)/block
• 2 way set associative
• Lock function: For specific program code to be resident in cashe memory

DMA controller (DMAC)
• 8 channels
• Transfer incident/external pins/internal resource interrupt requests
• Transfer sequence: Step transfer/block transfer/burst transfer/continuous transfer
• Transfer data length: 8 bits/16 bits/32 bits selective
• NMI/interrupt request enables temporary stop operation.

UART
• 3 independent channels
• Full-duplex double buffer
• Data length: 7 bits to 9 bits (non-parity), 6 bits to 8 bits (parity)
• Asynchronous (start-stop system), CLK-synchronized communication selective
• Multi-processor mode
• Internal 16-bit timer (U-TIMER) operating as a proprietary baud rate generator: Generates any given baud rate
• External clock can be used as a transfer clock.
• Error detection: Parity, frame, overrun

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10-bit A/D converter (successive approximation conversion type)
- 10-bit resolution, 4 channels
- Successive approximation type: Conversion time of 5.6 μs at 25 MHz
- Internal sample and hold circuit
- Conversion mode: Single conversion/scanning conversion/repeated conversion/stop conversion selective
- Start: Software/external trigger/internal timer selective

16-bit reload timer
- 3 channels
- Internal clock: 2 clock cycle resolution, divide by 2/8/32 selective

Other interval timers
- 16-bit timer: 3 channels (U-TIMER)
- PWM timer: 4 channels
- Watchdog timer: 1 channel

Bit search module

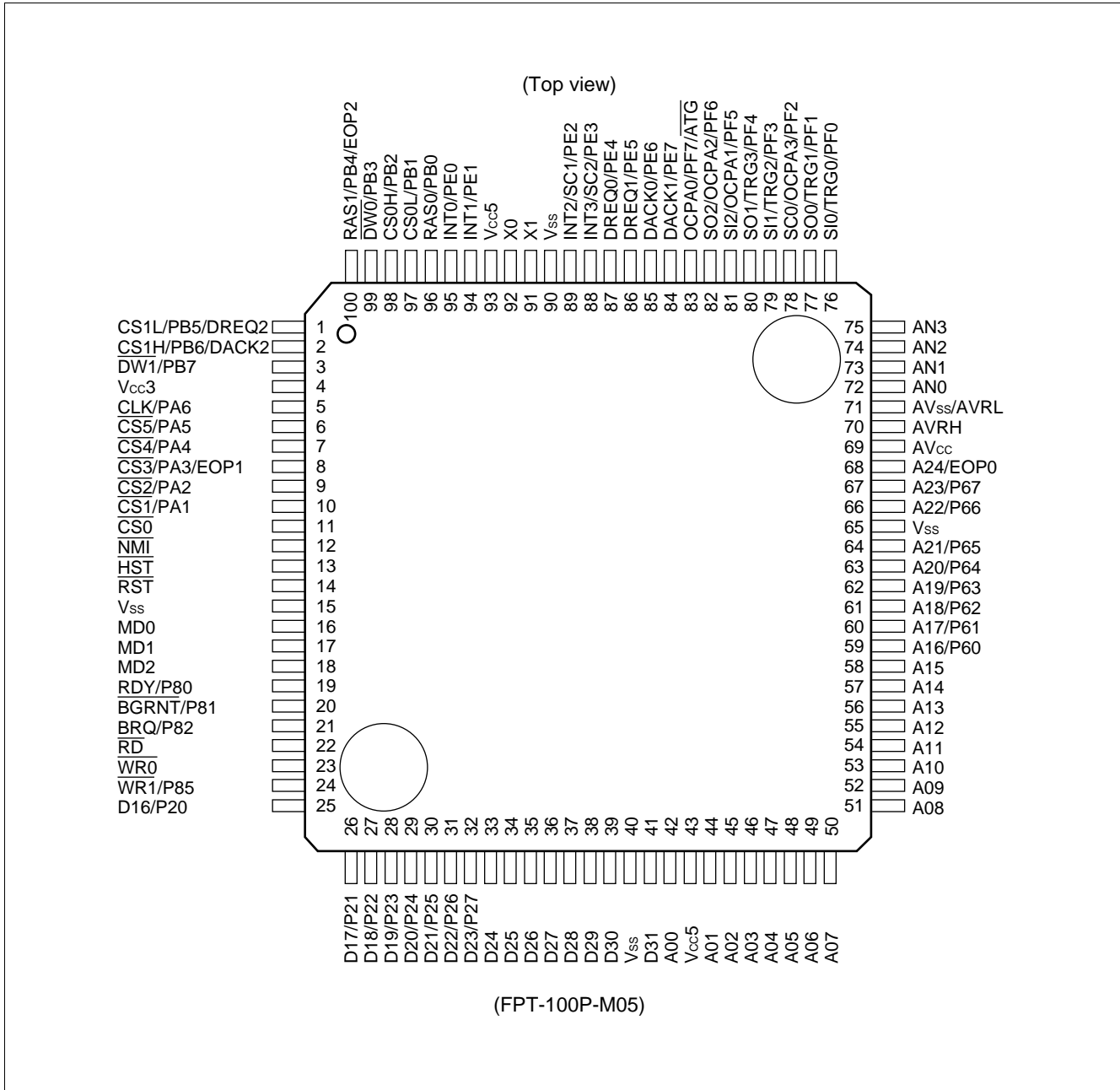First bit transition "1" or "0" from MSB can be detected in 1 cycle.

Interrupt controller
- External interrupt input: Non-maskable interrupt ($\overline{\text{NMI}}$), normal interrupt $\times$ 4 (INT0 to INT3)
- Internal interrupt incident:UART, DMA controller (DMAC), A/D converter, U-TIMER and delayed interrupt module
- Priority levels of interrupts are programmable except for non-maskable interrupt (in 16 steps).

Others
- Reset cause: Power-on reset/hardware standby/watchdog timer/software reset/external reset
- Low-power consumption mode: Sleep mode/stop mode
- Clock control
  Gear function: Operating clocks for CPU and peripherals are independently selective.
  Gear clock can be selected from 1/1, 1/2, 1/4 and 1/8 (or 1/2, 1/4, 1/8 and 1/16).
  However, operating frequency for peripherals is less than 25 MHz.
- Packages: LQFP-100 and QFP-100
- CMOS technology (0.35 μm)
- Power supply voltage
  5 V: CPU power supply 5.0 V $\pm$10% (internal regulator)
       A/D power supply   2.7 V to 3.6 V
  3 V: CPU power supply 2.7 V to 3.6 V (without internal regulator)
       A/D power supply   2.7 V to 3.6 V
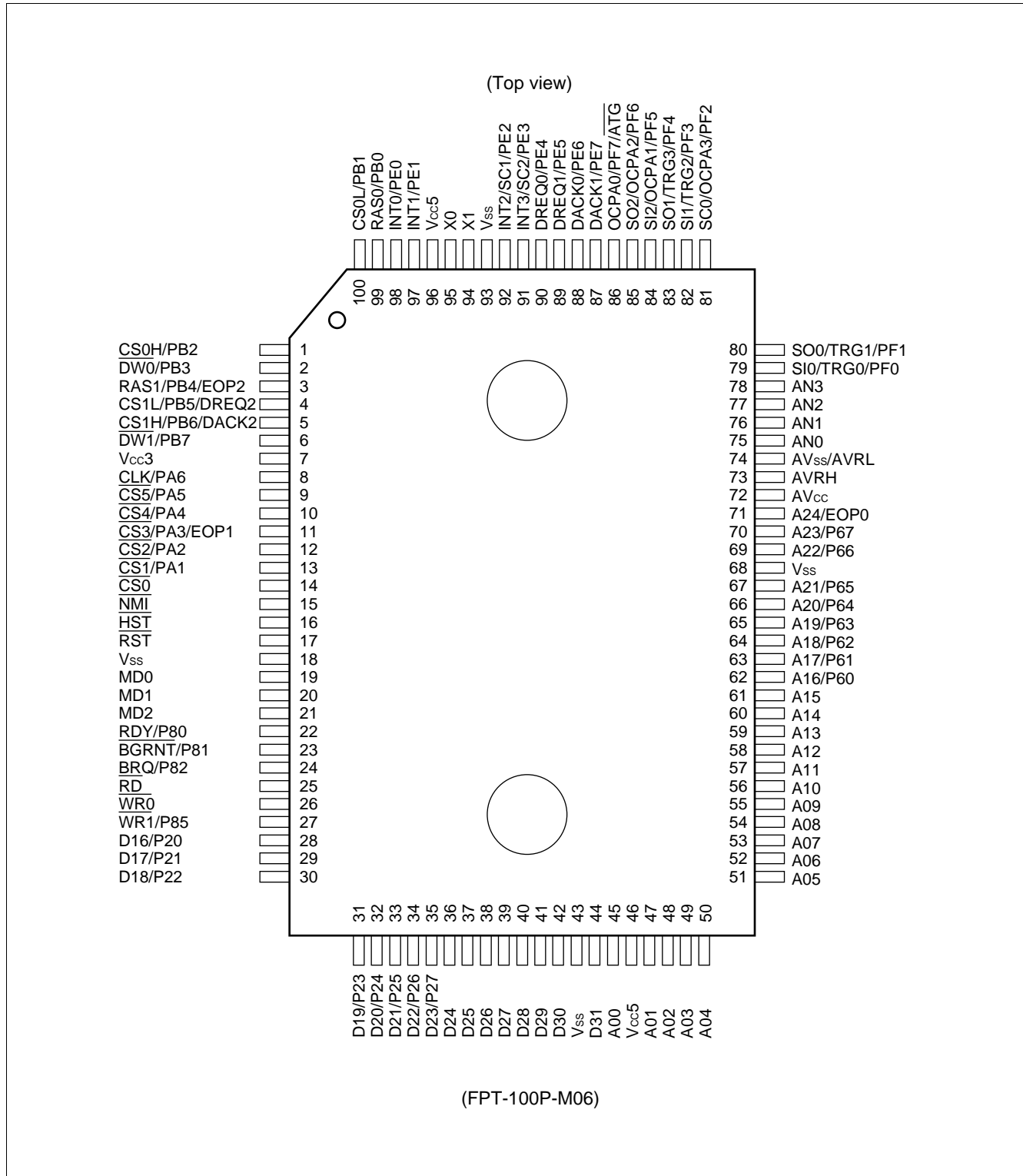
■ PIN ASSIGNMENT

(Top view)

```
                    R D C C R I I V X X V I I D D D D O S S S S S S S S
                    A W S S A N N c 0 1 s N N R R A A C C I I O O C O I
                    S 0 0 0 S T T c   s T T E E C C P P 2 1 1 I 0 0 0
                    1 / H L 0 0 1 5   2 3 Q Q K K A A / / / / / / / /
                    / P / / / / /   / / 0 1 0 1 0 0 O T T P T P T
                    P B P P P E E   S S / / / / / / C R R F R R
                    B 3 B B B 0 1   C C P P P P P P P G G 3 G 2 G
                    4 / 2 1 0       1 2 E E E E E E A 3 2 / 1 / 0
                    / E             / / 4 5 6 7 / A / / P / P /
                    E O             P P       P 1 P P F P F P
                    O P             E E       F / F F 4 F 1 F
                    P 2             2 3       7 P F 5   3   0
                    2               / / A T G 6 5
```

CS1L/PB5/DREQ2   1   ○ 100   75   AN3
CS1H/PB6/DACK2   2   74   AN2
DW1/PB7   3   73   AN1
Vcc3   4   72   AN0
CLK/PA6   5   71   AVss/AVRL
CS5/PA5   6   70   AVRH
CS4/PA4   7   69   AVcc
CS3/PA3/EOP1   8   68   A24/EOP0
CS2/PA2   9   67   A23/P67
CS1/PA1   10   66   A22/P66
CS0   11   65   Vss
NMI   12   64   A21/P65
HST   13   63   A20/P64
RST   14   62   A19/P63
Vss   15   61   A18/P62
MD0   16   60   A17/P61
MD1   17   59   A16/P60
MD2   18   58   A15
RDY/P80   19   57   A14
BGRNT/P81   20   56   A13
BRQ/P82   21   55   A12
RD   22   54   A11
WR0   23   53   A10
WR1/P85   24   52   A09
D16/P20   25   51   A08

```
  D D D D D D D D D D D D D V D A V A A A A A A A
  1 1 1 2 2 2 2 2 2 2 2 3 3 s 3 0 c 0 0 0 0 0 0 0
  7 8 9 0 1 2 3 4 5 6 7 8 9 s 1 0 c 1 2 3 4 5 6 7
  / / / / / /                  5
  P P P P P P
  2 2 2 2 2 2
  1 2 3 4 5 6
                26-50
```

(FPT-100P-M05)

(Continued)

(Top view)

Left side pins:
Pin	Signal
1	CS0H/PB2
2	DW0/PB3
3	RAS1/PB4/EOP2
4	CS1L/PB5/DREQ2
5	CS1H/PB6/DACK2
6	DW1/PB7
7	Vcc3
8	CLK/PA6
9	CS5/PA5
10	CS4/PA4
11	CS3/PA3/EOP1
12	CS2/PA2
13	CS1/PA1
14	CS0
15	NMI
16	HST
17	RST
18	Vss
19	MD0
20	MD1
21	MD2
22	RDY/P80
23	BGRNT/P81
24	BRQ/P82
25	RD
26	WR0
27	WR1/P85
28	D16/P20
29	D17/P21
30	D18/P22

Top side pins:
Pin	Signal
100	CS0L/PB1
99	RAS0/PB0
98	INT0/PE0
97	INT1/PE1
96	Vcc5
95	X0
94	X1
93	Vss
92	INT2/SC1/PE2
91	INT3/SC2/PE3
90	DREQ0/PE4
89	DREQ1/PE5
88	DACK0/PE6
87	DACK1/PE7
86	OCPA0/PF7/ATG
85	SO2/OCPA2/PF6
84	SI2/OCPA1/PF5
83	SO1/TRG3/PF4
82	SI1/TRG2/PF3
81	SC0/OCPA3/PF2

Right side pins:
Pin	Signal
80	SO0/TRG1/PF1
79	SI0/TRG0/PF0
78	AN3
77	AN2
76	AN1
75	AN0
74	AVss/AVRL
73	AVRH
72	AVcc
71	A24/EOP0
70	A23/P67
69	A22/P66
68	Vss
67	A21/P65
66	A20/P64
65	A19/P63
64	A18/P62
63	A17/P61
62	A16/P60
61	A15
60	A14
59	A13
58	A12
57	A11
56	A10
55	A09
54	A08
53	A07
52	A06
51	A05

Bottom side pins:
Pin	Signal
31	D19/P23
32	D20/P24
33	D21/P25
34	D22/P26
35	D23/P27
36	D24
37	D25
38	D26
39	D27
40	D28
41	D29
42	D30
43	Vss
44	D31
45	A00
46	Vcc5
47	A01
48	A02
49	A03
50	A04

(FPT-100P-M06)

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Description
LQFP*1	QFP*2			
25 to 32	28 to 35	D16 to D23	C	Bit 16 to bit 23 of external data bus
		P20 to P27		Can be configured as I/O ports when external data bus width is set to 8-bit.
33 to 39, 41	36 to 42, 44	D24 to D30, D31	C	Bit 24 to bit 31 of external data bus
42, 44 to 58	45, 47 to 61	A00, A01 to A15	F	Bit 00 to bit 15 of external address bus
59 to 64, 66, 67	62 to 67, 69, 70	A16 to A21, A22, A23	F	Bit 16 to bit 23 of external address bus
		P60 to P65, P66, P67		Can be configured as I/O ports when not used as address bus.
68	71	A24	L	Bit 24 of external address bus
		EOP0		Can be configured as DMAC EOP output (ch. 0) when DMAC EOP output is enabled.
19	22	RDY	C	External ready input Inputs "0" when bus cycle is being executed and not completed.
		P80		Can be configured as a port when RDY is not used.
20	23	$\overline{\text{BGRNT}}$	F	External bus release acknowledge output Outputs "L" level when external bus is released.
		P81		Can be configured as a port when $\overline{\text{BGRNT}}$ is not used.
21	24	BRQ	C	External bus release request input Inputs "1" when release of external bus is required.
		P82		Can be configured as a port when BRQ is not used.
22	25	$\overline{\text{RD}}$	L	Read strobe output pin for external bus
23	26	$\overline{\text{WR0}}$	L	Write strobe output pin for external bus Relation between control signals and effective byte locations is as follows:
24	27	$\overline{\text{WR1}}$	F	$\overline{\text{WR1}}$ is High-Z during resetting. Attach an external pull-up resister when using at 16-bit bus width.
		P85		Can be configured as a port when $\overline{\text{WR1}}$ is not used.

	16-bit bus width	8-bit bus width
D15 to D08	$\overline{\text{WR0}}$	$\overline{\text{WR0}}$
D07 to D00	$\overline{\text{WR1}}$	(I/O port enabled)

*1: FPT-100P-M05

*2: FPT-100P-M06

(Continued)

Pin no.		Pin name	Circuit type	Description
LQFP*1	QFP*2			
11	14	$\overline{CS0}$	L	Chip select 0 output ("L" active)
10	13	$\overline{CS1}$	F	Chip select 1 output ("L" active)
		PA1		Can be configured as a port when $\overline{CS1}$ is not used.
9	12	$\overline{CS2}$	F	Chip select 2 output ("L" active)
		PA2		Can be configured as a port when $\overline{CS2}$ is not used.
8	11	$\overline{CS3}$	F	Chip select 3 output ("L" active)
		PA3		Can be configured as a port when $\overline{CS3}$ and EOP1 are not used.
		EOP1		EOP output pin for DMAC (ch. 1) This function is available when EOP output for DMAC is enabled.
7	10	$\overline{CS4}$	F	Chip select 4 output ("L" active)
		PA4		Can be configured as a port when $\overline{CS4}$ is not used.
6	9	$\overline{CS5}$	F	Chip select 5 output ("L" active)
		PA5		Can be configured as a port when $\overline{CS5}$ is not used.
5	8	CLK	F	System clock output Outputs clock signal of external bus operating frequency.
		PA6		Can be configured as a port when CLK is not used.
96	99	RAS0	F	RAS output for DRAM bank 0 Refer to the DRAM interface for details.
		PB0		Can be configured as a port when RAS0 is not used.
97	100	CS0L	F	CASL output for DRAM bank 0 Refer to the DRAM interface for details.
		PB1		Can be configured as a port when CS0L is not used.
98	1	CS0H	F	CASH output for DRAM bank 0 Refer to the DRAM interface for details.
		PB2		Can be configured as a port when CS0H is not used.
99	2	$\overline{DW0}$	F	$\overline{WE}$ output for DRAM bank 0 ("L" active) Refer to the DRAM interface for details.
		PB3		Can be configured as a port when $\overline{DW0}$ is not used.
100	3	RAS1	F	RAS output for DRAM bank 1 Refer to the DRAM interface for details.
		PB4		Can be configured as a port when RAS1 and EOP2 are not used.
		EOP2		DMAC EOP output (ch. 2) This function is available when DMAC EOP output is enabled.

*1: FPT-100P-M05

*2: FPT-100P-M06

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Pin no.		Pin name	Circuit type	Description
LQFP*1	QFP*2			
1	4	CS1L	F	CASL output for DRAM bank 1 Refer to the DRAM interface for details.
		PB5		Can be configured as a port when CS1L and DREQ2 are not used.
		DREQ2		External transfer request input pin for DMA This pin is used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
2	5	CS1H	F	CASH output for DRAM bank 1 Refer to the DRAM interface for details.
		PB6		Can be configured as a port when CS1H and DACK2 are not used.
		DACK2		External transfer request acknowledge output pin for DMAC (ch. 2) This function is available when transfer request output for DMAC is enabled.
3	6	$\overline{DW1}$	F	$\overline{WE}$ output for DRAM bank 1 ("L" active) Refer to the DRAM interface for details.
		PB7		Can be configured as a port when $\overline{DW1}$ is not used.
16 to 18	19 to 21	MD0 to MD2	G	Mode pins 0 to 2 MCU basic operation mode is set by these pins. Directly connect these pins with V_{CC} or V_{SS} for use.
92	95	X0	A	Clock (oscillator) input
91	94	X1	A	Clock (oscillator) output
14	17	$\overline{RST}$	B	External reset input
13	16	$\overline{HST}$	H	Hardware standby input ("L" active)
12	15	$\overline{NMI}$	H	NMI (non-maskable interrupt pin) input ("L" active)
95, 94	98, 97	INT0, INT1	F	External interrupt request input pins These pins are used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from these pins unless such output is made intentionally.
		PE0, PE1		Can be configured as I/O ports when INT0, INT1 are not used.
89	92	INT2	F	External interrupt request input pin This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		SC1		Clock I/O pin for UART1 Clock output is available when clock output of UART1 is enabled.
		PE2		Can be configured as the I/O port when INT2 and SC1 are not used. This function is available when UART1 clock output is disabled.

*1: FPT-100P-M05

*2: FPT-100P-M06

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Pin no.		Pin name	Circuit type	Description
LQFP*1	QFP*2			
88	91	INT3	F	External interrupt request input pin This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		SC2		UART2 clock I/O pin Clock output is available when UART2 clock output is enabled.
		PE3		Can be configured as the I/O port when INT3 and SC2 are not used. This function is available when UART2 clock output is disabled.
87, 86	90, 89	DREQ0, DREQ1	F	External transfer request input pins for DMA These pins are used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from these pins unless such output is made intentionally.
		PE4, PE5		Can be configured as I/O ports when DREQ0, DREQ1 are not used.
85	88	DACK0	F	External transfer request acknowledge output pin for DMAC (ch. 0) This function is available when transfer request output for DMAC is enabled.
		PE6		Can be configured as the I/O port when DACK0 is not used. This function is available when transfer request acknowledge output for DMAC or DACK0 output is disabled.
84	87	DACK1	F	External transfer request acknowledge output pin for DMAC (ch. 1) This function is available when transfer request output for DMAC is enabled.
		PE7		Can be configured as the I/O port when DACK1 is not used. This function is available when transfer request output for DMAC or DACK1 output is disabled.
76	79	SI0	F	UART0 data input pin This pin is used for input during UART0 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		TRG0		PWM timer external trigger input pin This pin is used for input during PWM timer external trigger is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		PF0		Can be configured as the I/O port when SI0 and TRG0 are not used.

*1: FPT-100P-M05

*2: FPT-100P-M06

(Continued)

Pin no.		Pin name	Circuit type	Description
LQFP*1	QFP*2			
77	80	SO0	F	UART0 data output pin This function is available when UART0 data output is enabled.
		TRG1		PWM timer external trigger input pin This function is available when serial data output of PF1, UART0 are disabled.
		PF1		Can be configured as the I/O port when SO0 and TRG1 are not used. This function is available when serial data output of UART0 is disabled.
78	81	SC0	F	UART0 clock I/O pin Clock output is available when UART0 clock output is enabled.
		OCPA3		PWM timer output pin This function is available when PWM timer output is enabled.
		PF2		Can be configured as the I/O port when SC0 and OCPA3 are not used. This function is available when UART0 clock output is disabled.
79	82	SI1	F	UART1 data input pin This pin is used for input during UART1 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		TRG2		PWM timer external trigger input pin This pin is used for input during PWM timer external trigger is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		PF3		Can be configured as the I/O port when SI1 and TRG2 are not used.
80	83	SO1	F	UART1 data output pin This function is available when UART1 data output is enabled.
		TRG3		PWM timer external trigger input pin This function is available when PF4, UART1 data outputs are disabled.
		PF4		Can be configured as the I/O port when SO1 and TRG3 are not used. This function is available when UART1 data output is disabled.
81	84	SI2	F	UART2 data input pin This pin is used for input during UART2 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
		OCPA1		PWM timer output pin This function is available when PWM timer output is enabled.
		PF5		Can be configured as the I/O port when SI2 and OCPA1 are not used.

*1: FPT-100P-M05

*2: FPT-100P-M06

(Continued)

Pin no.		Pin name	Circuit type	Description
LQFP*1	QFP*2			
82	85	SO2	F	UART2 data output pin This function is available when UART2 data output is enabled.
		OCPA2		PWM timer output pin This function is available when PWM timer output is enabled.
		PF6		Can be configured as the I/O port when SO2 and OCPA2 are not used. This function is available when UART2 data output is disabled.
83	86	OCPA0	F	PWM timer output pin This function is available when PWM timer output is enabled.
		PF7		Can be configured as the I/O port when OCPA0 and $\overline{ATG}$ are not used. This function is available when PWM timer output is disabled.
		$\overline{ATG}$		External trigger input pin for A/D converter This pin is used for input when external trigger is selected to cause A/D converter operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
72 to 75	75 to 78	AN0 to AN3	D	Analog input pins of A/D converter
69	72	AV_{CC}	—	Power supply pin (V_{CC}) for A/D converter
70	73	AVRH	—	Reference voltage input (high) for A/D converter Make sure to turn on and off this pin with potential of AVRH or more applied to AV_{CC}.
71	74	AV_{SS} / AVRL	—	Power supply pin (V_{SS}) for A/D converter and reference voltage input pin (low)
43, 93	46, 96	$V_{CC}5$	—	5 V power supply pin (V_{CC}) for digital circuit Always two pins must be connected to the power supply (connect to 3 V power supply when operating at 3 V).
4	7	$V_{CC}3$	—	Bypass capacitor pin for internal capacitor. Also connect this pin to 3 V power supply when operating at 3 V.
15, 40, 65, 90	18, 43, 68, 93	V_{SS}	—	Earth level (V_{SS}) for digital circuit

*1: FPT-100P-M05

*2: FPT-100P-M06

Note: In most of the above pins, I/O ports and resource I/O are multiplexed, e.g. P82 and BRQ. In case of conflict between output of I/O ports and resource I/O, priority is always given to the output of resource I/O.

MB91101/MB91101A

■ DRAM CONTROL PIN

Pin name	Data bus 16-bit mode		Data bus 8-bit mode	Remarks
	2CAS/1WR mode	1CAS/2WR mode	—	
RAS0	Area 4 RAS	Area 4 RAS	Area 4 RAS	Correspondence of "L", "H" to lower address 1 bit (A0) in data bus 16-bit mode "L": "0" "H": "1" CASL:CAS which A0 corresponds to "0" area CASH:CAS which A0 corresponds to "1" area $\overline{\text{WEL}}$: $\overline{\text{WE}}$ which A0 corresponds to "0" area $\overline{\text{WEH}}$:$\overline{\text{WE}}$ which A0 corresponds to "1" area
RAS1	Area 5 RAS	Area 5 RAS	Area 5 RAS	
CS0L	Area 4 CASL	Area 4 CAS	Area 4 CAS	
CS0H	Area 4 CASH	Area 4 $\overline{\text{WEL}}$	Area 4 CAS	
CS1L	Area 5 CASL	Area 5 CAS	Area 5 CAS	
CS1H	Area 5 CASH	Area 5 $\overline{\text{WEL}}$	Area 5 CAS	
$\overline{\text{DW0}}$	Area 4 $\overline{\text{WE}}$	Area 4 $\overline{\text{WEH}}$	Area 4 $\overline{\text{WE}}$	
$\overline{\text{DW1}}$	Area 5 $\overline{\text{WE}}$	Area 5 $\overline{\text{WEH}}$	Area 5 $\overline{\text{WE}}$	
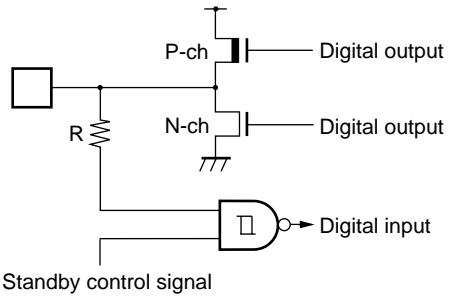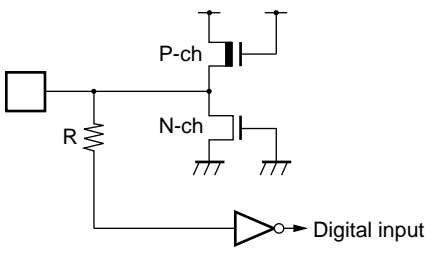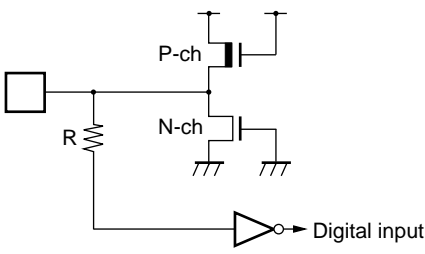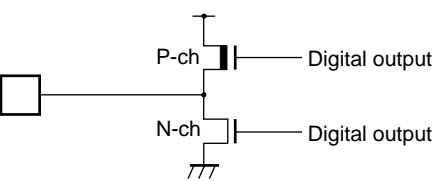
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	X1 / X0 / Clock input / Standby control signal	• Oscillation feedback resistance 1 MΩ approx. With standby control
B	V_{CC} / P-ch / P-ch / N-ch / R / V_{SS} / Digital input	• CMOS level Hysteresis input Without standby control With pull-up resistance
C	P-ch / Digital output / N-ch / Digital output / R / Digital input / Standby control signal	• CMOS level I/O With standby control
D	P-ch / Digital output / N-ch / Digital output / R / Analog input	• Analog input

(Continued)

(Continued)

Type	Circuit	Remarks
F		• CMOS level output • CMOS level Hysteresis input With standby control
G		• CMOS level input Without standby control
H		• CMOS level Hysteresis input Without standby control
L		• CMOS level output

■ HANDLING DEVICES

1. Preventing Latchup

In CMOS ICs, applying voltage higher than V_{CC} or lower than V_{SS} to input/output pin or applying voltage over rating across V_{CC} and V_{SS} may cause latchup.
This phenomenon rapidly increases the power supply current, which may result in thermal breakdown of the device. Make sure to prevent the voltage from exceeding the maximum rating.
Take care that the analog power supply (AV_{CC}, AVRH) and the analog input do not exceed the digital power supply (V_{CC}) when the analog power supply turned on or off.

2. Treatment of Unused Pins

Unused pins left open may cause malfunctions. Make sure to connect them to pull-up or pull-down resistors.

3. External Reset Input

It takes at least 5 machine cycle to input "L" level to the $\overline{RST}$ pin and to ensure inner reset operation properly.

4. Remarks for External Clock Operation

When external clock is selected, supply it to X0 pin generally, and simultaneously the opposite phase clock to X0 must be supplied to X1 pin. However, in this case the stop mode must not be used (because X1 pin stops at "H" output in stop mode).
And it can be used to supply only to X0 pin with 5 V power supply at 12.5 MHz and less than.

• Using an external clock

X0
X1
MB91101/MB91101A
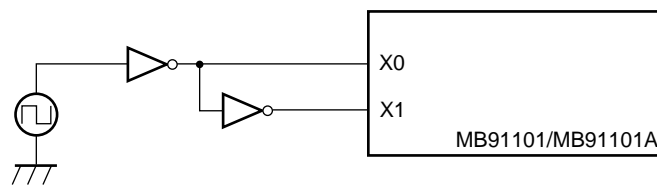
Using an external clock (normal)
Note: Stop mode (oscillation stop mode) can not be used.

X0
Open ——— X1
MB91101/MB91101A
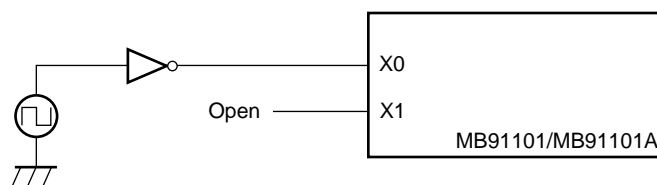
Using an external clock (can be used at 12.5 MHz and less than.)
(5 V power supply only)

5. Power Supply Pins

When there are several V_{CC} and V_{SS} pins, each of them is equipotentially connected to its counterpart inside of the device, minimizing the risk of malfunctions such as latch up. To further reduce the risk of malfunctions, to prevent EMI radiation, to prevent strobe signal malfunction resulting from creeping-up of ground level and to observe the total output current standard, connect all V_{CC} and V_{SS} pins to the power supply or GND.
It is preferred to connect V_{CC} and V_{SS} of the MB91101and MB91101A to power supply with minimal impedance possible.
It is also recommended to connect a ceramic capacitor as a bypass capacitor of about 0.1 µF between V_{CC} and V_{SS} at a position as close as possible to the MB91101 and MB91101A.

The MB91101 and MB91101A have an internal regulator. When using with 5 V power supply, supply 5 V to $V_{CC}5$ pin and make sure to connect about 0.1 µF bypass capacitor to $V_{CC}3$ pin for regulator. And another 3 V power supply is needed for the A/D convertor. When using with 3 V power supply, connect both $V_{CC}5$ pin and $V_{CC}3$ pin to the 3 V power supply.

• **Connecting to a power supply**

[Using with 5 V power supply]

[Using with 3 V power supply]
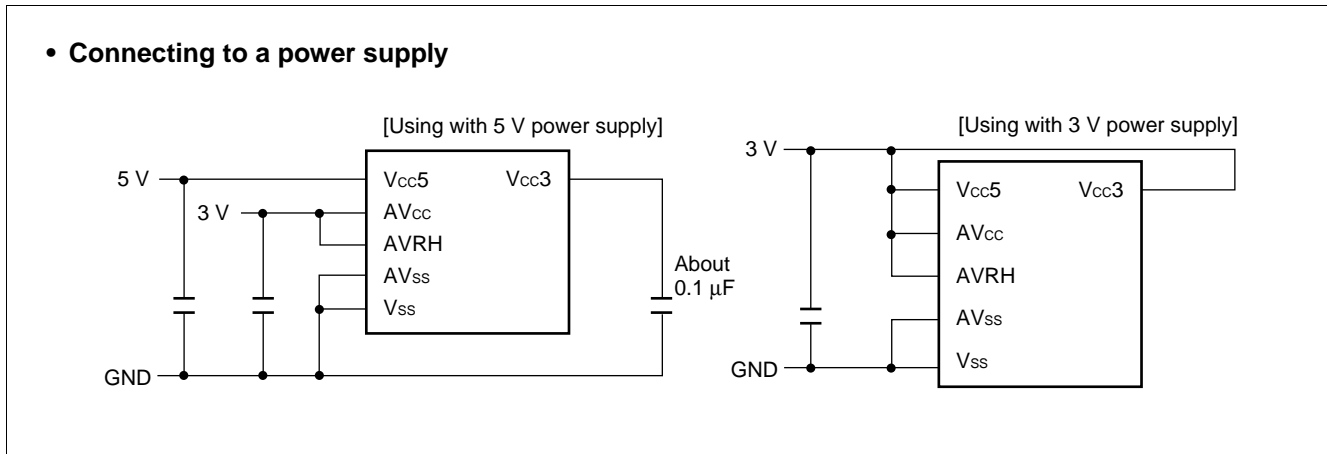
6. Crystal Oscillator Circuit

Noises around X0 and X1 pins may cause malfunctions of the MB91101 and MB91101A. In designing the PC board, layout X0 and X1 pins, crystal oscillator (or ceramic oscillator) and bypass capacitor for grounding as close as possible.
It is strongly recommended to design PC board so that X1 and X0 pins are surrounded by grounding area for stable operation.

7. Turning-on Sequence of A/D Converter Power Supply and Analog Input

Make sure to turn on the digital power supply (V_{CC}) before turning on the A/D converter (AV_{CC}, AVRH) and applying voltage to analog input (AN0 to AN3).
Make sure to turn off digital power supply after power supply to A/D converters and analog inputs have been switched off. (There are no such limitations in turning on power supplies. Analog and digital power supplies may be turned on simultaneously.) Make sure that AVRH never exceeds AV_{CC} when turning on/off power supplies.

8. Fluctuation of Power Supply Voltage

Warranty range for normal operation against fluctuation of power supply voltage V_{CC} is as given in rating. However, sudden fluctuation of power supply voltage within the warranty range may cause malfunctions. It is recommended to make every effort to stabilize the power supply voltage to IC. It is also recommended that by controlling power supply as a reference of stabilizing, V_{CC} ripple fluctuation (P-P value) at the commercial frequency (50 Hz to 60 Hz) should be less than 10% of the standard V_{CC} value and the transient regulation should be less than 0.1 V/ms at instantaneous deviation like turning off the power supply.

9. Mode Setting Pins (MD0 to MD2)

Connect mode setting pins (MD0 to MD2) directly to V_{CC} or V_{SS}.
Arrange each mode setting pin and V_{CC} or V_{SS} patterns on the printed circuit board as close as possible and make the impedance between them minimal to prevent mistaken entrance to the test mode caused by noises.

10. Internal DC Regulator

Internal DC regulator stops in stop mode. When the regulator stops owing to the increase of inner leakage current (ICCH) in stop mode, malfunction caused by noise or any troubles about power supply in normal operation, the internal 3 V power supply voltage may decrease less than the warranty range for normal operation. So when using the internal regulator and stop mode with 5 V power supply, never fail to support externally so that 3 V power supply voltage might not decrease. However, even in such a case, the internal regulator can be restarted

by inputting the reset procedure. (In this case, set the reset to "L" level within the oscillation stabilizing waiting time.)

• **Using STOP mode with 5 V power supply**

5 V

V_{CC}5

V_{CC}3

V_{SS}

3.6 kΩ

6.8 kΩ

0.1 μF
approx.

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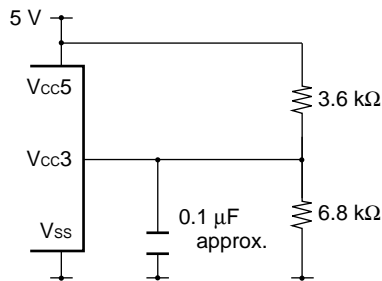
11. Pin Condition at Turning on the Power Supply

The pin condition at turning on the power supply is unstable. The circuit starts being initialized after turning on the power supply and then starting oscillation and then the operation of the internal regulator becomes stable. So it takes about 42 ms for the pin to be initialized from the oscillation starting at the source oscillation 12.5 MHz. Take care that the pin condition may be output condition at initial unstable condition.
(With the MB91101A, however, initalization can be achieved in less than about 42 ms after turning on the internal power supply by maintaining the $\overline{RST}$ pin at "L" level.)

12. Source Oscillation Input at Turning on the Power Supply

At turning on the power supply, never fail to input the clock before cancellation of the oscillation stabilizing waiting.

13. Hardware Stand-by at Turning on the Power Supply

When turning on the power supply with the $\overline{HST}$ pin being set to "L" level, the hardware doesn't stand by. However the $\overline{HST}$ pin becomes available after the reset cancellation, the $\overline{HST}$ pin must once be back to "H" level.

14. Power on Reset

Make sure to make power on reset at turning on the power supply or returning on the power supply when the power supply voltage is below the warranty range for normal operation.

15. Notes on during operation of PLL clock mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self oscillating circuit evevn when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

16. Watchdog timer function

The watchdog timer supported by the FR family monitors the program that performs the reset delay operation for a specified time. If the program hangs and the reset delay operation is not performed, the watchdog timer resets the CPU. Therefore, once the watchdog timer is enabled, operation continues until the CPU is reset. As an exception, a reset delay automatically occurs if the CPU stops program execution.

MB91101/MB91101A

■ BLOCK DIAGRAM

Note: Pins are display for functions (Actually some pins are multiplexer).
When using REALOS, time control should be done by using external interrupt or inner timer.
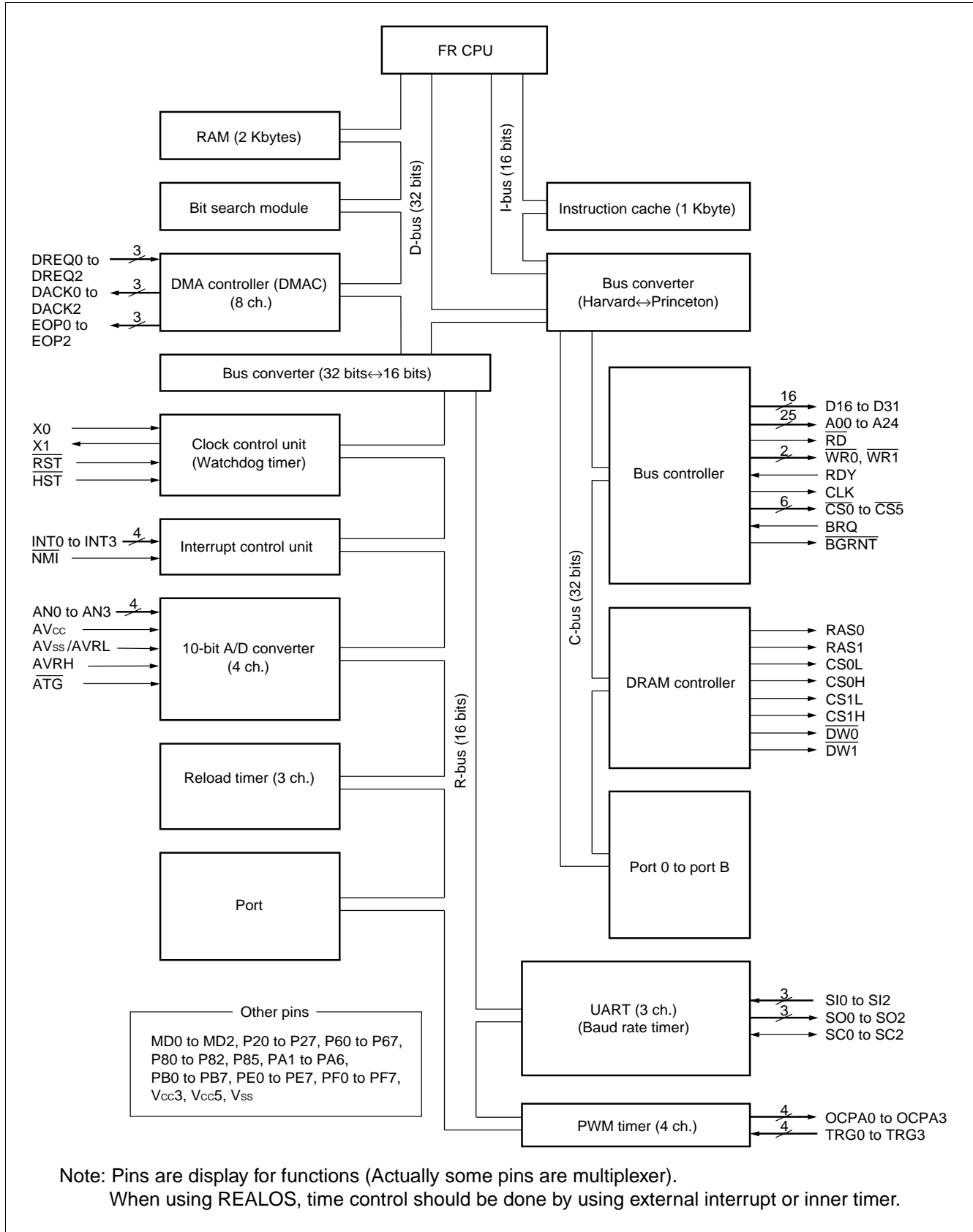
■ CPU CORE

1. Memory Space

The FR family has a logical address space of 4 Gbytes (2^{32} bytes) and the CPU linearly accesses the memory space.

• **Memory space**

Address   External ROM/external bus mode

0000 0000$_H$

I/O area   } Direct addressing area

0000 0400$_H$

I/O area   See "■ I/O MAP"

0000 0800$_H$

Access inhibited

0000 1000$_H$

Embedded RAM

0000 1800$_H$

Access inhibited

0001 0000$_H$

External area

FFFF FFFF$_H$
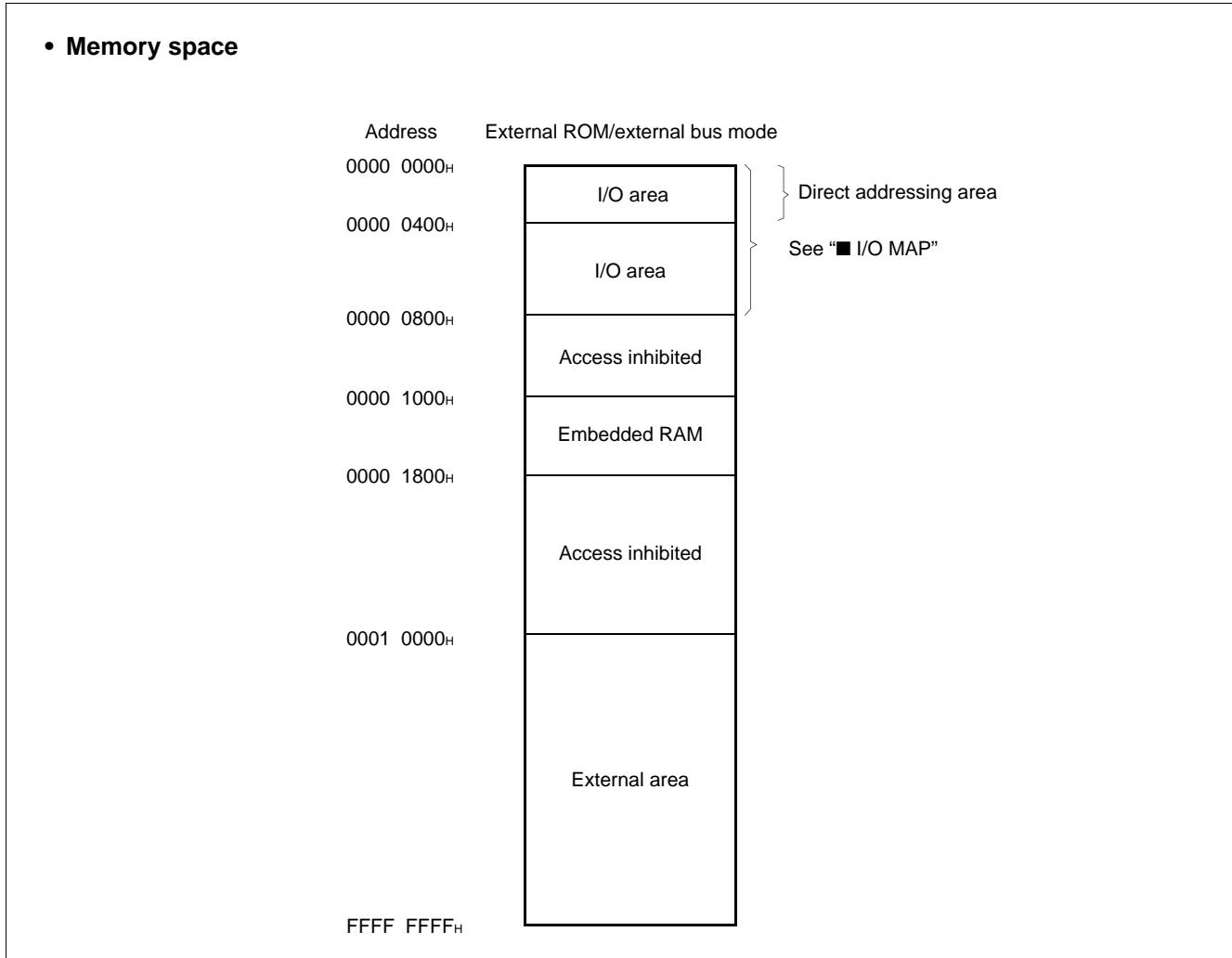
• **Direct addressing area**

The following areas on the memory space are assigned to direct addressing area for I/O. In these areas, an address can be specified in a direct operand of a code.

Direct areas consists of the following areas dependent on accessible data sizes.

Byte data access: 000$_H$ to 0FF$_H$

Half word data access: 000$_H$ to 1FF$_H$

Word data access: 000$_H$ to 3FF$_H$

2. Registers

The FR family has two types of registers; dedicated registers embedded on the CPU and general-purpose registers on memory.

• Dedicated registers

Program counter (PC):   32-bit length, indicates the location of the instruction to be executed.
Program status (PS):   32-bit length, register for storing register pointer or condition codes
Table base register (TBR): Holds top address of vector table used in EIT (Exceptional/Interrupt/Trap) processing.
Return pointer (RP):   Holds address to resume operation after returning from a subroutine.
System stack pointer (SSP): Indicates system stack space.
User's stack pointer (USP): Indicates user's stack space.
Multiplication/division result register (MDH/MDL): 32-bit length, register for multiplication/division

		Initial value	
32 bits			
PC	Program counter	XXXX XXXX$_H$	Indeterminate
PS	Program status		
TBR	Table base register	000F FC00$_H$	
RP	Return pointer	XXXX XXXX$_H$	Indeterminate
SSP	System stack pointer	0000 0000 $_H$	
USP	User's stack pointer	XXXX XXXX$_H$	Indeterminate
MDH	Multiplication/division result register	XXXX XXXX$_H$	Indeterminate
MDL		XXXX XXXX$_H$	Indeterminate

• Program status (PS)

The PS register is for holding program status and consists of a condition code register (CCR), a system condition code register (SCR) and a interrupt level mask register (ILM).

	31 to 21	20	19	18	17	16	15 to 11	10	9	8	7	6	5	4	3	2	1	0
PS	—	ILM4	ILM3	ILM2	ILM1	ILM0	—	D1	D0	T	—	—	S	I	N	Z	V	C
				ILM					SCR						CCR			
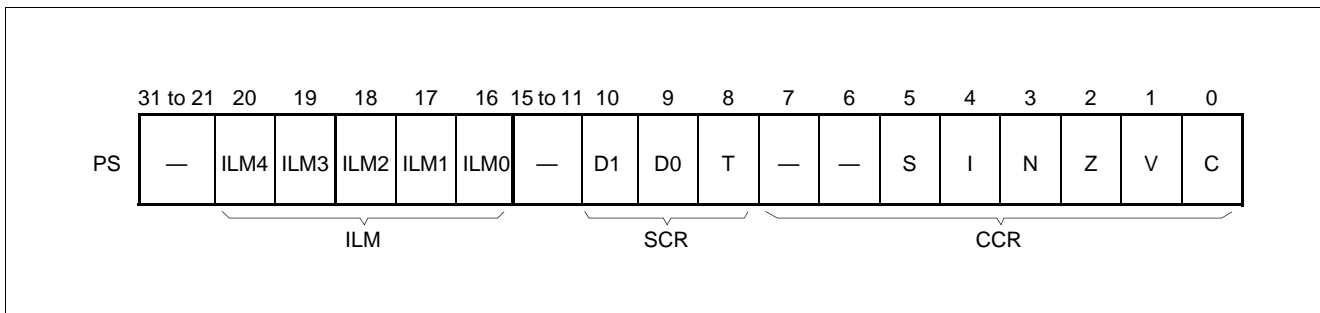
• **Condition code register (CCR)**

    S-flag: Specifies a stack pointer used as R15.
    I-flag: Controls user interrupt request enable/disable.
    N-flag: Indicates sign bit when division result is assumed to be in the 2's complement format.
    Z-flag: Indicates whether or not the result of division was "0".
    V-flag: Assumes the operand used in calculation in the 2's complement format and indicates whether or not overflow has occurred.
    C-flag: Indicates if a carry or borrow from the MSB has occurred.

• **System condition code register (SCR)**

    T-flag: Specifies whether or not to enable step trace trap.

• **Interrupt level mask register (ILM)**

    ILM4 to ILM0: Register for holding interrupt level mask value. The value held by this register is used as a level mask. When an interrupt request issued to the CPU is higher than the level held by ILM, the interrupt request is accepted.

ILM4	ILM3	ILM2	ILM1	ILM0	Interrupt level	High-low
0	0	0	0	0	0	High
:		:			:	
0	1	0	0	0	15	
:		:			:	
1	1	1	1	1	31	Low

■ GENERAL-PURPOSE REGISTERS

R0 to R15 are general-purpose registers embedded on the CPU. These registers functions as an accumulator and a memory access pointer (field for indicating address).

• **Register bank structure**
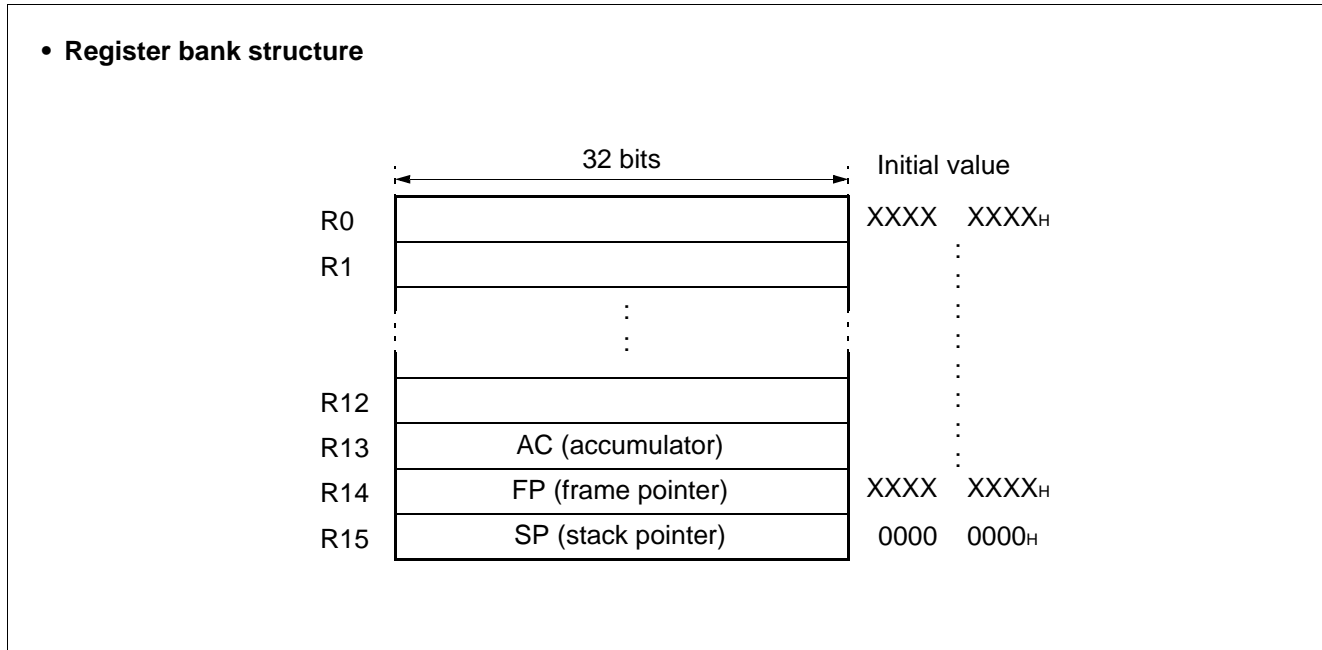
Of the above 16 registers, following registers have special functions. To support the special functions, part of the instruction set has been sophisticated to have enhanced functions.

R13: Virtual accumulator (AC)
R14: Frame pointer (FP)
R15: Stack pointer (SP)

Upon reset, values in R0 to R14 are not fixed. Value in R15 is initialized to be 0000 0000$_H$ (SSP value).

■ SETTING MODE

1. Pin
• **Mode setting pins and modes**

Mode setting pins			Mode name	Reset vector access area	External data bus width	Bus mode
MD2	MD1	MD0				
0	0	0	External vector mode 0	External	8 bits	External ROM/external bus mode
0	0	1	External vector mode 1	External	16 bits	
0	1	0	—	—	—	Inhibited
0	1	1	Internal vector mode	Internal	(Mode register)	Single-chip mode*
1	—	—	—	—	—	Inhibited

*: The MB91101 and MB91101A do not support single-chip mode.

2. Registers
• **Mode setting registers (MODR) and modes**

Address 0000 07FF$_H$ | M1 | M0 | * | * | * | * | * | * | Initial value XXXX XXXX$_B$ | Access W

Bus mode setting bit

W : Write only
X : Indeterminate
* : Always write "0" except for M1 and M0.
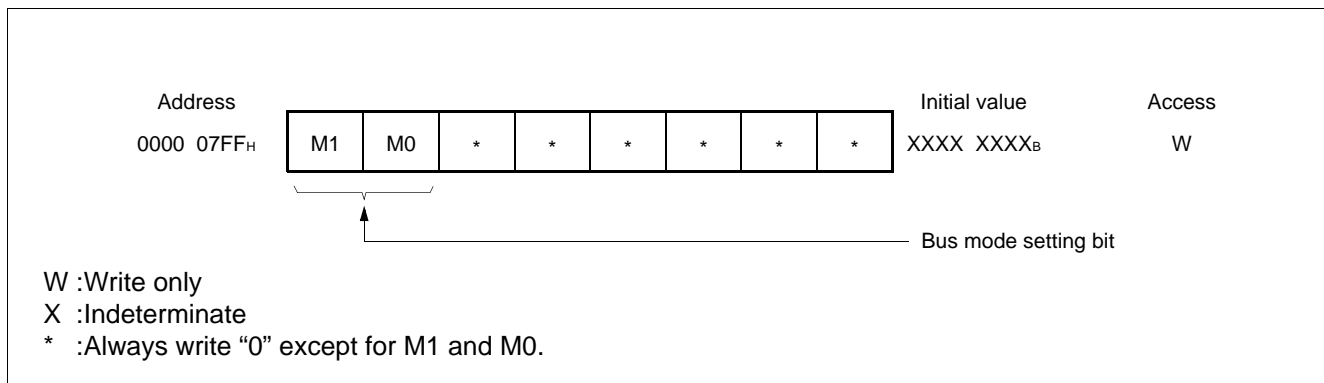
• **Bus mode setting bits and functions**

M1	M0	Functions	Note
0	0	Single-chip mode	
0	1	Internal ROM/external bus mode	
1	0	External ROM/external bus mode	
1	1	—	Inhibited

Note: Because of without internal ROM, the MB91101 and MB91101A allow "10$_B$" setting value only.

■ I/O MAP

Address	Abbreviation	Register name	Read/write	Initial value
0000$_H$		(Reserved)		
0001$_H$	PDR2	Port 2 data register	R/W	XXXXXXXX$_B$
0002$_H$ to 0004$_H$		(Reserved)		
0005$_H$	PDR6	Port 6 data register	R/W	XXXXXXXX$_B$
0006$_H$		(Reserved)		
0007$_H$				
0008$_H$	PDRB	Port B data register	R/W	XXXXXXXX$_B$
0009$_H$	PDRA	Port A data register	R/W	_ XXXXXX _$_B$
000A$_H$		(Reserved)		
000B$_H$	PDR8	Port 8 data register	R/W	_ _ X _ _ XXX$_B$
000C$_H$ to 0011$_H$		(Reserved)		
0012$_H$	PDRE	Port E data register	R/W	XXXXXXXX$_B$
0013$_H$	PDRF	Port F data register	R/W	XXXXXXXX$_B$
0014$_H$ to 001B$_H$		(Reserved)		
001C$_H$	SSR0	Serial status register 0	R/W	0 0 0 0 1 _ 0 0$_B$
001D$_H$	SIDR0/SODR0	Serial input register 0/serial output register 0	R/W	XXXXXXXX$_B$
001E$_H$	SCR0	Serial control register 0	R/W	0 0 0 0 0 1 0 0$_B$
001F$_H$	SMR0	Serial mode register 0	R/W	0 0 _ _ 0 _ 0 0$_B$
0020$_H$	SSR1	Serial status register 1	R/W	0 0 0 0 1 _ 0 0$_B$
0021$_H$	SIDR1/SODR1	Serial input register 1/serial output register 1	R/W	XXXXXXXX$_B$
0022$_H$	SCR1	Serial control register 1	R/W	0 0 0 0 0 1 0 0$_B$
0023$_H$	SMR2	Serial mode register 1	R/W	0 0 _ _ 0 _ 0 0$_B$
0024$_H$	SSR2	Serial status register 2	R/W	0 0 0 0 1 _ 0 0$_B$
0025$_H$	SIDR2/SODR2	Serial input register 2/serial output register 2	R/W	XXXXXXXX$_B$
0026$_H$	SCR2	Serial control register 2	R/W	0 0 0 0 0 1 0 0$_B$
0027$_H$	SMR2	Serial mode register 2	R/W	0 0 _ _ 0 _ 0 0$_B$

(Continued)

Address	Abbreviation	Register name	Read/write	Initial value
0028H	TMRLR0	16-bit reload register ch. 0	W	XXXXXXXX$_B$
0029H				XXXXXXXX$_B$
002AH	TMR0	16-bit timer register ch. 0	R	XXXXXXXX$_B$
002BH				XXXXXXXX$_B$
002CH	(Reserved)			
002DH				
002EH	TMCSR0	16-bit reload timer control status register ch. 0	R/W	_ _ _ _ 0 0 0 0$_B$
002FH				0 0 0 0 0 0 0 0$_B$
0030H	TMRLR1	16-bit reload register ch. 1	W	XXXXXXXX$_B$
0031H				XXXXXXXX$_B$
0032H	TMR1	16-bit timer register ch. 1	R	XXXXXXXX$_B$
0033H				XXXXXXXX$_B$
0034H	(Reserved)			
0035H				
0036H	TMCSR1	16-bit reload timer control status register ch. 1	R/W	_ _ _ _ 0 0 0 0$_B$
0037H				0 0 0 0 0 0 0 0$_B$
0038H	ADCR	A/D converter data register	R	_ _ _ _ _ _ XX$_B$
0039H				XXXXXXXX$_B$
003AH	ADCS	A/D converter control status register	R/W	0 0 0 0 0 0 0 0$_B$
003BH				0 0 0 0 0 0 0 0$_B$
003CH	TMRLR2	16-bit reload register ch. 2	W	XXXXXXXX$_B$
003DH				XXXXXXXX$_B$
003EH	TMR2	16-bit timer register ch. 2	R	XXXXXXXX$_B$
003FH				XXXXXXXX$_B$
0040H	(Reserved)			
0041H				
0042H	TMCSR2	16-bit reload timer control status register ch. 2	R/W	_ _ _ _ 0 0 0 0$_B$
0043H				0 0 0 0 0 0 0 0$_B$
0044H to 0077H	(Reserved)			

(Continued)

Address	Abbreviation	Register name	Read/write	Initial value
0078$_H$	UTIM0/UTIMR0	U-TIMER register ch. 0/reload register ch. 0	R/W	0 0 0 0 0 0 0 0$_B$
0079$_H$				0 0 0 0 0 0 0 0$_B$
007A$_H$	(Reserved)			
007B$_H$	UTIMC0	U-TIMER control register ch. 0	R/W	0 _ _ 0 0 0 0 1$_B$
007C$_H$	UTIM1/UTIMR1	U-TIMER register ch. 1/reload register ch. 1	R/W	0 0 0 0 0 0 0 0$_B$
007D$_H$				0 0 0 0 0 0 0 0$_B$
007E$_H$	(Reserved)			
007F$_H$	UTIMC1	U-TIMER control register ch. 1	R/W	0 _ _ 0 0 0 0 1$_B$
0080$_H$	UTIM2/UTIMR2	U-TIMER register ch. 2/reload register ch. 2	R/W	0 0 0 0 0 0 0 0$_B$
0081$_H$				0 0 0 0 0 0 0 0$_B$
0082$_H$	(Reserved)			
0083$_H$	UTIMC2	U-TIMER control register ch. 2	R/W	0 _ _ 0 0 0 0 1$_B$
0084$_H$ to 0093$_H$	(Reserved)			
0094$_H$	EIRR	External interrupt cause register	R/W	0 0 0 0 0 0 0 0$_B$
0095$_H$	ENIR	Interrupt enable register	R/W	0 0 0 0 0 0 0 0$_B$
0096$_H$ to 0098$_H$	(Reserved)			
0099$_H$	ELVR	External interrupt request level setting register	R/W	0 0 0 0 0 0 0 0$_B$
009A$_H$ to 00D1$_H$	(Reserved)			
00D2$_H$	DDRE	Port E data direction register	W	0 0 0 0 0 0 0 0$_B$
00D3$_H$	DDRF	Port F data direction register	W	0 0 0 0 0 0 0 0$_B$
00D4$_H$ to 00DB$_H$	(Reserved)			
00DC$_H$	GCN1	General control register 1	R/W	0 0 1 1 0 0 1 0$_B$
00DD$_H$				0 0 0 1 0 0 0 0$_B$
00DE$_H$	(Reserved)			
00DF$_H$	GCN2	General control register 2	R/W	0 0 0 0 0 0 0 0$_B$

(Continued)

26

Address	Abbreviation	Register name	Read/write	Initial value
00E0H	PTMR0	Ch. 0 timer register	R	1 1 1 1 1 1 1 1B
00E1H				1 1 1 1 1 1 1 1B
00E2H	PCSR0	Ch. 0 cycle setting register	W	XXXXXXXXB
00E3H				XXXXXXXXB
00E4H	PDUT0	Ch. 0 duty setting register	W	XXXXXXXXB
00E5H				XXXXXXXXB
00E6H	PCNH0	Ch. 0 control status register H	R/W	0 0 0 0 0 0 0 _B
00E7H	PCNL0	Ch. 0 control status register L	R/W	0 0 0 0 0 0 0 0B
00E8H	PTMR1	Ch. 1 timer register	R	1 1 1 1 1 1 1 1B
00E9H				1 1 1 1 1 1 1 1B
00EAH	PCSR1	Ch. 1 cycle setting register	W	XXXXXXXXB
00EBH				XXXXXXXXB
00ECH	PDUT1	Ch. 1 duty setting register	W	XXXXXXXXB
00EDH				XXXXXXXXB
00EEH	PCNH1	Ch. 1 control status register H	R/W	0 0 0 0 0 0 0 _B
00EFH	PCNL1	Ch. 1 control status register L	R/W	0 0 0 0 0 0 0 0B
00F0H	PTMR2	Ch. 2 timer register	R	1 1 1 1 1 1 1 1B
00F1H				1 1 1 1 1 1 1 1B
00F2H	PCSR2	Ch. 2 cycle setting register	W	XXXXXXXXB
00F3H				XXXXXXXXB
00F4H	PDUT2	Ch. 2 duty setting register	W	XXXXXXXXB
00F5H				XXXXXXXXB
00F6H	PCNH2	Ch. 2 control status register H	R/W	0 0 0 0 0 0 0 _B
00F7H	PCNL2	Ch. 2 control status register L	R/W	0 0 0 0 0 0 0 0B
00F8H	PTMR3	Ch. 3 timer register	R	1 1 1 1 1 1 1 1B
00F9H				1 1 1 1 1 1 1 1B
00FAH	PCSR3	Ch. 3 cycle setting register	W	XXXXXXXXB
00FBH				XXXXXXXXB
00FCH	PDUT3	Ch. 3 duty setting register	W	XXXXXXXXB
00FDH				XXXXXXXXB
00FEH	PCNH3	Ch. 3 control status register H	R/W	0 0 0 0 0 0 0 _B
00FFH	PCNL3	Ch. 3 control status register L	R/W	0 0 0 0 0 0 0 0B

(Continued)

Address	Abbreviation	Register name	Read/write	Initial value
0100_H to 01FF_H	(Reserved)			
0200_H	DPDP	DMAC parameter descriptor pointer	R/W	XXXXXXXX_B
0201_H				XXXXXXXX_B
0202_H				XXXXXXXX_B
0203_H				X 0 0 0 0 0 0 0_B
0204_H	DACSR	DMAC control status register	R/W	0 0 0 0 0 0 0 0_B
0205_H				0 0 0 0 0 0 0 0_B
0206_H				0 0 0 0 0 0 0 0_B
0207_H				0 0 0 0 0 0 0 0_B
0208_H	DATCR	DMAC pin control register	R/W	XXXXXXXX_B
0209_H				XXXX 0 0 0 0_B
020A_H				XXXX 0 0 0 0_B
020B_H				XXXX 0 0 0 0_B
020C_H to 03E3_H	(Reserved)			
03E4_H	ICHCR	Instruction cache control register	R/W	_ _ _ _ _ _ _ __B
03E5_H				_ _ _ _ _ _ _ __B
03E6_H				_ _ _ _ _ _ _ __B
03E7_H				_ _ 0 0 0 0 0 0_B
03E8_H to 03EF_H	(Reserved)			
03F0_H	BSD0	Bit search module 0-detection data register	W	XXXXXXXX_B
03F1_H				XXXXXXXX_B
03F2_H				XXXXXXXX_B
03F3_H				XXXXXXXX_B
03F4_H	BSD1	Bit search module 1-detection data register	R/W	XXXXXXXX_B
03F5_H				XXXXXXXX_B
03F6_H				XXXXXXXX_B
03F7_H				XXXXXXXX_B

(Continued)

Address	Abbreviation	Register name	Read/write	Initial value
03F8$_H$	BSDC	Bit search module transition-detection data register	W	XXXXXXXX$_B$
03F9$_H$				XXXXXXXX$_B$
03FA$_H$				XXXXXXXX$_B$
03FB$_H$				XXXXXXXX$_B$
03FC$_H$	BSRR	Bit search module detection result register	R	XXXXXXXX$_B$
03FD$_H$				XXXXXXXX$_B$
03FE$_H$				XXXXXXXX$_B$
03FF$_H$				XXXXXXXX$_B$
0400$_H$	ICR00	Interrupt control register 0	R/W	_ _ _ 1 1 1 1 1$_B$
0401$_H$	ICR01	Interrupt control register 1	R/W	_ _ _ 1 1 1 1 1$_B$
0402$_H$	ICR02	Interrupt control register 2	R/W	_ _ _ 1 1 1 1 1$_B$
0403$_H$	ICR03	Interrupt control register 3	R/W	_ _ _ 1 1 1 1 1$_B$
0404$_H$	ICR04	Interrupt control register 4	R/W	_ _ _ 1 1 1 1 1$_B$
0405$_H$	ICR05	Interrupt control register 5	R/W	_ _ _ 1 1 1 1 1$_B$
0406$_H$	ICR06	Interrupt control register 6	R/W	_ _ _ 1 1 1 1 1$_B$
0407$_H$	ICR07	Interrupt control register 7	R/W	_ _ _ 1 1 1 1 1$_B$
0408$_H$	ICR08	Interrupt control register 8	R/W	_ _ _ 1 1 1 1 1$_B$
0409$_H$	ICR09	Interrupt control register 9	R/W	_ _ _ 1 1 1 1 1$_B$
040A$_H$	ICR10	Interrupt control register 10	R/W	_ _ _ 1 1 1 1 1$_B$
040B$_H$	ICR11	Interrupt control register 11	R/W	_ _ _ 1 1 1 1 1$_B$
040C$_H$	ICR12	Interrupt control register 12	R/W	_ _ _ 1 1 1 1 1$_B$
040D$_H$	ICR13	Interrupt control register 13	R/W	_ _ _ 1 1 1 1 1$_B$
040E$_H$	ICR14	Interrupt control register 14	R/W	_ _ _ 1 1 1 1 1$_B$
040F$_H$	ICR15	Interrupt control register 15	R/W	_ _ _ 1 1 1 1 1$_B$
0410$_H$	ICR16	Interrupt control register 16	R/W	_ _ _ 1 1 1 1 1$_B$
0411$_H$	ICR17	Interrupt control register 17	R/W	_ _ _ 1 1 1 1 1$_B$
0412$_H$	ICR18	Interrupt control register 18	R/W	_ _ _ 1 1 1 1 1$_B$
0413$_H$	ICR19	Interrupt control register 19	R/W	_ _ _ 1 1 1 1 1$_B$
0414$_H$	ICR20	Interrupt control register 20	R/W	_ _ _ 1 1 1 1 1$_B$
0415$_H$	ICR21	Interrupt control register 21	R/W	_ _ _ 1 1 1 1 1$_B$
0416$_H$	ICR22	Interrupt control register 22	R/W	_ _ _ 1 1 1 1 1$_B$

(Continued)

Address	Abbreviation	Register name	Read/write	Initial value
0417_H	ICR23	Interrupt control register 23	R/W	_ _ _ 1 1 1 1 1_B
0418_H	ICR24	Interrupt control register 24	R/W	_ _ _ 1 1 1 1 1_B
0419_H	ICR25	Interrupt control register 25	R/W	_ _ _ 1 1 1 1 1_B
$041A_H$	ICR26	Interrupt control register 26	R/W	_ _ _ 1 1 1 1 1_B
$041B_H$	ICR27	Interrupt control register 27	R/W	_ _ _ 1 1 1 1 1_B
$041C_H$	ICR28	Interrupt control register 28	R/W	_ _ _ 1 1 1 1 1_B
$041D_H$	ICR29	Interrupt control register 29	R/W	_ _ _ 1 1 1 1 1_B
$041E_H$	ICR30	Interrupt control register 30	R/W	_ _ _ 1 1 1 1 1_B
$041F_H$	ICR31	Interrupt control register 31	R/W	_ _ _ 1 1 1 1 1_B
$042F_H$	ICR47	Interrupt control register 47	R/W	_ _ _ 1 1 1 1 1_B
0430_H	DICR	Delayed interrupt control register	R/W	_ _ _ _ _ _ _ 0_B
0431_H	HRCL	Hold request cancel request level setting register	R/W	_ _ _ 1 1 1 1 1_B
0432_H to $047F_H$		(Reserved)		
0480_H	RSRR/WTCR	Reset cause register/ watchdog peripheral control register	R/W	1 XXXX _ 0 0_B
0481_H	STCR	Standby control register	R/W	0 0 0 1 1 1 _ $_B$
0482_H	PDRR	DMA controller request squelch register	R/W	_ _ _ _ 0 0 0 0_B
0483_H	CTBR	Timebase timer clear register	W	XXXXXXXX_B
0484_H	GCR	Gear control register	R/W	1 1 0 0 1 1 _ 1_B
0485_H	WPR	Watchdog reset occurrence postpone register	W	XXXXXXXX_B
0486_H		(Reserved)		
0487_H				
0488_H	PCTR	PLL control register	R/W	0 0 _ _ 0 _ _ $_B$
0489_H to 0600_H		(Reserved)		
0601_H	DDR2	Port 2 data direction register	W	0 0 0 0 0 0 0 0_B
0602_H to 0604_H		(Reserved)		
0605_H	DDR6	Port 6 data direction register	W	0 0 0 0 0 0 0 0_B
0606_H		(Reserved)		
0607_H				

(Continued)

Address	Abbreviation	Register name	Read/write	Initial value
0608H	DDRB	Port B data direction register	W	0 0 0 0 0 0 0 0B
0609H	DDRA	Port A data direction register	W	_ 0 0 0 0 0 0 _B
060AH		(Reserved)		
060BH	DDR8	Port 8 data direction register	W	_ _ 0 _ _ 0 0 0B
060CH	ASR1	Area select register 1	W	0 0 0 0 0 0 0 0B
060DH				0 0 0 0 0 0 0 1B
060EH	AMR1	Area mask register 1	W	0 0 0 0 0 0 0 0B
060FH				0 0 0 0 0 0 0 0B
0610H	ASR2	Area select register 2	W	0 0 0 0 0 0 0 0B
0611H				0 0 0 0 0 0 1 0B
0612H	AMR2	Area mask register 2	W	0 0 0 0 0 0 0 0B
0613H				0 0 0 0 0 0 0 0B
0614H	ASR3	Area select register 3	W	0 0 0 0 0 0 0 0B
0615H				0 0 0 0 0 0 1 1B
0616H	AMR3	Area mask register 3	W	0 0 0 0 0 0 0 0B
0617H				0 0 0 0 0 0 0 0B
0618H	ASR4	Area select register 4	W	0 0 0 0 0 0 0 0B
0619H				0 0 0 0 0 1 0 0B
061AH	AMR4	Area mask register 4	W	0 0 0 0 0 0 0 0B
061BH				0 0 0 0 0 0 0 0B
061CH	ASR5	Area select register 5	W	0 0 0 0 0 0 0 0B
061DH				0 0 0 0 0 1 0 1B
061EH	AMR5	Area mask register 5	W	0 0 0 0 0 0 0 0B
061FH				0 0 0 0 0 0 0 0B
0620H	AMD0	Area mode register 0	R/W	_ _ _ 0 0 1 1 1B
0621H	AMD1	Area mode register 1	R/W	0 _ _ 0 0 0 0 0B
0622H	AMD32	Area mode register 32	R/W	0 0 0 0 0 0 0 0B
0623H	AMD4	Area mode register 4	R/W	0 _ _ 0 0 0 0 0B
0624H	AMD5	Area mode register 5	R/W	0 _ _ 0 0 0 0 0B
0625H	DSCR	DRAM signal control register	W	0 0 0 0 0 0 0 0B
0626H	RFCR	Refresh control register	R/W	_ _ XXXXXXB
0627H				0 0 _ _ _ 0 0 0B

(Continued)

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(Continued)

Address	Abbreviation	Register name	Read/write	Initial value
0628$_H$	EPCR0	External pin control register 0	W	_ _ _ _ 1 1 0 0$_B$
0629$_H$				_ 1 1 1 1 1 1 1$_B$
062A$_H$	(Reserved)			
062B$_H$	EPCR1	External pin control register 1	W	1 1 1 1 1 1 1 1$_B$
062C$_H$	DMCR4	DRAM control register 4	R/W	0 0 0 0 0 0 0 0$_B$
062D$_H$				0 0 0 0 0 0 0 _$_B$
062E$_H$	DMCR5	DRAM control register 5	R/W	0 0 0 0 0 0 0 0$_B$
062F$_H$				0 0 0 0 0 0 0 _$_B$
0630$_H$ to 07FD$_H$	(Reserved)			
07FE$_H$	LER	Little endian register	W	_ _ _ _ _ 0 0 0$_B$
07FF$_H$	MODR	Mode register	W	XXXXXXXX$_B$

Note : Do not use (reserved).

■ **INTERRUPT CAUSES, INTERRUPT VECTORS
AND INTERRUPT CONTROL REGISTER ALLOCATIONS**

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Reset	0	00	—	3FC$_H$	000FFFFC$_H$
Reserved for system	1	01	—	3F8$_H$	000FFFF8$_H$
Reserved for system	2	02	—	3F4$_H$	000FFFF4$_H$
Reserved for system	3	03	—	3F0$_H$	000FFFF0$_H$
Reserved for system	4	04	—	3EC$_H$	000FFFEC$_H$
Reserved for system	5	05	—	3E8$_H$	000FFFE8$_H$
Reserved for system	6	06	—	3E4$_H$	000FFFE4$_H$
Reserved for system	7	07	—	3E0$_H$	000FFFE0$_H$
Reserved for system	8	08	—	3DC$_H$	000FFFDC$_H$
Reserved for system	9	09	—	3D8$_H$	000FFFD8$_H$
Reserved for system	10	0A	—	3D4$_H$	000FFFD4$_H$
Reserved for system	11	0B	—	3D0$_H$	000FFFD0$_H$
Reserved for system	12	0C	—	3CC$_H$	000FFFCC$_H$
Reserved for system	13	0D	—	3C8$_H$	000FFFC8$_H$
Exception for undefined instruction	14	0E	—	3C4$_H$	000FFFC4$_H$
NMI request	15	0F	F$_H$ fixed	3C0$_H$	000FFFC0$_H$
External interrupt 0	16	10	ICR00	3BC$_H$	000FFFBC$_H$
External interrupt 1	17	11	ICR01	3B8$_H$	000FFFB8$_H$
External interrupt 2	18	12	ICR02	3B4$_H$	000FFFB4$_H$
External interrupt 3	19	13	ICR03	3B0$_H$	000FFFB0$_H$
UART0 receive complete	20	14	ICR04	3AC$_H$	000FFFAC$_H$
UART1 receive complete	21	15	ICR05	3A8$_H$	000FFFA8$_H$
UART2 receive complete	22	16	ICR06	3A4$_H$	000FFFA4$_H$
UART0 transmit complete	23	17	ICR07	3A0$_H$	000FFFA0$_H$
UART1 transmit complete	24	18	ICR08	39C$_H$	000FFF9C$_H$
UART2 transmit complete	25	19	ICR09	398$_H$	000FFF98$_H$
DMAC0 (complete, error)	26	1A	ICR10	394$_H$	000FFF94$_H$
DMAC1 (complete, error)	27	1B	ICR11	390$_H$	000FFF90$_H$
DMAC2 (complete, error)	28	1C	ICR12	38C$_H$	000FFF8C$_H$
DMAC3 (complete, error)	29	1D	ICR13	388$_H$	000FFF88$_H$
DMAC4 (complete, error)	30	1E	ICR14	384$_H$	000FFF84$_H$
DMAC5 (complete, error)	31	1F	ICR15	380$_H$	000FFF80$_H$

(Continued)

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
DMAC6 (complete, error)	32	20	ICR16	37C$_H$	000FFF7C$_H$
DMAC7 (complete, error)	33	21	ICR17	378$_H$	000FFF78$_H$
A/D converter (successive approximation conversion type)	34	22	ICR18	374$_H$	000FFF74$_H$
16-bit reload timer 0	35	23	ICR19	370$_H$	000FFF70$_H$
16-bit reload timer 1	36	24	ICR20	36C$_H$	000FFF6C$_H$
16-bit reload timer 2	37	25	ICR21	368$_H$	000FFF68$_H$
PWM 0	38	26	ICR22	364$_H$	000FFF64$_H$
PWM 1	39	27	ICR23	360$_H$	000FFF60$_H$
PWM 2	40	28	ICR24	35C$_H$	000FFF5C$_H$
PWM 3	41	29	ICR25	358$_H$	000FFF58$_H$
U-TIMER 0	42	2A	ICR26	354$_H$	000FFF54$_H$
U-TIMER 1	43	2B	ICR27	350$_H$	000FFF50$_H$
U-TIMER 2	44	2C	ICR28	34C$_H$	000FFF4C$_H$
Reserved for system	45	2D	ICR29	348$_H$	000FFF48$_H$
Reserved for system	46	2E	ICR30	344$_H$	000FFF44$_H$
Reserved for system	47	2F	ICR31	340$_H$	000FFF40$_H$
Reserved for system	48	30	ICR32	33C$_H$	000FFF3C$_H$
Reserved for system	49	31	ICR33	338$_H$	000FFF38$_H$
Reserved for system	50	32	ICR34	334$_H$	000FFF34$_H$
Reserved for system	51	33	ICR35	330$_H$	000FFF30$_H$
Reserved for system	52	34	ICR36	32C$_H$	000FFF2C$_H$
Reserved for system	53	35	ICR37	328$_H$	000FFF28$_H$
Reserved for system	54	36	ICR38	324$_H$	000FFF24$_H$
Reserved for system	55	37	ICR39	320$_H$	000FFF20$_H$
Reserved for system	56	38	ICR40	31C$_H$	000FFF1C$_H$
Reserved for system	57	39	ICR41	318$_H$	000FFF18$_H$
Reserved for system	58	3A	ICR42	314$_H$	000FFF14$_H$
Reserved for system	59	3B	ICR43	310$_H$	000FFF10$_H$
Reserved for system	60	3C	ICR44	30C$_H$	000FFF0C$_H$
Reserved for system	61	3D	ICR45	308$_H$	000FFF08$_H$
Reserved for system	62	3E	ICR46	304$_H$	000FFF04$_H$
Delayed interrupt cause bit	63	3F	ICR47	300$_H$	000FFF00$_H$

(Continued)

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(Continued)

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Reserved for system (used in REA-LOS*)	64	40	—	2FC$_H$	000FFEFC$_H$
Reserved for system (used in REA-LOS*)	65	41	—	2F8$_H$	000FFEF8$_H$
Used in INT instructions	66 to 255	42 to FF	—	2F4$_H$ to 000$_H$	000FFEF4$_H$ to 000FFC00$_H$

*: REALOS/FR uses interrupt number 0x40 and 0x41 for system code.

MB91101/MB91101A

■ PERIPHERAL RESOURCES

1.   I/O Ports

There are 2 types of I/O port register structure; port data register (PDR0 to PDRF) and data direction register (DDR0 to DDRF), where bits PDR0 to PDRF and bits DDR0 to DDRF corresponds respectively. Each bit on the register corresponds to an external pin. In port registers input/output register of the port configures input/ output function of the port, while corresponding bit (pin) configures input/output function in data direction registers. Bit "0" specifies input and "1" specifies output.
  • For input (DDR = "0") setting;
    PDR reading operation: reads level of corresponding external pin.
    PDR writing operation: writes set value to PDR.
  • For output (DDR = "1") setting;
    PDR reading operation: reads PDR value.
    PDR writing operation: outputs PDR value to corresponding external pin.
  • **Block diagram**
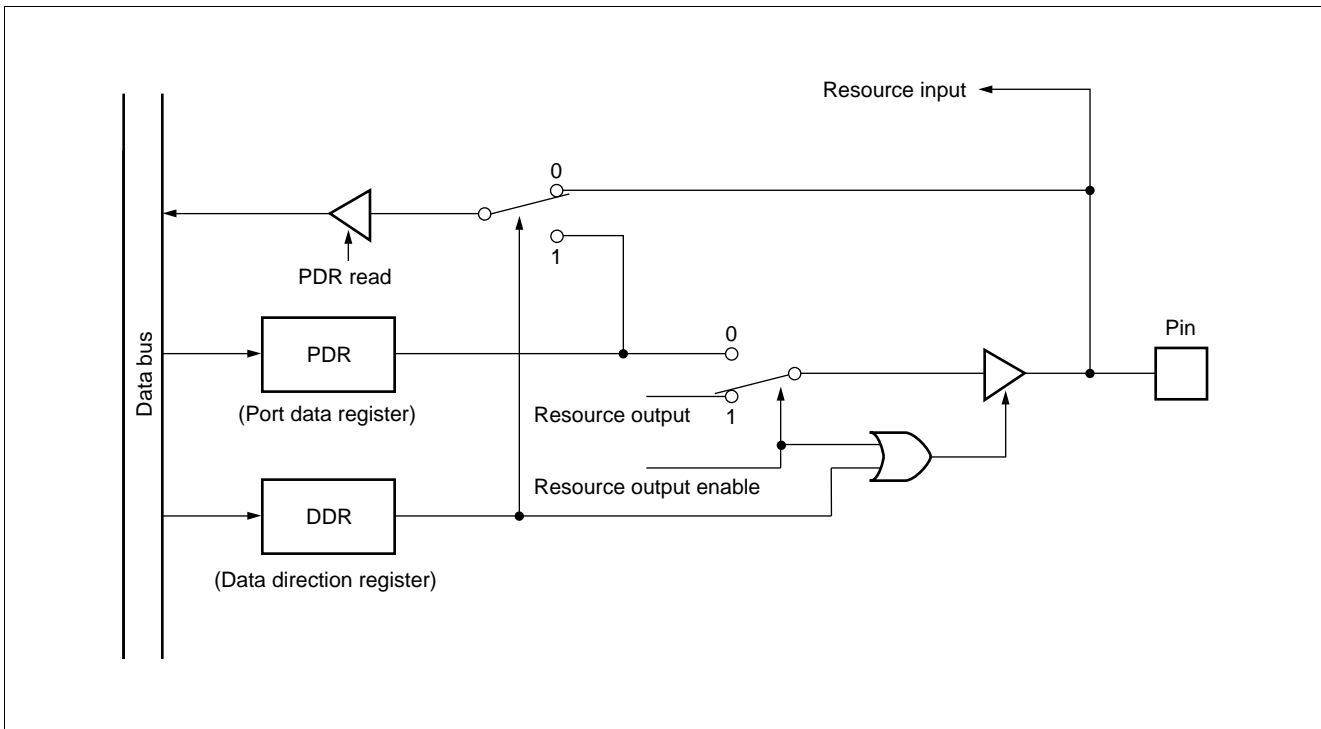
• **Port data register**

Address	bit 7 — bit 0	Initial value	
000001$_H$	PDR2	XXXXXXXX$_B$	(R/W)
000005$_H$	PDR6	XXXXXXXX$_B$	(R/W)
00000B$_H$	PDR8	- - X - - XXX$_B$	(R/W)
000009$_H$	PDRA	- XXXXXX -$_B$	(R/W)
000008$_H$	PDRB	XXXXXXXX$_B$	(R/W)
000012$_H$	PDRE	XXXXXXXX$_B$	(R/W)
000013$_H$	PDRF	XXXXXXXX$_B$	(R/W)

( ) :Access
R/W :Readable and writable
X :Indeterminate

• **Data direction register**

Address	bit 7 — bit 0	Initial value	
000601$_H$	DDR2	00000000$_B$	(W)
000605$_H$	DDR6	00000000$_B$	(W)
00060B$_H$	DDR8	- - 0 - - 0 0 0$_B$	(W)
000609$_H$	DDRA	- 000000 -$_B$	(W)
000608$_H$	DDRB	00000000$_B$	(W)
0000D2$_H$	DDRE	00000000$_B$	(W)
0000D3$_H$	DDRF	00000000$_B$	(W)

( ) :Access
W :Write only
– :Unused

2. DMA Controller (DMAC)

The DMA controller is a module embedded in FR family devices, and performs DMA (direct memory access) transfer.

DMA transfer performed by the DMA controller transfers data without intervention of CPU, contributing to enhanced performance of the system.
- 8 channels
- Mode: single/block transfer, burst transfer and continuous transfer: 3 kinds of transfer
- Transfer all through the area
- Max 65536 of transfer cycles
- Interrupt function right after the transfer
- Selectable for address transfer increase/decrease by the software
- External transfer request input pin, external transfer request accept output pin, external transfer complete output pin three pins for each

- **Block diagram**
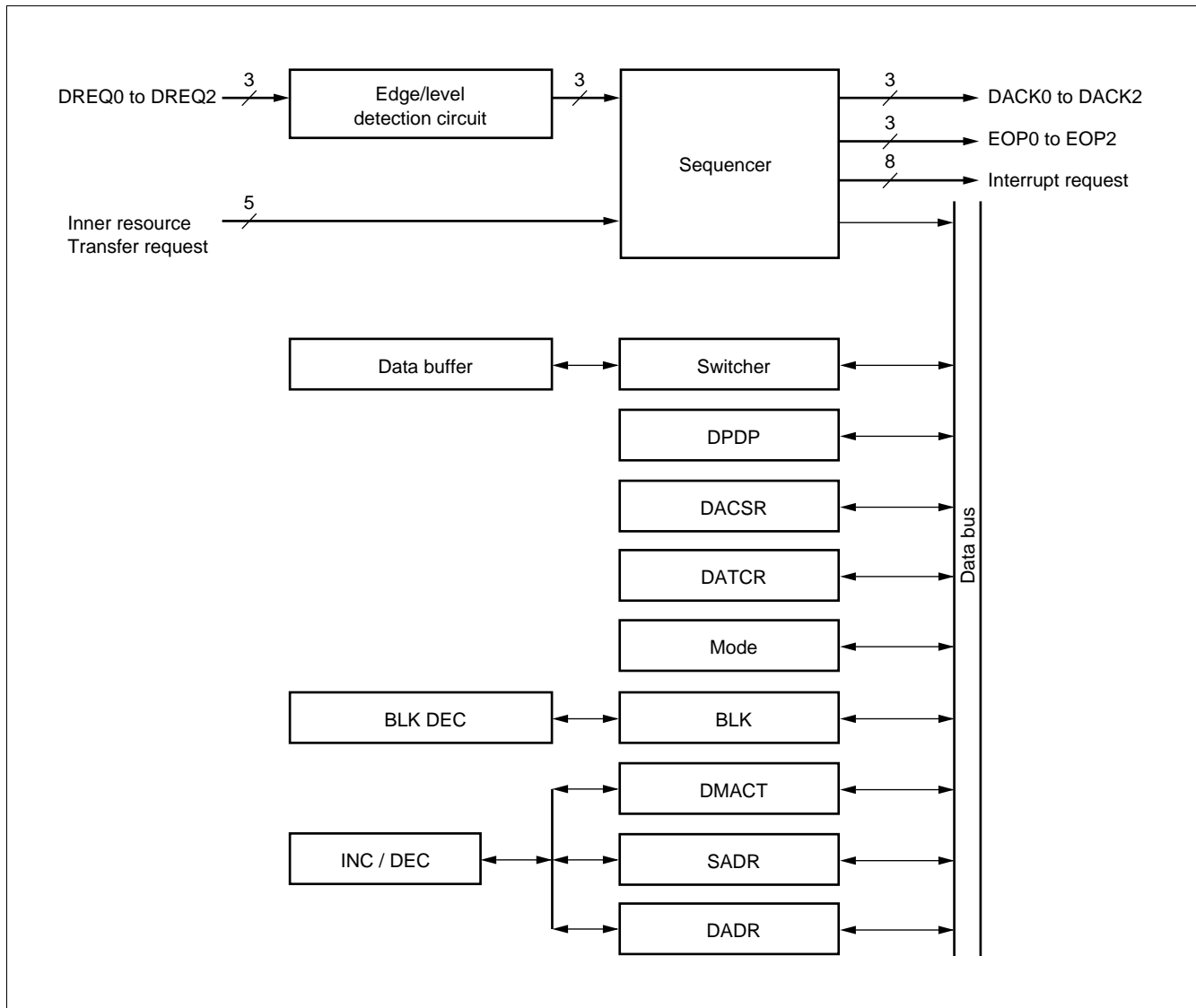
- **Registers (DMAC internal registers)**

Address	bit 31	bit 16	bit 0	Initial value	
00000200$_H$ 00000201$_H$ 00000202$_H$ 00000203$_H$		DPDP		XXXXXXXX$_B$ XXXXXXXX$_B$ XXXXXXXX$_B$ X0000000$_B$	(R/W)
00000204$_H$ 00000205$_H$ 00000206$_H$ 00000207$_H$		DACSR		00000000$_B$ 00000000$_B$ 00000000$_B$ 00000000$_B$	(R/W)
00000208$_H$ 00000209$_H$ 0000020A$_H$ 0000020B$_H$		DATCR		XXXXXXXX$_B$ XXXX0000$_B$ XXXX0000$_B$ XXXX0000$_B$	(R/W)

( ) :Access
R/W:Readable and writable
X :Indeterminate

- **Registers (DMA descriptor)**

Address	bit 31	bit 0	
DPDP + 0$_H$			DMA ch.0 Descriptor
DPDP + 0C$_H$			DMA ch.1 Descriptor
DPDP + 54$_H$			DMA ch.7 Descriptor

3. UART

The UART is a serial I/O port for supporting asynchronous (start-stop system) communication or CLK synchro-nous communication, and it has the following features.

The MB91101 and MB91101A consist of 3 channels of UART.
• Full double double buffer
• Both a synchronous (start-stop system) communication and CLK synchronous communication are available.
• Supporting multi-processor mode
• Perfect programmable baud rate
  Any baud rate can be set by internal timer (refer to section "4. U-TIMER").
• Any baud rate can be set by external clock.
• Error checking function (parity, framing and overrun)
• Transfer signal: NRZ code
• Enable DMA transfer/start by interrupt.

● **Block diagram**
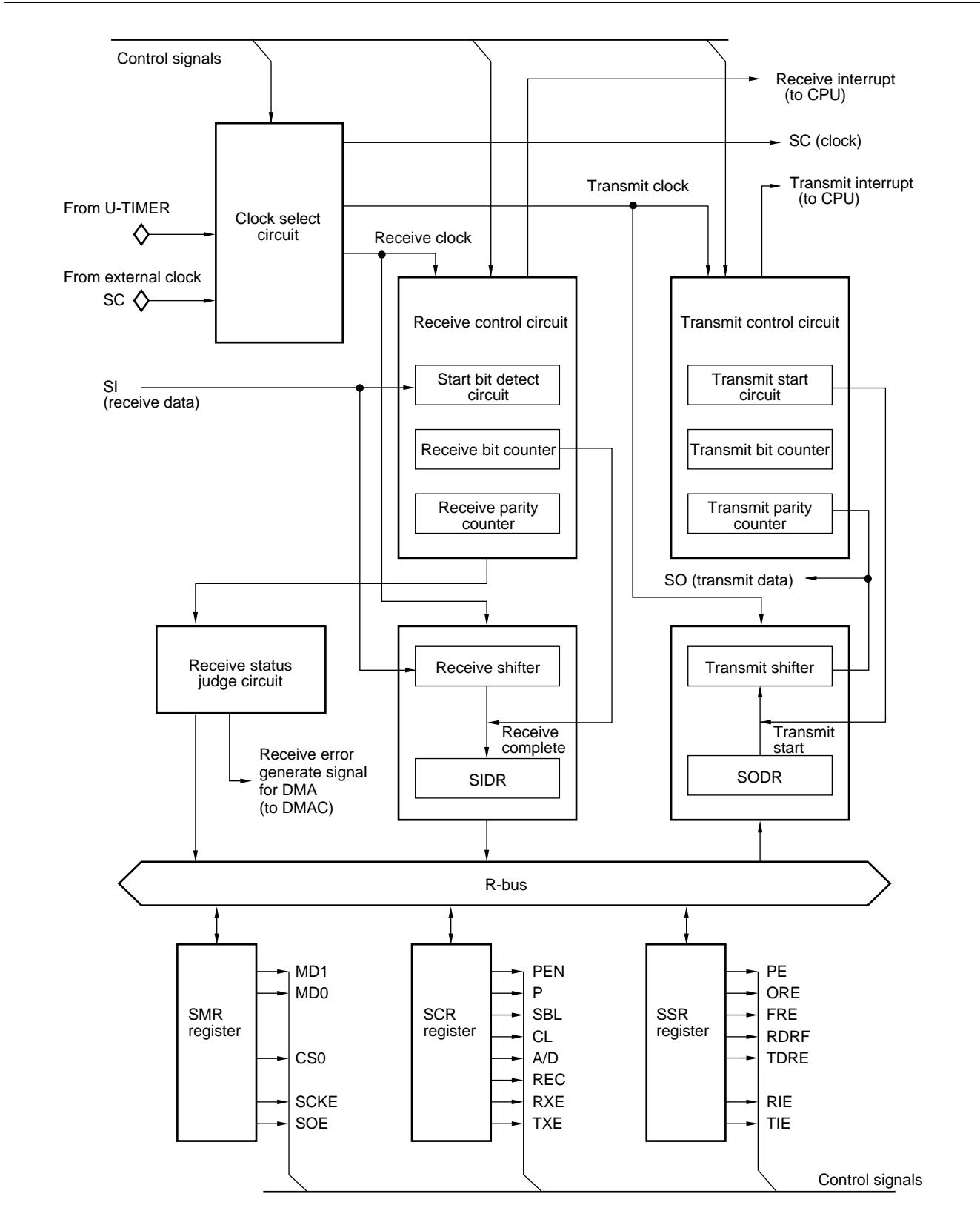
- **Register configuration**

Address	bit 15	bit 8	bit 0	Initial value	
$0000001E_H$	SCR0			00000100_B	(R/W)
00000022_H	SCR1			00000100_B	(R/W)
00000026_H	SCR2			00000100_B	(R/W)
$0000001F_H$		SMR0		$00 - - 0 - 00_B$	(R/W)
00000023_H		SMR1		$00 - - 0 - 00_B$	(R/W)
00000027_H		SMR2		$00 - - 0 - 00_B$	(R/W)
$0000001C_H$	SSR0			$00001 - 00_B$	(R/W)
00000020_H	SSR1			$00001 - 00_B$	(R/W)
00000024_H	SSR2			$00001 - 00_B$	(R/W)
$0000001D_H$		SIDR0/SODR0		$XXXXXXXX_B$	(R/W)
00000021_H		SIDR1/SIDR1		$XXXXXXXX_B$	(R/W)
00000002_H		SIDR2/SIDR2		$XXXXXXXX_B$	(R/W)

( )   :Access
R/W :Readable and writable
–   :Unused
X   :Indeterminate

4. U-TIMER (16-bit Timer for UART Baud Rate Generation)

The U-TIMER is a 16-bit timer for generating UART baud rate. Combination of chip operating frequency and reload value of U-TIMER allows flexible setting of baud rate.

The U-TIMER operates as an interval timer by using interrupt issued on counter underflow.

The MB91101 and MB91101A have 3 channel U-TIMER embedded on the chip. An interval of up to $2^{16} \times \phi$ can be counted.

• **Block diagram**

• **Register configuration**


```
( )    :Access
R/W  :Readable and writable
–      :Unused
```

5. PWM Timer

The PWM timer can output high accurate PWM waves efficiently.

The MB91101 and MB91101A have inner 4-channel PWM timers, and has the following features.
• Each channel consists of a 16-bit down counter, a 16-bit data resister with a buffer for scyde setting, a 16-bit compare resister with a buffer for duty setting, and a pin controller.
• The count clock of a 16-bit down counter can be selected from the following four inner clocks.
  Inner clock ϕ, $\phi/4$, $\phi/16$, $\phi/64$
• The counter value can be initialized "FFFF$_H$" by the resetting or the counter borrow.
• PWM output (each channel)
• Resister description

• **Block diagram (general construction)**
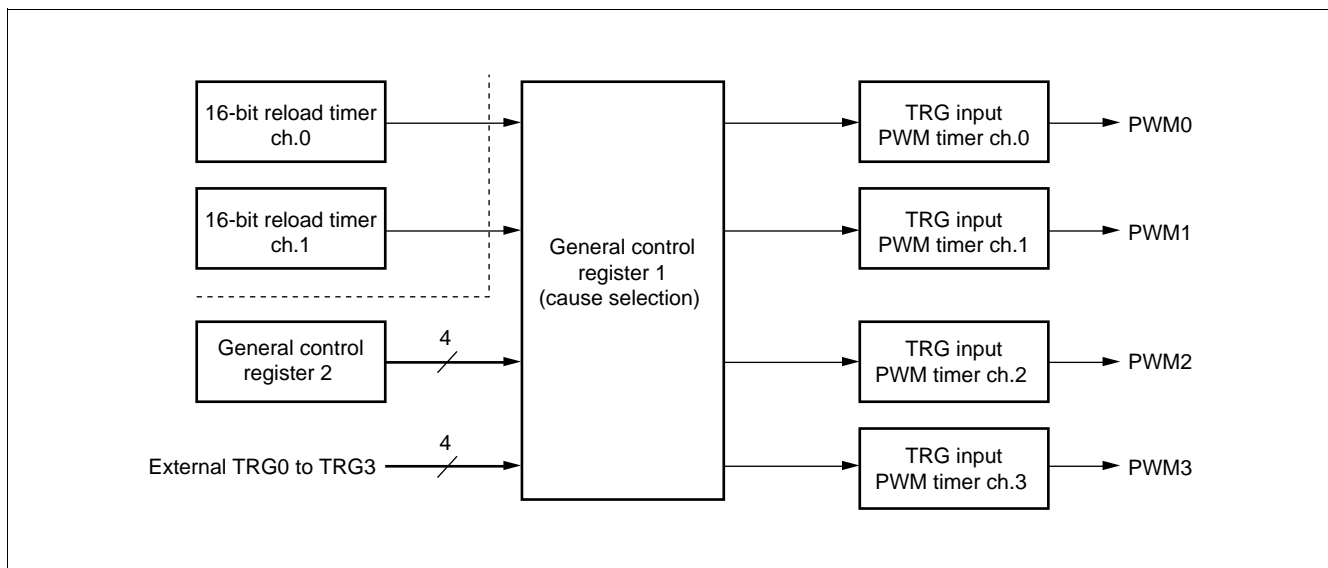
• **Block diagram (for one channel)**
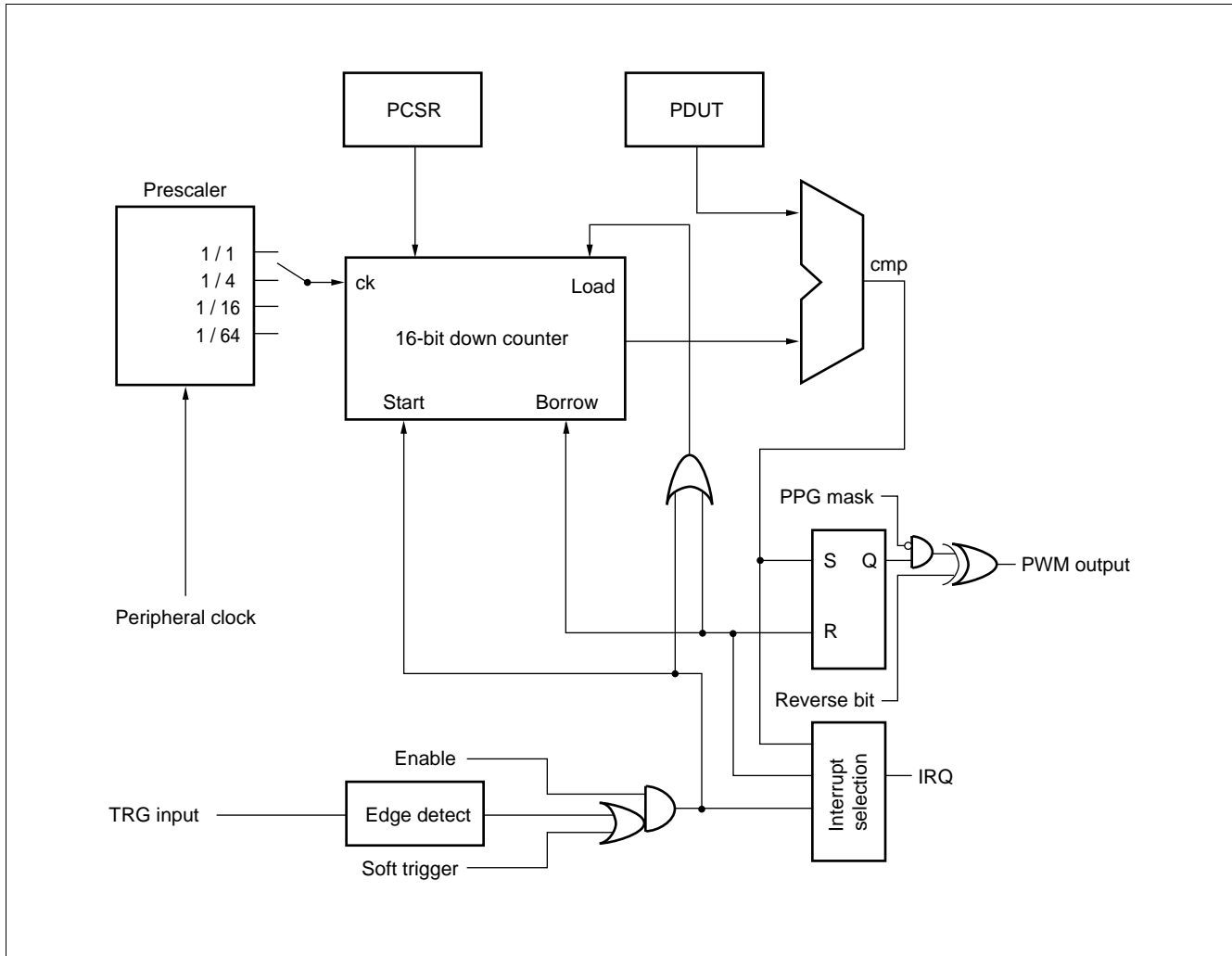
• **Register configuration**

Address	bit 15	bit 8	bit 0	Initial value	
000000DC$_H$ 000000DD$_H$	GCN1			00110010$_B$ 00010000$_B$	(R/W)
000000DF$_H$		GCN2		00000000$_B$	(R/W)
000000E0$_H$ 000000E1$_H$	PTMR0			11111111$_B$ 11111111$_B$	(R)
000000E2$_H$ 000000E3$_H$	PCSR0			XXXXXXXX$_B$ XXXXXXXX$_B$	(W)
000000E4$_H$ 000000E5$_H$	PDUT0			XXXXXXXX$_B$ XXXXXXXX$_B$	(W)
000000E6$_H$	PCNH0			0000000-$_B$	(R/W)
000000E7$_H$		PCNL0		00000000$_B$	(R/W)
000000E8$_H$ 000000E9$_H$	PTMR1			11111111$_B$ 11111111$_B$	(R)
000000EA$_H$ 000000EB$_H$	PCSR1			XXXXXXXX$_B$ XXXXXXXX$_B$	(W)
000000EC$_H$ 000000ED$_H$	PDUT1			XXXXXXXX$_B$ XXXXXXXX$_B$	(W)
000000EE$_H$	PCNH1			0000000-$_B$	(R/W)
000000EF$_H$		PCNL1		00000000$_B$	(R/W)
000000F0$_H$ 000000F1$_H$	PTMR2			11111111$_B$ 11111111$_B$	(R)
000000F2$_H$ 000000F3$_H$	PCSR2			XXXXXXXX$_B$ XXXXXXXX$_B$	(W)
000000F4$_H$ 000000F5$_H$	PDUT2			XXXXXXXX$_B$ XXXXXXXX$_B$	(W)
000000F6$_H$	PCNH2			0000000-$_B$	(R/W)
000000F7$_H$		PCNL2		00000000$_B$	(R/W)
000000F8$_H$ 000000F9$_H$	PTMR3			11111111$_B$ 11111111$_B$	(R)
000000FA$_H$ 000000FB$_H$	PCSR3			XXXXXXXX$_B$ XXXXXXXX$_B$	(W)
000000FC$_H$ 000000FD$_H$	PDUT3			XXXXXXXX$_B$ XXXXXXXX$_B$	(W)
000000FE$_H$	PCNH3			0000000-$_B$	(R/W)
000000FF$_H$		PCNL3		00000000$_B$	(R/W)

( )   :Access
R/W   :Readable and writable
R   :Read only
W   :Write only
–   :Unused
X   :Indeterminate

6. 16-bit Reload Timer

The 16-bit reload timer consists of a 16-bit down counter, a 16-bit reload timer, a prescaler for generating internal count clock and control registers.

Internal clock can be selected from 3 types of internal clocks (divided by 2/8/32 of machine clock).

The DMA transfer can be started by the interruption.

The MB91101 and MB91101A consist of 3 channels of the 16-bit reload timer.

• Block diagram
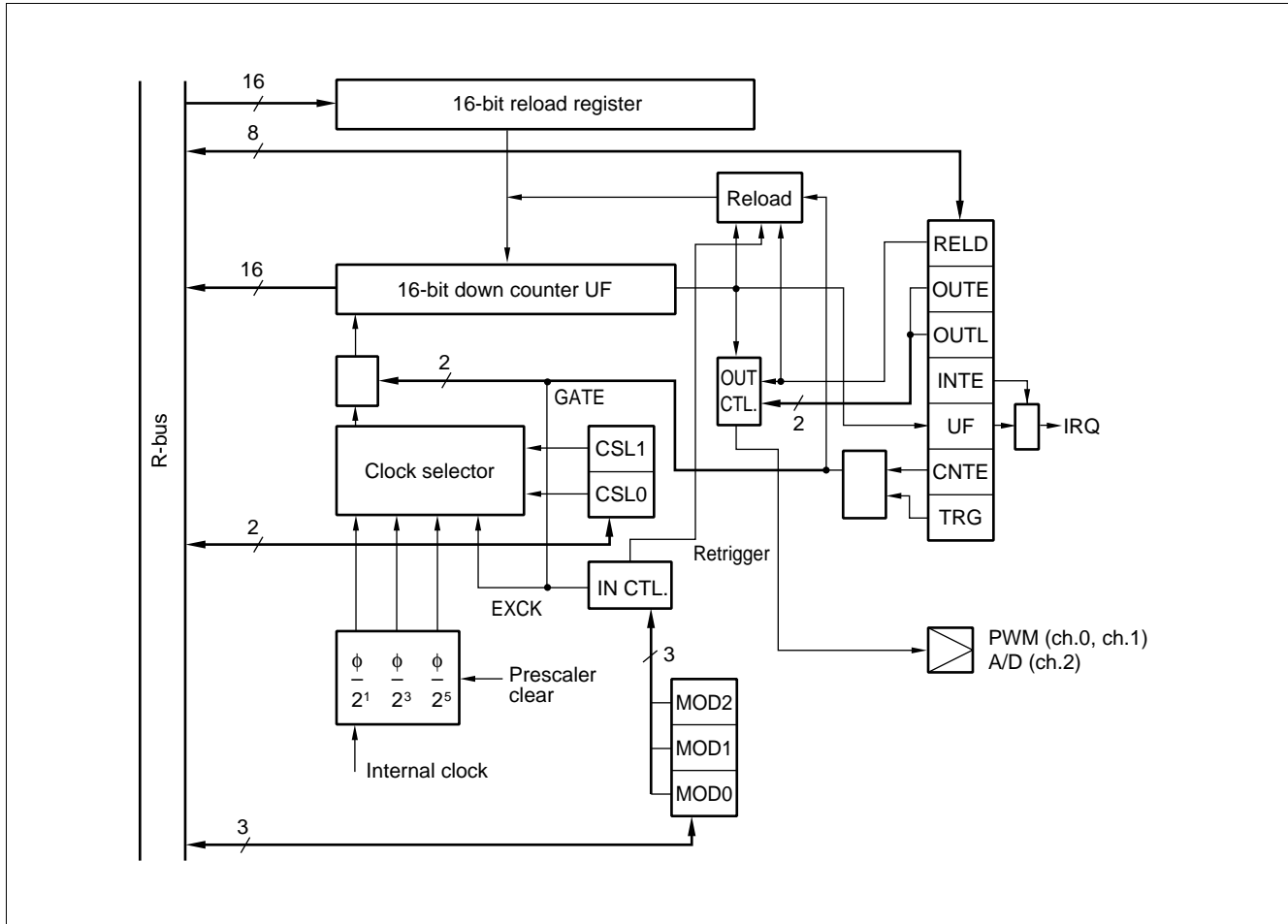
- **Register configuration**

Address	bit 15	bit 0	Initial value	
0000002E$_H$ 0000002F$_H$	TMCSR0		- - - - 0 0 0 0$_B$ 0 0 0 0 0 0 0 0$_B$	(R/W)
00000036$_H$ 00000037$_H$	TMCSR1		- - - - 0 0 0 0$_B$ 0 0 0 0 0 0 0 0$_B$	(R/W)
00000042$_H$ 00000043$_H$	TMCSR2		- - - - 0 0 0 0$_B$ 0 0 0 0 0 0 0 0$_B$	(R/W)
0000002A$_H$ 0000002B$_H$	TMR0		XXXXXXXX$_B$ XXXXXXXX$_B$	(R)
00000032$_H$ 00000033$_H$	TMR1		XXXXXXXX$_B$ XXXXXXXX$_B$	(R)
0000003E$_H$ 0000003F$_H$	TMR2		XXXXXXXX$_B$ XXXXXXXX$_B$	(R)
00000028$_H$ 00000029$_H$	TMRLR0		XXXXXXXX$_B$ XXXXXXXX$_B$	(W)
00000030$_H$ 00000031$_H$	TMRLR1		XXXXXXXX$_B$ XXXXXXXX$_B$	(W)
0000003C$_H$ 0000003D$_H$	TMRLR2		XXXXXXXX$_B$ XXXXXXXX$_B$	(W)

( )　:Access
R/W　:Readable and writable
R　　:Read only
W　　:Write only
–　　:Unused
X　　:Indeterminate

7. Bit Search Module

The bit search module detects transitions of data (0 to 1/1 to 0) on the data written on the input registers and returns locations of the transitions.

• **Block diagram**

• **Register configuration**
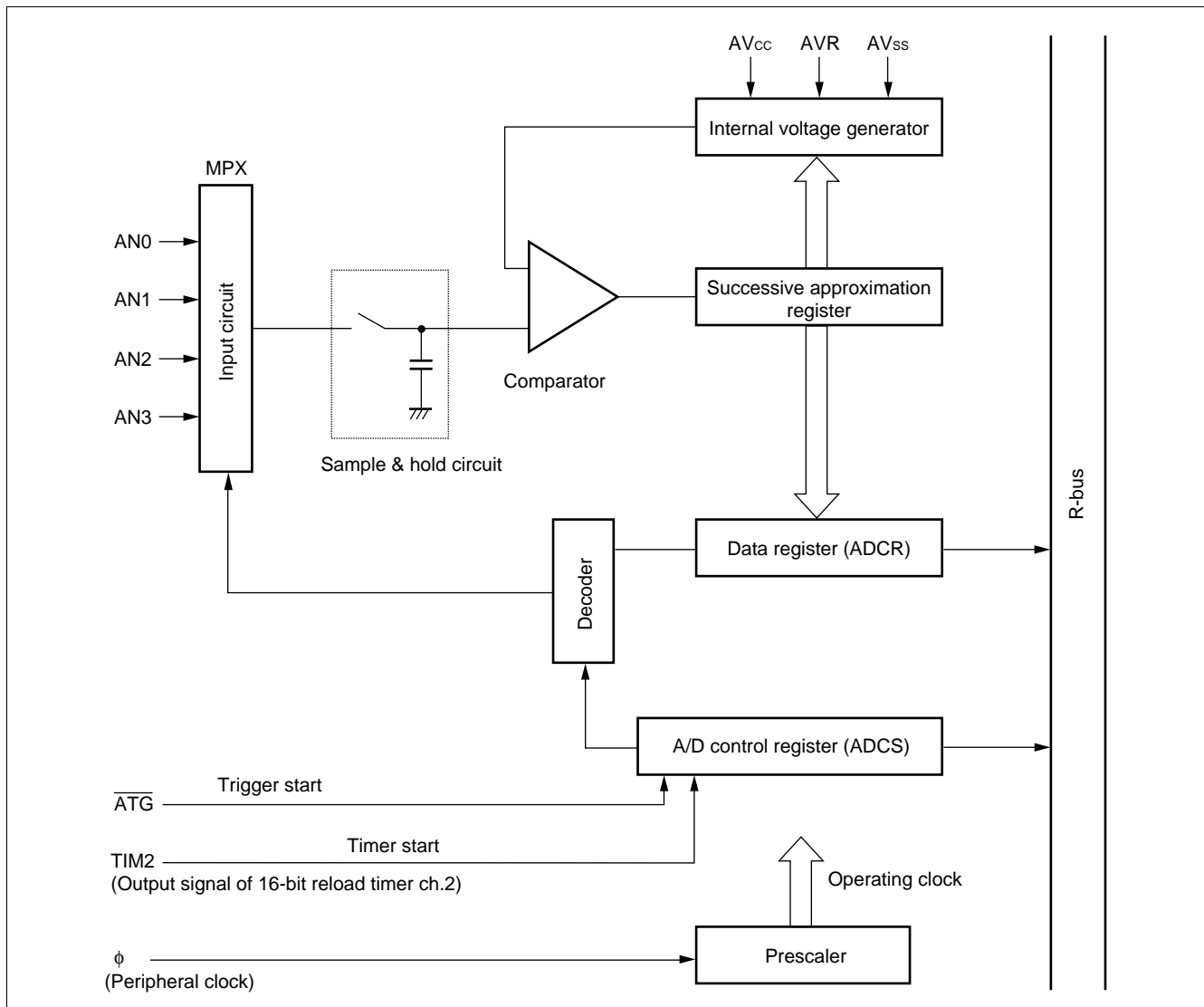

( )   :Access
R/W   :Readable and writable
R   :Read only
W   :Write only
X   :Indeterminate

8. 10-bit A/D Converter (Successive Approximation Conversion Type)

The A/D converter is the module which converts an analog input voltage to a digital value, and it has following features.

- Minimum converting time: 5.6 μs/ch. (system clock: 25 MHz)
- Inner sample and hold circuit
- Resolution: 10 bits
- Analog input can be selected from 4 channels by program.
  Single convert mode: 1 channel is selected and converted.
  Scan convert mode: Converting continuous channels. Maximum 4 channels are programmable.
  Continuous convert mode: Converting the specified channel repeatedly.
  Stop convert mode: After converting one channel then stop and wait till next activation synchronizing at the beginning of conversion can be performed.
- DMA transfer operation is available by interruption.
- Operating factor can be selected from the software, the external trigger (falling edge), and 16-bit reload timer (rising edge).
- **Block diagram**

• **Register configuration**

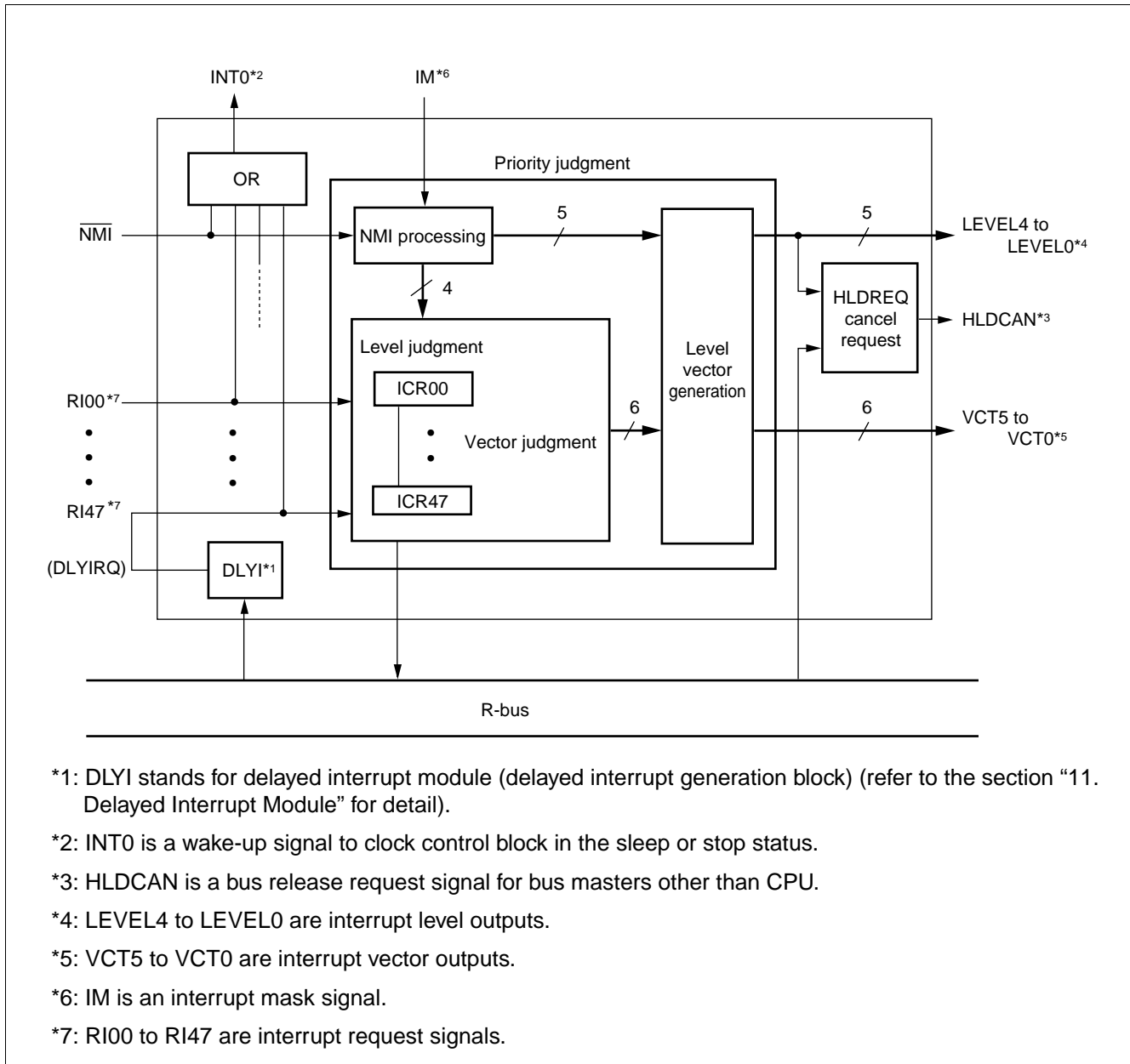| Address	bit 15	bit 0	Initial value	
0000003A$_H$ 0000003B$_H$	ADCS		0000000$_B$ 0000000$_B$	(R/W)
00000038$_H$ 00000039$_H$	ADCR		- - - - - - XX$_B$ XXXXXXXX$_B$	(R)

( ) :Access
R/W :Readable and writable
R :Read only
– :Unused
X :Indeterminate

9. Interrupt Controller

The interrupt controller processes interrupt acknowledgments and arbitration between interrupts.

• **Block diagram**

*1: DLYI stands for delayed interrupt module (delayed interrupt generation block) (refer to the section "11. Delayed Interrupt Module" for detail).

*2: INT0 is a wake-up signal to clock control block in the sleep or stop status.

*3: HLDCAN is a bus release request signal for bus masters other than CPU.

*4: LEVEL4 to LEVEL0 are interrupt level outputs.

*5: VCT5 to VCT0 are interrupt vector outputs.

*6: IM is an interrupt mask signal.

*7: RI00 to RI47 are interrupt request signals.

• **Register configuration**

Address	bit 7 ⟶ bit 0	Initial value	Address	bit 7 ⟶ bit 0	Initial value
00000400H	ICR00	- - - 11111 B (R/W)	00000411H	ICR17	- - - 11111 B (R/W)
00000401H	ICR01	- - - 11111 B (R/W)	00000412H	ICR18	- - - 11111 B (R/W)
00000402H	ICR02	- - - 11111 B (R/W)	00000413H	ICR19	- - - 11111 B (R/W)
00000403H	ICR03	- - - 11111 B (R/W)	00000414H	ICR20	- - - 11111 B (R/W)
00000404H	ICR04	- - - 11111 B (R/W)	00000415H	ICR21	- - - 11111 B (R/W)
00000405H	ICR05	- - - 11111 B (R/W)	00000416H	ICR22	- - - 11111 B (R/W)
00000406H	ICR06	- - - 11111 B (R/W)	00000417H	ICR23	- - - 11111 B (R/W)
00000407H	ICR07	- - - 11111 B (R/W)	00000418H	ICR24	- - - 11111 B (R/W)
00000408H	ICR08	- - - 11111 B (R/W)	00000419H	ICR25	- - - 11111 B (R/W)
00000409H	ICR09	- - - 11111 B (R/W)	0000041AH	ICR26	- - - 11111 B (R/W)
0000040AH	ICR10	- - - 11111 B (R/W)	0000041BH	ICR27	- - - 11111 B (R/W)
0000040BH	ICR11	- - - 11111 B (R/W)	0000041CH	ICR28	- - - 11111 B (R/W)
0000040CH	ICR12	- - - 11111 B (R/W)	0000041DH	ICR29	- - - 11111 B (R/W)
0000040DH	ICR13	- - - 11111 B (R/W)	0000041EH	ICR30	- - - 11111 B (R/W)
0000040EH	ICR14	- - - 11111 B (R/W)	0000041FH	ICR31	- - - 11111 B (R/W)
0000040FH	ICR15	- - - 11111 B (R/W)	0000042FH	ICR47	- - - 11111 B (R/W)
00000410H	ICR16	- - - 11111 B (R/W)	00000431H	HRCL	- - - 11111 B (R/W)
			00000430H	DICR	- - - - - - - 0 B (R/W)

( ) :Access
R/W :Readable and writable
– :Unused
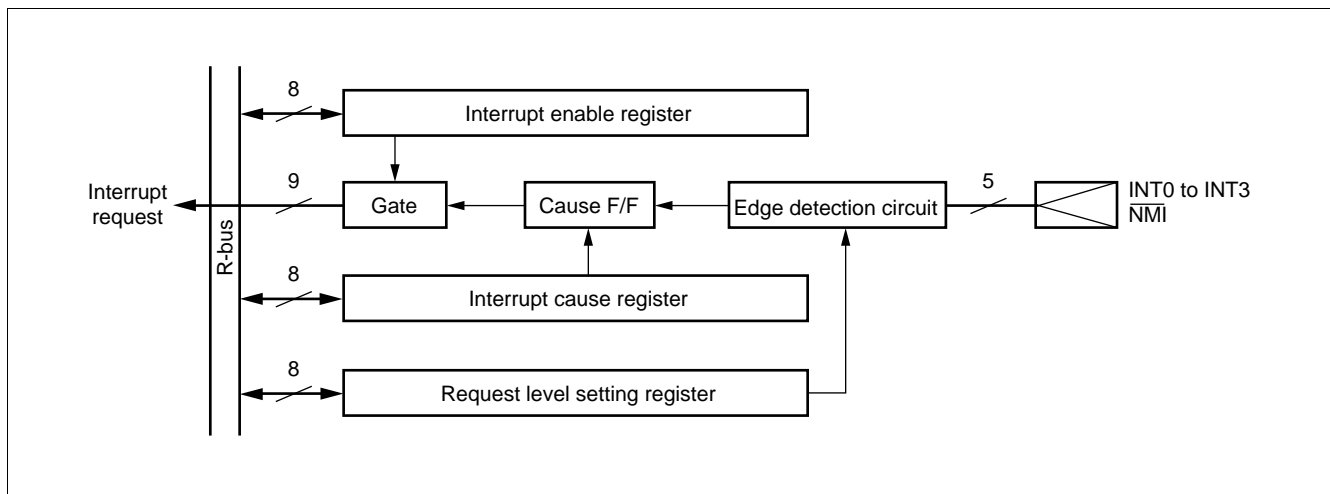
10. External Interrupt/NMI Control Block

The external interrupt/NMI control block controls external interrupt request signals input to $\overline{\text{NMI}}$ pin and INT0 to INT3 pins.

Detecting levels can be selected from "H", "L", rising edge and falling edge (not for $\overline{\text{NMI}}$ pin).

• **Block diagram**

• **Register configuration**


```
Address        bit 15              bit 8              bit 0    Initial value
00000095H                            |      ENIR            |   00000000 B  (R/W)
00000094H      |      EIRR            |                          00000000 B  (R/W)
00000099H                            |      ELVR            |   00000000 B  (R/W)

        ( )    :Access
        R/W  :Readable and writable
```

11. Delayed Interrupt Module

Delayed interrupt module is a module which generates a interrupt for changing a task. By using this delayed interrupt module, an interrupt request to CPU can be generated/cancelled by the software.

Refer to the section "9. Interrupt Controller" for delayed interrupt module block diagram.

• **Register configuration**

Address	bit 7	bit 0	Initial value
00000430$_H$	DICR	- - - - - - - 0$_B$ (R/W)

( )　:Access
R/W :Readable and writable
–　　:Unused

12. Clock Generation (Low-power consumption mechanism)

The clock control block is a module which undertakes the following functions.

- CPU clock generation (including gear function)
- Peripheral clock generation (including gear function)
- Reset generation and cause hold
- Standby function (including hardware standby)
- DMA request prohibit
- PLL (multiplier circuit) embedded

- **Block diagram**
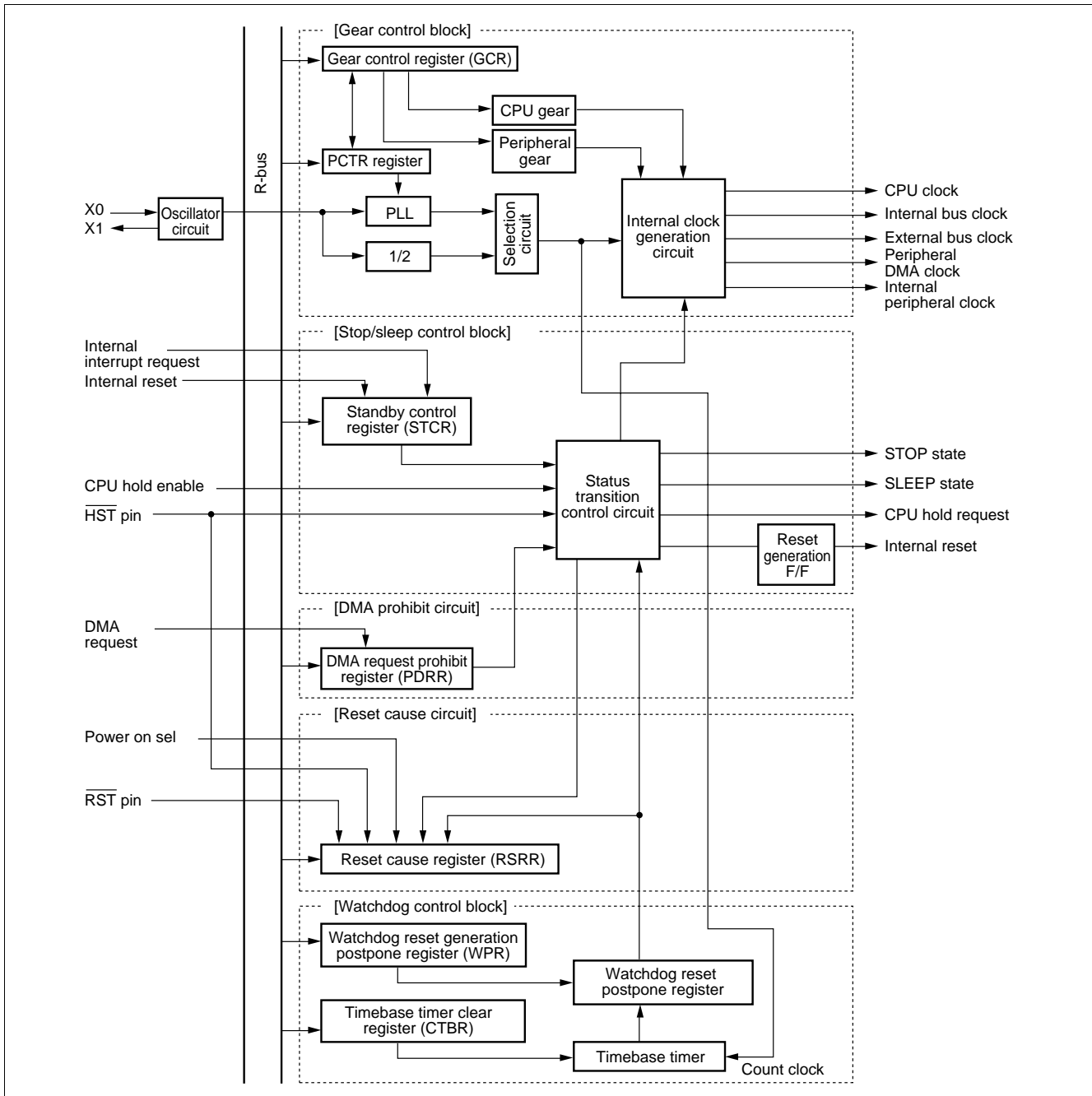
• **Register configuration**

Address	bit 15	bit 8	bit 0	Initial value	
00000480$_H$	RSRR/WTCR			1XXXX - 0 0$_B$	(R/W)
00000481$_H$		STCR		0 0 0 1 1 1 - -$_B$	(R/W)
00000482$_H$	PDRR			- - - - 0 0 0 0$_B$	(R/W)
00000483$_H$		CTBR		XXXXXXXX$_B$	(W)
00000484$_H$	GCR			1 1 0 0 1 1 - 1$_B$	(R/W)
00000485$_H$		WPR		XXXXXXXX$_B$	(W)
00000488$_H$	PCTR			0 0 - - 0 - - -$_B$	(R/W)

( )   :Access
R/W :Readable and writable
W   :Write only
–   :Unused
X   :Indeterminate

13. External Bus Interface

The external bus interface controls the interface between the device and the external memory and also the external I/O, and has the following features.

- 25-bit (32 Mbytes) address output
- 6 independent banks owing to the chip select function.
  Can be set to anywhere on the logical address space for minimum unit 64 Kbytes.
  Total 32 Mbytes × 6 area setting is available by the address pin and the chip select pin.
- 8/16-bit bus width setting are available for every chip select area.
- Programmable automatic memory wait (Max for 7 cycles) can be inserted.
- DRAM interface support
  Three kinds of DRAM interface: Double CAS DRAM (normally DRAM I/F)
  Single CAS DRAM
  Hyper DRAM
  2 banks independent control (RAS, CAS, etc. control signals)
  DRAM select is available from 2CAS/1WE and 1CAS/2WE.
  Hi-speed page mode supported
  CBR/self refresh supported
  Programmable wave form
- Unused address/data pin can be used for I/O port.
- Little endian mode supported
- Clock doubler: Internal bus 50 MHz, external bus 25 MHz

• **Block diagram**
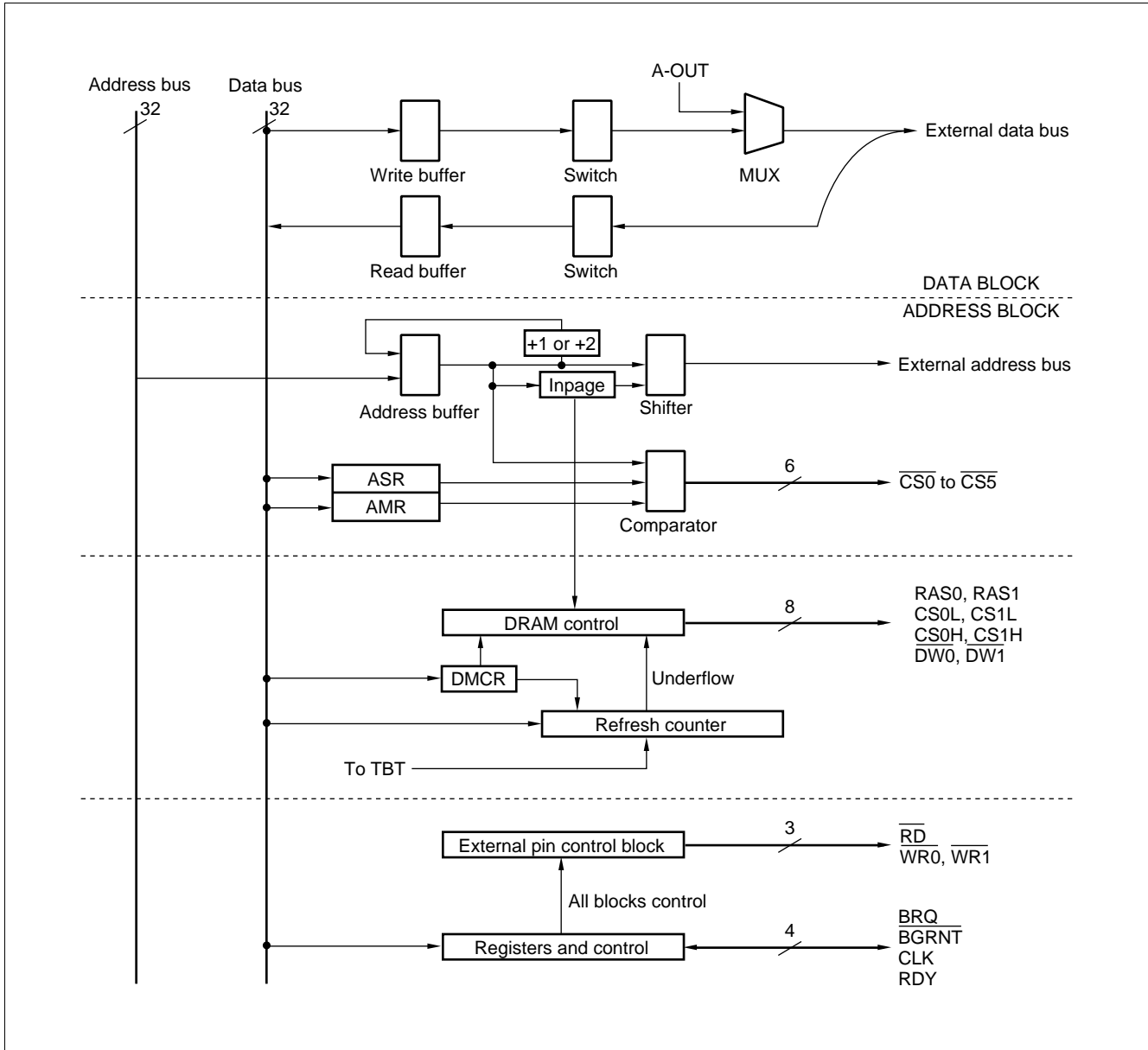
• **Register configuration**

Address	bit 31 → bit 16 → bit 0	Initial value	Access
$0000060C_H$ $0000060D_H$	ASR1	00000000_B 00000001_B	(W)
$0000060E_H$ $0000060F_H$	AMR1	00000000_B 00000000_B	(W)
00000610_H 00000611_H	ASR2	00000000_B 00000010_B	(W)
00000612_H 00000613_H	AMR2	00000000_B 00000000_B	(W)
00000614_H 00000615_H	ASR3	00000000_B 00000011_B	(W)
00000616_H 00000617_H	AMR3	00000000_B 00000000_B	(W)
00000618_H 00000619_H	ASR4	00000000_B 00000100_B	(W)
$0000061A_H$ $0000061B_H$	AMR4	00000000_B 00000000_B	(W)
$0000061C_H$ $0000061D_H$	ASR5	00000000_B 00000101_B	(W)
$0000061E_H$ $0000061F_H$	AMR5	00000000_B 00000000_B	(W)
00000620_H	AMD0	$---00111_B$	(R/W)
00000621_H	AMD1	$0--00000_B$	(R/W)
00000622_H	AMD32	00000000_B	(R/W)
00000623_H	AMD4	$0--00000_B$	(R/W)
00000624_H	AMD5	$0--00000_B$	(R/W)
00000625_H	DSCR	00000000_B	(W)
00000626_H 00000627_H	RFCR	$--XXXXXX_B$ $00---000_B$	(R/W)
00000628_H 00000629_H	EPCR0	$----1100_B$ -1111111_B	(W)
$0000062B_H$	EPCR1	11111111_B	(W)
$0000062C_H$ $0000062D_H$	DMCR4	00000000_B $0000000-_B$	(R/W)
$0000062E_H$ $0000062F_H$	DMCR5	00000000_B $0000000-_B$	(R/W)
$000007FE_H$	LER	$-----000_B$	(W)
$000007FF_H$	MODR	$XXXXXXXX_B$	(W)

( ) :Access
R/W :Readable and writable
W :Write only
– :Unused
X :Indeterminate

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

$(V_{SS} = AV_{SS} = 0.0$ V)

Parameter		Symbol	Rating		Unit	Remarks
			Min	Max		
Power supply voltage	At 5 V power supply	$V_{CC}5$	$V_{SS} - 0.3$	$V_{SS} + 6.5$	V	
		$V_{CC}3$	—	—	V	
	At 3 V power supply	$V_{CC}5$	$V_{CC}3 - 0.3$	$V_{SS} + 6.5$	V	*1
		$V_{CC}3$	$V_{SS} - 0.3$	$V_{SS} + 3.6$	V	*1
Analog supply voltage		AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 3.6$	V	*2
Analog reference voltage		AVRH	$V_{SS} - 0.3$	$V_{SS} + 3.6$	V	*2
Analog pin input voltage		V_{IA}	$V_{SS} - 0.3$	$AV_{CC} + 0.3$	V	
Input voltage		V_{I}	$V_{SS} - 0.3$	$V_{CC}5 + 0.3$	V	
Output voltage		V_{O}	$V_{SS} - 0.3$	$V_{CC}5 + 0.3$	V	
"L" level maximum output current		I_{OL}	—	10	mA	*3
"L" level average output current		I_{OLAV}	—	4	mA	*4
"L" level maximum total output current		ΣI_{OL}	—	100	mA	
"L" level average total output current		ΣI_{OLAV}	—	50	mA	*5
"H" level maximum output current		I_{OH}	—	-10	mA	*3
"H" level average output current		I_{OHAV}	—	-4	mA	*4
"H" level maximum total output current		ΣI_{OH}	—	-50	mA	
"H" level average total output current		ΣI_{OHAV}	—	-20	mA	*5
Power consumption		P_{D}	—	500	mW	
Operating temperature		T_{A}	-40	$+70$	°C	
Storage temperature		Tstg	-55	$+150$	°C	

*1: $V_{CC}5$ must not be less than $V_{SS} - 0.3$ V.

*2: Care must be taken that AV_{CC} and AVRH do not exceed $V_{CC}5 + 0.3$ V and $V_{SS} + 3.6$ V.
　　Also care must be taken that AVRH does not exceed AV_{CC}.

*3: Maximum output current is a peak current value measured at a corresponding pin.

*4: Average output current is an average current for a 100 ms period at a corresponding pin.

*5: Average total output current is an average current for a 100 ms period for all corresponding pins.

WARNING:　Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(1) At 5 V operation (4.5 V to 5.5 V)

$(V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}5$	4.5	5.5	V	Normal operation
	$V_{CC}5$	*1	*1	V	Retaining the RAM state in stop mode
	$V_{CC}3$	—	—	V	*2
Analog supply voltage	AV_{CC}	$V_{SS} + 2.7$	$V_{SS} + 3.6$	V	
Analog reference voltage	AVRH	$V_{SS} - 0.3$	AV_{CC}	V	
Operating temperature	T_A	–40	+70	°C	
Smoothing capacitor	C_S	0.1	1.0	µF	$V_{CC}3$ pin, *3

*1: At $V_{CC}5$, the RAM state holding is not warranted in stop mode.

*2: $V_{CC}3$ is used for the bypass capacitor pin.

*3: Use the ceramic capacitor or the capacitor whose frequency characteristic is equivalent to that of the ceramic capacitor.
And select the larger capacity bypass capacitor to connect to the power supply ($V_{CC}5$) than C_S.
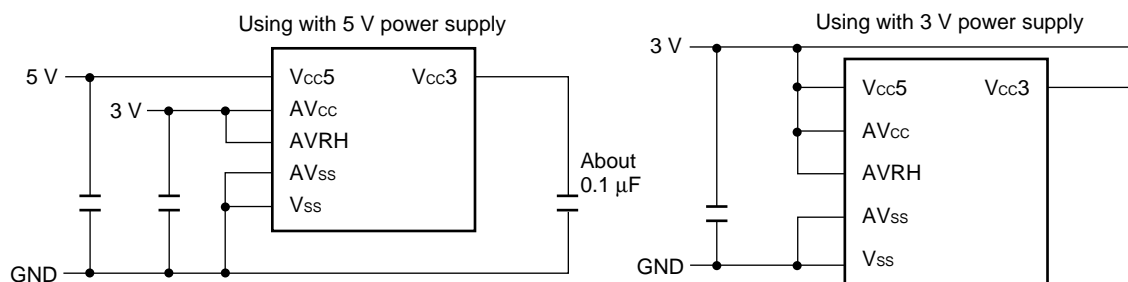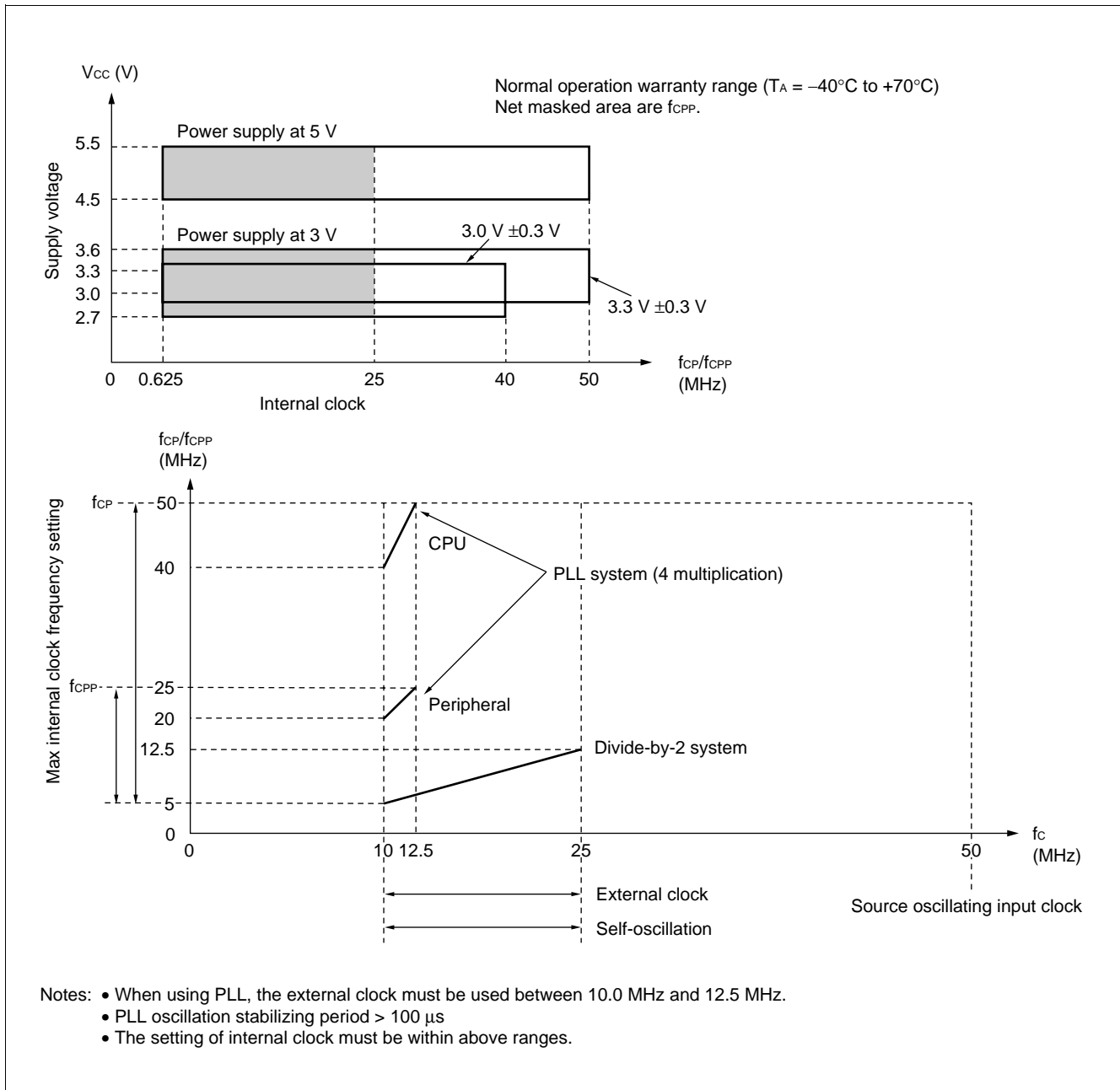
(2) At 3 V operation (2.7 V to 3.6 V)

$(V_{SS} = AV_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}5$	2.7	3.6	V	Normal operation
	$V_{CC}5$	2.7	3.6	V	Retaining the RAM state in stop mode
	$V_{CC}3$	2.7	3.6	V	*
Analog power supply voltage	AV_{CC}	$V_{SS} + 2.7$	$V_{SS} + 3.6$	V	
Analog reference voltage	AVRH	AV_{SS}	AV_{CC}	V	
Operating temperature	T_A	–40	+70	°C	

*: Connect to $V_{CC}5$ for the power supply pin.

- **Connecting to a power supply**

V_{CC} (V)

Supply voltage

Normal operation warranty range ($T_A = -40°C$ to $+70°C$)
Net masked area are f_{CPP}.

Power supply at 5 V

5.5

4.5

Power supply at 3 V

3.0 V ±0.3 V

3.6
3.3
3.0
2.7

3.3 V ±0.3 V

0   0.625   25   40   50 f_{CP}/f_{CPP}
                                                                (MHz)
              Internal clock

f_{CP}/f_{CPP}
(MHz)

Max internal clock frequency setting

f_{CP} — 50

CPU

40

PLL system (4 multiplication)

f_{CPP} — 25

Peripheral

20

12.5

Divide-by-2 system

5

0

0   10 12.5   25   50 f_C
                                                                (MHz)

External clock

Self-oscillation

Source oscillating input clock

Notes: • When using PLL, the external clock must be used between 10.0 MHz and 12.5 MHz.
       • PLL oscillation stabilizing period > 100 μs
       • The setting of internal clock must be within above ranges.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

MB91101/MB91101A

3. DC Characteristics

$(V_{CC}5 = 5.0\ V \pm 10\%,\ V_{SS} = AV_{SS} = 0.0\ V,\ T_A = -40°C\ to\ +70°C)$
$(V_{CC}5 = V_{CC}3 = 2.7\ V\ to\ 3.6\ V,\ V_{SS} = AV_{SS} = 0.0\ V,\ T_A = -40°C\ to\ +70°C)$

Parameter	Symbol	Pin name	Condition	Min	Typ	Max	Unit	Remarks
"H" level input voltage	V_{IH}	Input pin except for hysteresis input	—	$0.65 \times V_{CC}3$	—	$V_{CC}5 + 0.3$	V	*
	V_{IHS}	$\overline{HST}$, $\overline{NMI}$, $\overline{RST}$, PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	—	$0.8 \times V_{CC}3$	—	$V_{CC}5 + 0.3$	V	Hysteresis input *
"L" level input voltage	V_{IL}	Input other than following symbols	—	$V_{SS} - 0.3$	—	$0.25 \times V_{CC}3$	V	*
	V_{ILS}	$\overline{HST}$, $\overline{NMI}$, $\overline{RST}$, PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	—	$V_{SS} - 0.3$	—	$0.2 \times V_{CC}3$	V	Hysteresis input *
"H" level output voltage	V_{OH}	D16 to D31, A00 to A24, P60 to P67, P80 to P82, P85, PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7 $\overline{CS0}$, $\overline{WR0}$	$V_{CC}5 = 4.5\ V$ $I_{OH} = -4.0\ mA$	$V_{CC}5 - 0.5$	—	—	V	
			$V_{CC}5 = V_{CC}3 = 2.7\ V$ $I_{OH} = -4.0\ mA$	$V_{CC}5 - 0.8$	—	—		
"L" level output voltage	V_{OL}	D16 to D31, A00 to A24, P60 to P67, P80 to P82, P85, PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7 $\overline{CS0}$, $\overline{WR0}$	$V_{CC}5 = 4.5\ V$ $I_{OL} = 4.0\ mA$	—	—	0.4	V	
			$V_{CC}5 = V_{CC}3 = 2.7\ V$ $I_{OL} = 4.0\ mA$	—	—	0.6		
Input leakage current (High-Z output leakage current)	I_{LI}	D16 to D31, A00 to A23, P80 to P82, P85, PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7	$V_{CC}5 = 5.5\ V$ $0.45\ V < V_I < V_{CC}$	-5	—	$+5$	μA	
			$V_{CC}5 = V_{CC}3 = 3.6\ V$ $0.45\ V < V_I < V_{CC}$	-5	—	$+5$		

(Continued)

(Continued)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Pull-up resistance	R_{PULL}	RST	$V_{CC}5 = 5.5$ V $V_I = 0.45$ V	25	50	100	kΩ	
			$V_{CC}5 = V_{CC}3 = 3.6$ V $V_I = 0.45$ V	60	125	250		
Power supply current	I_{CC}	$V_{CC}5$, $V_{CC}3$	$F_C = 12.5$ MHz $V_{CC}5 = 5.5$ V	—	75	100	mA	(4 multipli-cation) Operation at 50 MHz
			$F_C = 12.5$ MHz $V_{CC}5 = V_{CC}3 = 3.6$ V	—	75	100		
	I_{CCS}	$V_{CC}5$, $V_{CC}3$	$F_C = 12.5$ MHz $V_{CC}5 = 5.5$ V	—	40	60	mA	Sleep mode
			$F_C = 12.5$ MHz $V_{CC}5 = V_{CC}3 = 3.6$ V	—	40	60		
	I_{CCH}	$V_{CC}5$, $V_{CC}3$	$T_A = +25°C$ $V_{CC}5 = 5.5$ V	—	10	100	μA	Stop mode
			$T_A = +25°C$ $V_{CC}5 = V_{CC}3 = 3.6$ V	—	10	100		
Input capacitance	C_{IN}	Except for $V_{CC}5$, $V_{CC}3$, AV_{CC}, AV_{SS}, V_{SS}	—	—	10	—	pF	

*: $V_{CC}3 = 3.3 \pm 0.2$ V (internal regulator output voltage) when using 5 V power supply, $V_{CC}3$ = power supply voltage when using 3 V power supply (internal regulator unused).

4. AC Characteristics

Measurement Conditions

- $V_{CC}5 = 5.0$ V $\pm 10\%$

Parameter	Symbol	Value			Unit	Remarks
		Min	**Typ**	**Max**		
"H" level input voltage	V_{IH}	—	2.4	—	V	
"L" level input voltage	V_{IL}	—	0.8	—	V	
"H" level output voltage	V_{OH}	—	2.4	—	V	
"L" level output voltage	V_{OL}	—	0.8	—	V	
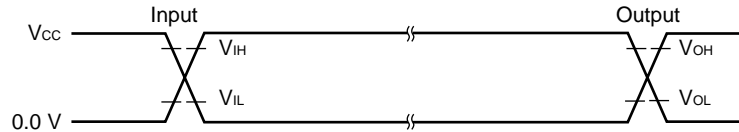
- $V_{CC}5 = V_{CC}3 = 2.7$ V to 3.6 V

Parameter	Symbol	Value			Unit	Remarks
		Min	**Typ**	**Max**		
"H" level input voltage	V_{IH}	—	$1/2 \times V_{CC}3$	—	V	
"L" level input voltage	V_{IL}	—	$1/2 \times V_{CC}3$	—	V	
"H" level output voltage	V_{OH}	—	$1/2 \times V_{CC}3$	—	V	
"L" level output voltage	V_{OL}	—	$1/2 \times V_{CC}3$	—	V	
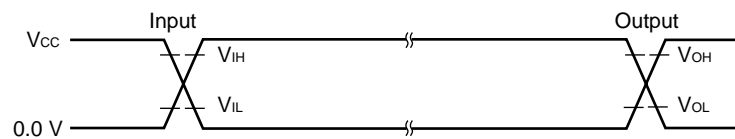
- **Load conditions**
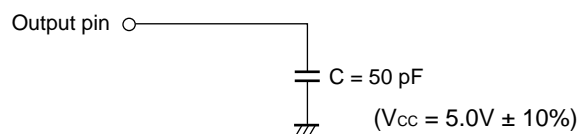
• **Load capacitance - Delay characteristics (Output delay with reference to the internal)**
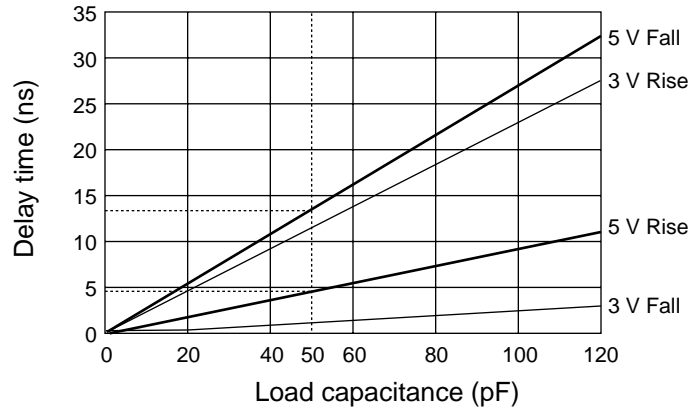
(1) Clock Timing Rating

$$(V_{CC}5 = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$$
$$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Clock frequency	f_C	X0, X1	When using PLL	10	12.5	MHz	
	f_C	X0, X1	Self-oscillation (divide-by-2 input)	10	25	MHz	
	f_C	X0, X1	External clock (divide-by-2 input)	10	25	MHz	
Clock cycle time	t_C	X0, X1	When using PLL	80	100	ns	
	t_C	X0, X1	—	40	100	ns	
Input clock pulse width	P_{WH}, P_{WL}	X0, X1	—	25	—	ns	Input to X0 only, when using 5 V power supply
	P_{WH}, P_{WL}	X0, X1		10	—	ns	Input to X0, X1
Input clock rising/falling time	t_{CR}, t_{CF}	X0, X1		—	8	ns	$(t_{CR} + t_{CF})$
Internal operating clock frequency	f_{CP}	—	CPU system	0.625[1]	50	MHz	
	f_{CPB}	—	Bus system	0.625[1]	25[2]	MHz	
	f_{CPP}	—	Peripheral system	0.625[1]	25	MHz	
Internal operating clock cycle time	t_{CP}	—	CPU system	20	1600[1]	ns	
	t_{CPB}	—	Bus system	40[2]	1600[1]	ns	
	t_{CPP}	—	Peripheral system	40	1600[1]	ns	

*1: These values are for a minimum clock of 10 MHz input to X0, a divide-by-2 system of the source oscillation and a 1/8 gear.

*2: Values when using the doubler and CPU operation at 50 MHz.

• **Clock timing rating measurement conditions**
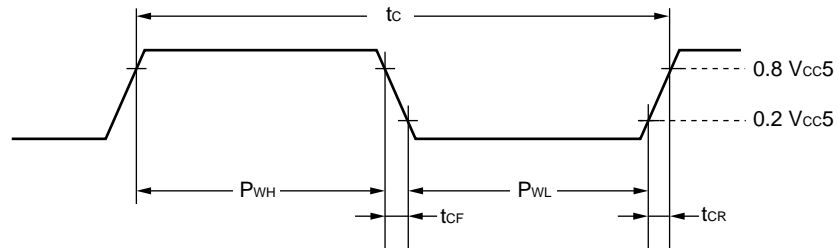
(2) Clock Output Timing

$(V_{CC}5 = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$
$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	*1
	t_{CYC}	CLK	Using the doubler	t_{CPB}	—	ns	
CLK $\uparrow \rightarrow$ CLK $\downarrow$	t_{CHCL}	CLK	—	$1/2 \times t_{CYC} - 10$	$1/2 \times t_{CYC} + 10$	ns	*2
CLK $\downarrow \rightarrow$ CLK $\uparrow$	t_{CLCH}	CLK		$1/2 \times t_{CYC} - 10$	$1/2 \times t_{CYC} + 10$	ns	*3

t_{CP}, t_{CPB} (internal operating clock cycle time): Refer to "(1) Clock Timing Rating."

*1: t_{CYC} is a frequency for 1 clock cycle including a gear cycle.
    Use the doubler when CPU frequency is above 25 MHz.

*2: Rating at a gear cycle of $\times 1$.
    When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute "n" in the following equations with 1/2, 1/4, 1/8, respectively.

    Min : $(1 - n/2) \times t_{CYC} - 10$
    Max : $(1 - n/2) \times t_{CYC} + 10$

    Select a gear cycle of $\times 1$ when using the doubler.

*3: Rating at a gear cycle of $\times 1$.
    When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute "n" in the following equations with 1/2, 1/4, 1/8, respectively.

    Min : $n/2 \times t_{CYC} - 10$
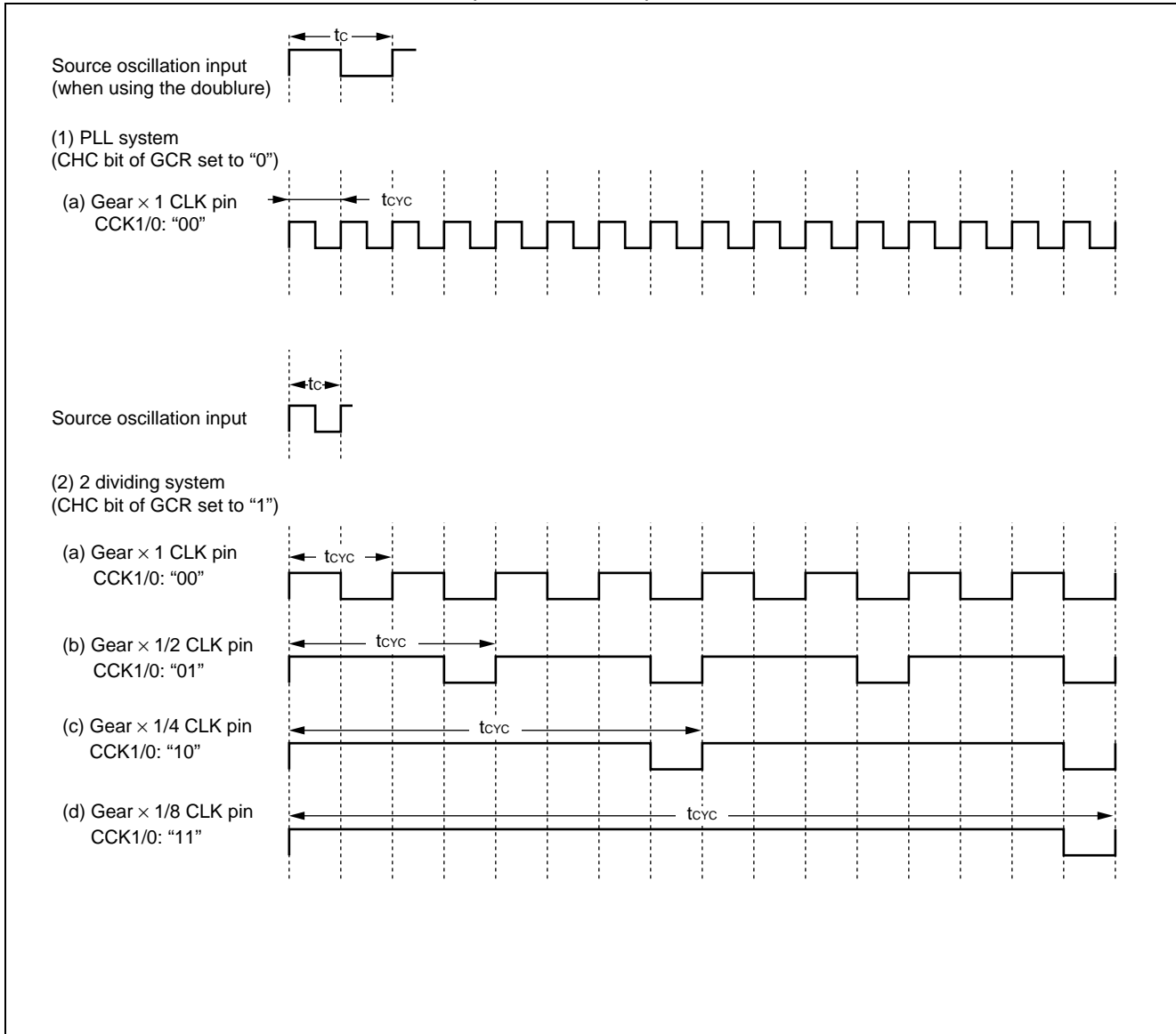
    Max : $n/2 \times t_{CYC} + 10$

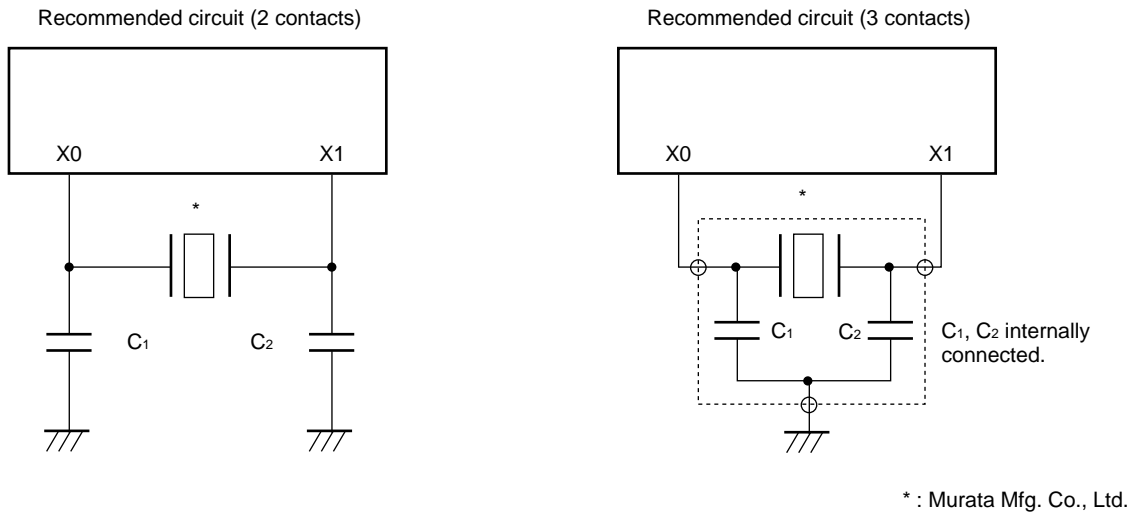   Select a gear cycle of $\times 1$ when using the doubler.
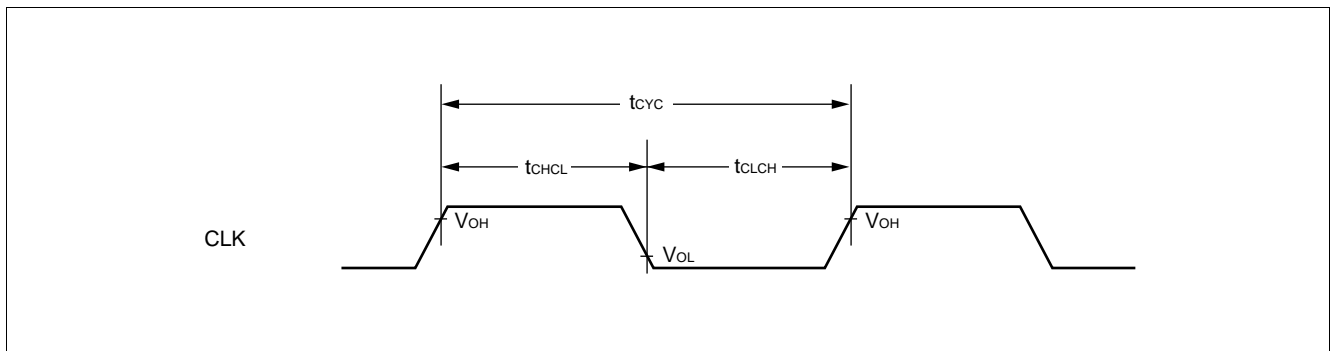
The relation between the input waveform of source oscillation and the output waveform of CLK pin for configured by CHC/CCK1/CCK0 settings of GCR (gear control register) is as follows:

However, in this chart source oscillation input means X0 input clock.

• **Ceramic oscillator applications**

Recommended circuit (2 contacts)　　　　　　　　　　Recommended circuit (3 contacts)

* : Murata Mfg. Co., Ltd.

• **Discreet type**

Oscillation frequency [MHz]	Model	Load capacitance $C_1 = C_2$ [pF]	Power supply voltage $V_{CC}5$ [V]
5.00 to 6.30	CSA☐☐☐MG	30	2.9 to 5.5
	CST☐☐☐MGW	(30)	
	CSA☐☐☐MG093	30	2.7 to 5.5
	CST☐☐☐MGW093	(30)	
6.31 to 10.0	CSA☐☐☐MTZ	30	2.9 to 5.5
	CST☐☐☐MTW	(30)	
	CSA☐☐☐MTZ093	30	2.7 to 5.5
	CST☐☐☐MTW093	(30)	
10.1 to 13.0	CSA☐☐☐MTZ	30	3.0 to 5.5
	CST☐☐☐MTW	(30)	
	CSA☐☐☐MTZ093	30	2.9 to 5.5
	CST☐☐☐MTW093	(30)	
13.01 to 15.00	CSA☐☐☐☐MXZ040	15	3.2 to 5.5
	CST☐☐☐☐MXW0C3	(15)	

( ): C_1 and C_2 internally connected 3 contacts type.

(3) Reset/Hardware Standby Input Ratings

$(V_{CC}5 = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$

$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	$t_{CP} \times 5$	—	ns	
Hardware standby input time	t_{HSTL}	$\overline{HST}$		$t_{CP} \times 5$	—	ns	

t_{CP} (internal operating clock cycle time): Refer to "(1) Clock Timing Rating."
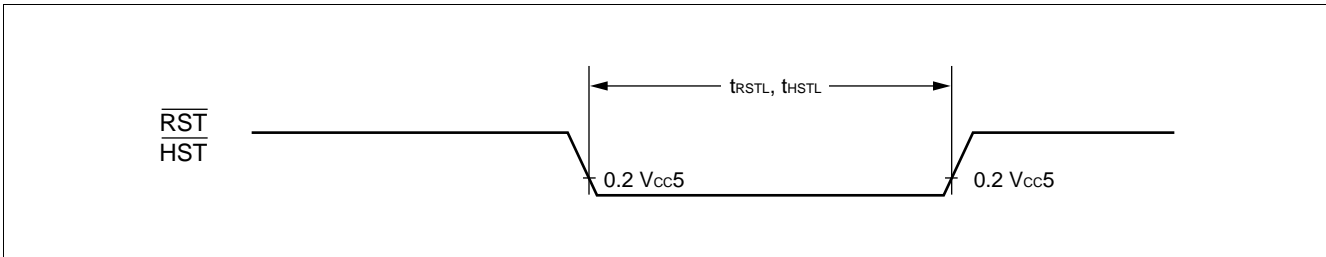
(4) Power on Supply Specifications (Power-on Reset)

$$(V_{CC}5 = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$$
$$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rising time	t_R	V_{CC}	V_{CC} = 5.0 V	50	—	µs	*
	t_R	V_{CC}		—	30	ms	*
	t_R	V_{CC}	V_{CC} = 3.0/3.3 V	50	—	µs	*
	t_R	V_{CC}		—	18	ms	*
Power supply shut off time	t_{OFF}	V_{CC}	—	1	—	ms	Repeated operations

t_C (clock cycle time): Refer to "(1) Clock Timing Rating."

*: V_{CC} < 0.2 V before the power supply rising

Note: Sudden change in supply voltage during operation may initiate a power-on sequence.
To change supply voltage during operation, it is recommended to smoothly raise the voltage to avoid rapid fluctuations in the supply voltage.

A voltage rising rate of 50 mV/ms or less is recommended.

t_{RSTL}: Reset input time

*: Reset can't be done during regulator stabilizing time.

Note: Set $\overline{RST}$ pin to "L" level when turning on the device, at least the described above duration after the supply voltage reaches Vcc is necessary before turning the $\overline{RST}$ to "H" level.

(5) Normal Bus Access Read/Write Operation

$(V_{CC}5 = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°\text{C to} +70°\text{C})$
$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°\text{C to} +70°\text{C})$

Parameter	Symbol	Pin name	Condition	Value Min	Value Max	Unit	Remarks
$\overline{CS0}$ to $\overline{CS5}$ delay time	t_{CHCSL}	CLK, $\overline{CS0}$ to $\overline{CS5}$	—	—	15	ns	
	t_{CHCSH}	CLK, $\overline{CS0}$ to $\overline{CS5}$		—	15	ns	
Address delay time	t_{CHAV}	CLK, A24 to A00		—	15	ns	
Data delay time	t_{CHDV}	CLK, D31 to D16		—	15	ns	
$\overline{RD}$ delay time	t_{CLRL}	CLK, $\overline{RD}$		—	6	ns	
	t_{CLRH}	CLK, $\overline{RD}$		—	6	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CLWL}	CLK, $\overline{WR0}$, $\overline{WR1}$		—	6	ns	
	t_{CLWH}	CLK, $\overline{WR0}$, $\overline{WR1}$		—	6	ns	
Valid address → valid data input time	t_{AVDV}	A24 to A00, D31 to D16		—	$3/2 \times t_{CYC} - 25$	ns	*1 *2
$\overline{RD}$ ↓→ valid data input time	t_{RLDV}	$\overline{RD}$, D31 to D16		—	$t_{CYC} - 10$	ns	*1
Data set up → $\overline{RD}$ ↑ time	t_{DSRH}	$\overline{RD}$, D31 to D16		10	—	ns	
$\overline{RD}$ ↑→ data hold time	t_{RHDX}	$\overline{RD}$, D31 to D16		0	—	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to "(2) Clock Output Timing."

*1: When bus timing is delayed by automatic wait insertion or RDY input, add ($t_{CYC} \times$ extended cycle number for delay) to this rating.

*2: Rating at a gear cycle of $\times 1$.
When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute "n" in the following equation with 1/2, 1/4, 1/8, respectively.
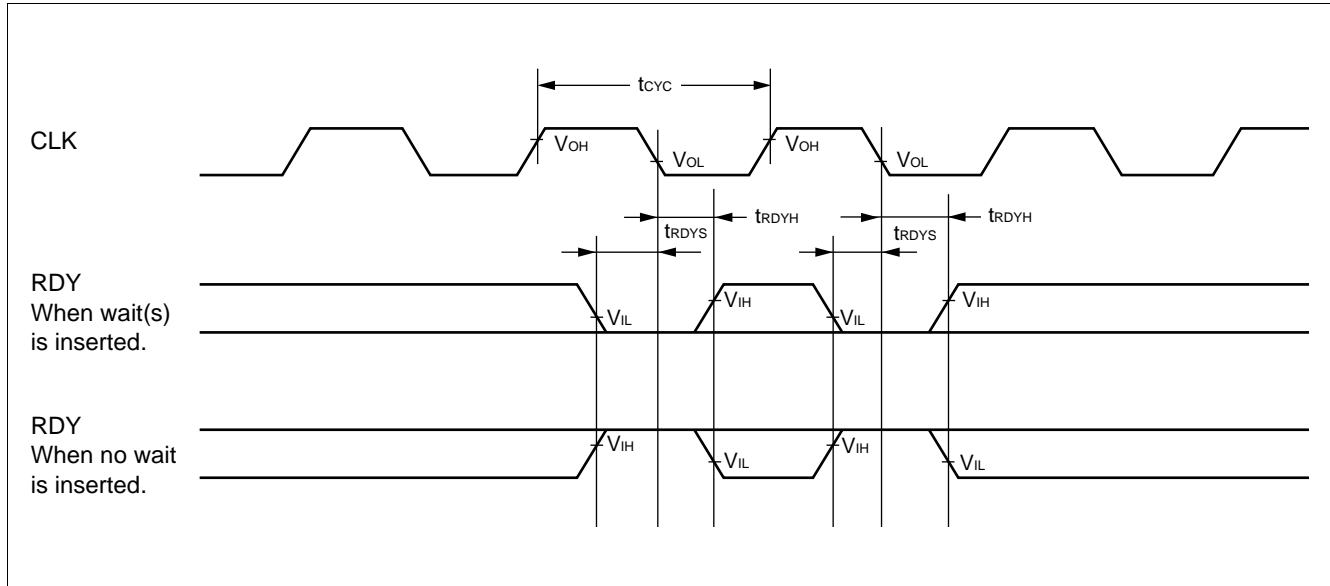
Equation: $(2 - n/2) \times t_{CYC} - 25$
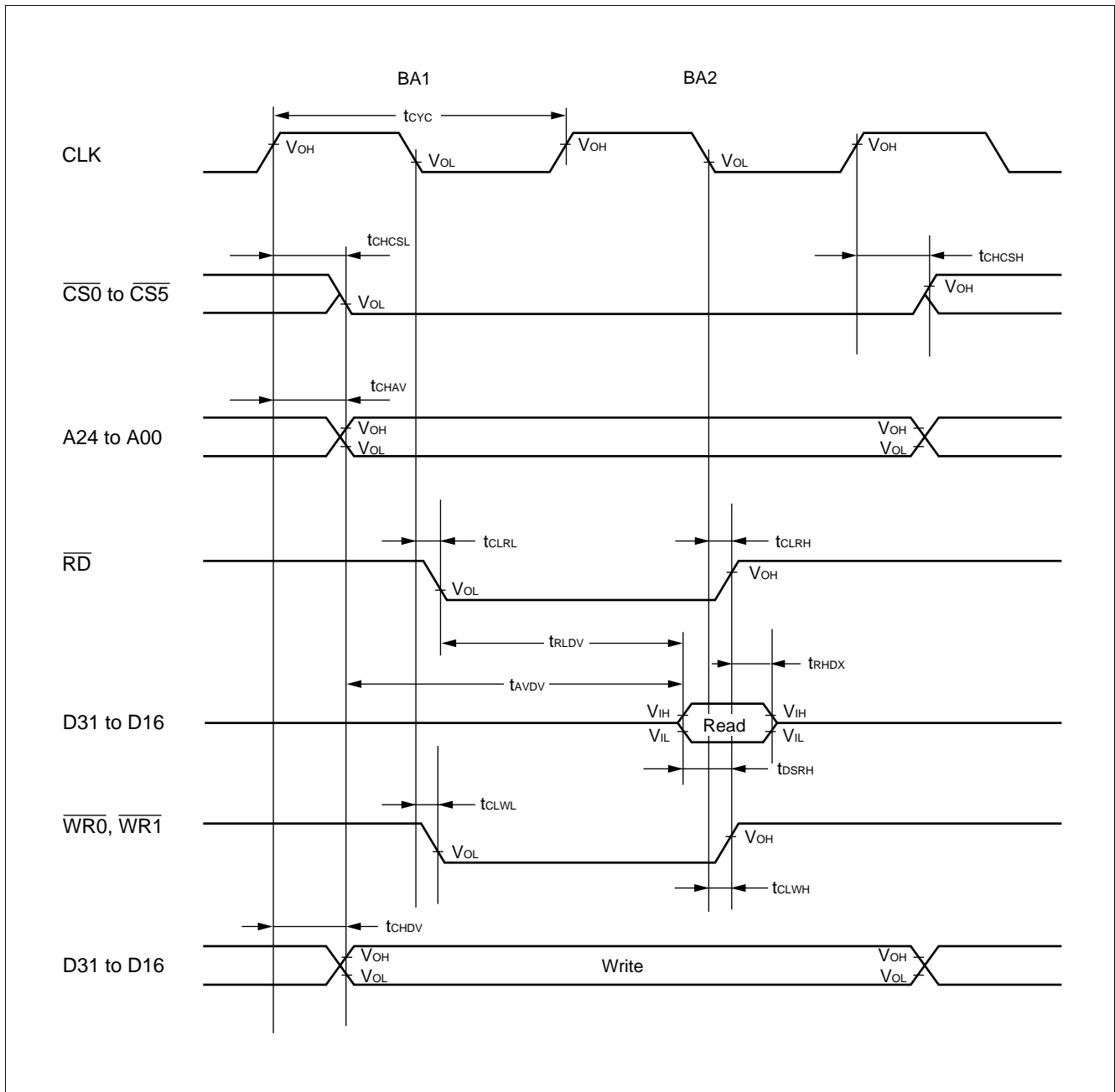
(6) Ready Input Timing

$(V_{CC}5 = 5.0 \text{ V } \pm10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$
$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RDY set up time → CLK ↓	t_{RDYS}	RDY, CLK	—	15	—	ns	
CLK ↓→ RDY hold time	t_{RDYH}	RDY, CLK		0	—	ns	

(7) Hold Timing

$(V_{CC}5 = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$
$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{\text{BGRNT}}$ delay time	t_{CHBGL}	CLK, $\overline{\text{BGRNT}}$	—	—	6	ns	
	t_{CHBGH}	CLK, $\overline{\text{BGRNT}}$	—	—	6	ns	
Pin floating $\rightarrow \overline{\text{BGRNT}} \downarrow$ time	t_{XHAL}	$\overline{\text{BGRNT}}$		$t_{CYC} - 10$	$t_{CYC} + 10$	ns	
$\overline{\text{BGRNT}} \uparrow \rightarrow$ pin valid time	t_{HAHV}	$\overline{\text{BGRNT}}$		$t_{CYC} - 10$	$t_{CYC} + 10$	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to "(2) Clock Output Timing."

Note : There is a delay time of more than 1 cycle from BRQ input to $\overline{\text{BGRNT}}$ change.
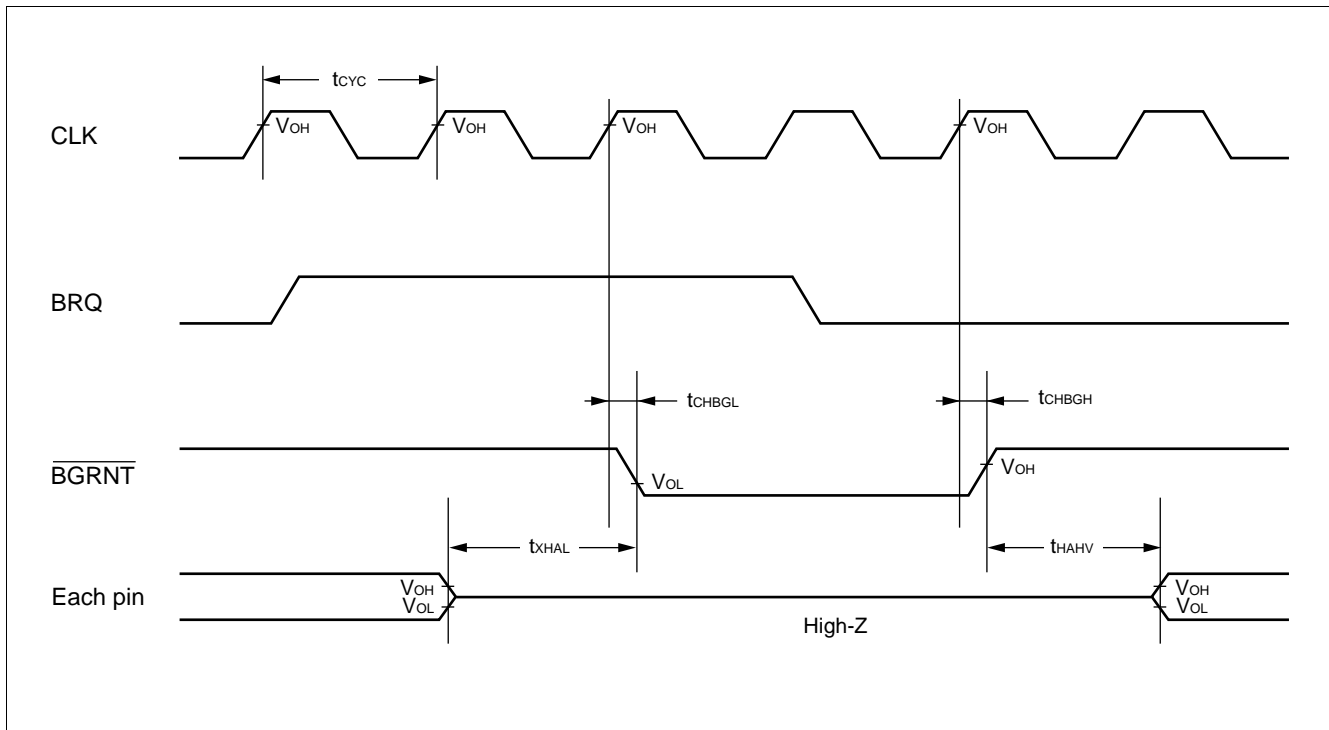
(8) Normal DRAM Mode Read/Write Cycle

$(V_{CC}5 = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$
$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$

Parameter	Symbol	Pin name	Condition	Value Min	Value Max	Unit	Remarks
RAS delay time	t_{CLRAH}	CLK, RAS0, RAS1	—	—	6	ns	
	t_{CHRAL}	CLK, RAS0, RAS1		—	6	ns	
CAS delay time	t_{CLCASL}	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
	t_{CLCASH}	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
ROW address delay time	t_{CHRAV}	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV}	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWL}	CLK, $\overline{DW0}$, $\overline{DW1}$		—	15	ns	
	t_{CHDWH}	CLK, $\overline{DW0}$, $\overline{DW1}$		—	15	ns	
Output data delay time	t_{CHDV1}	CLK, D31 to D16		—	15	ns	
RAS $\downarrow\rightarrow$ valid data input time	t_{RLDV}	RAS0, RAS1, D31 to D16		—	$5/2 \times t_{CYC} - 16$	ns	*1 *2
CAS $\downarrow\rightarrow$ valid data input time	t_{CLDV}	CS0H, CS0L, CS1H, CS1L, D31 to D16		—	$t_{CYC} - 17$	ns	*1
CAS $\uparrow\rightarrow$ data hold time	t_{CADH}	CS0H, CS0L, CS1H, CS1L, D31 to D16		0	—	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to "(2) Clock Output Timing."

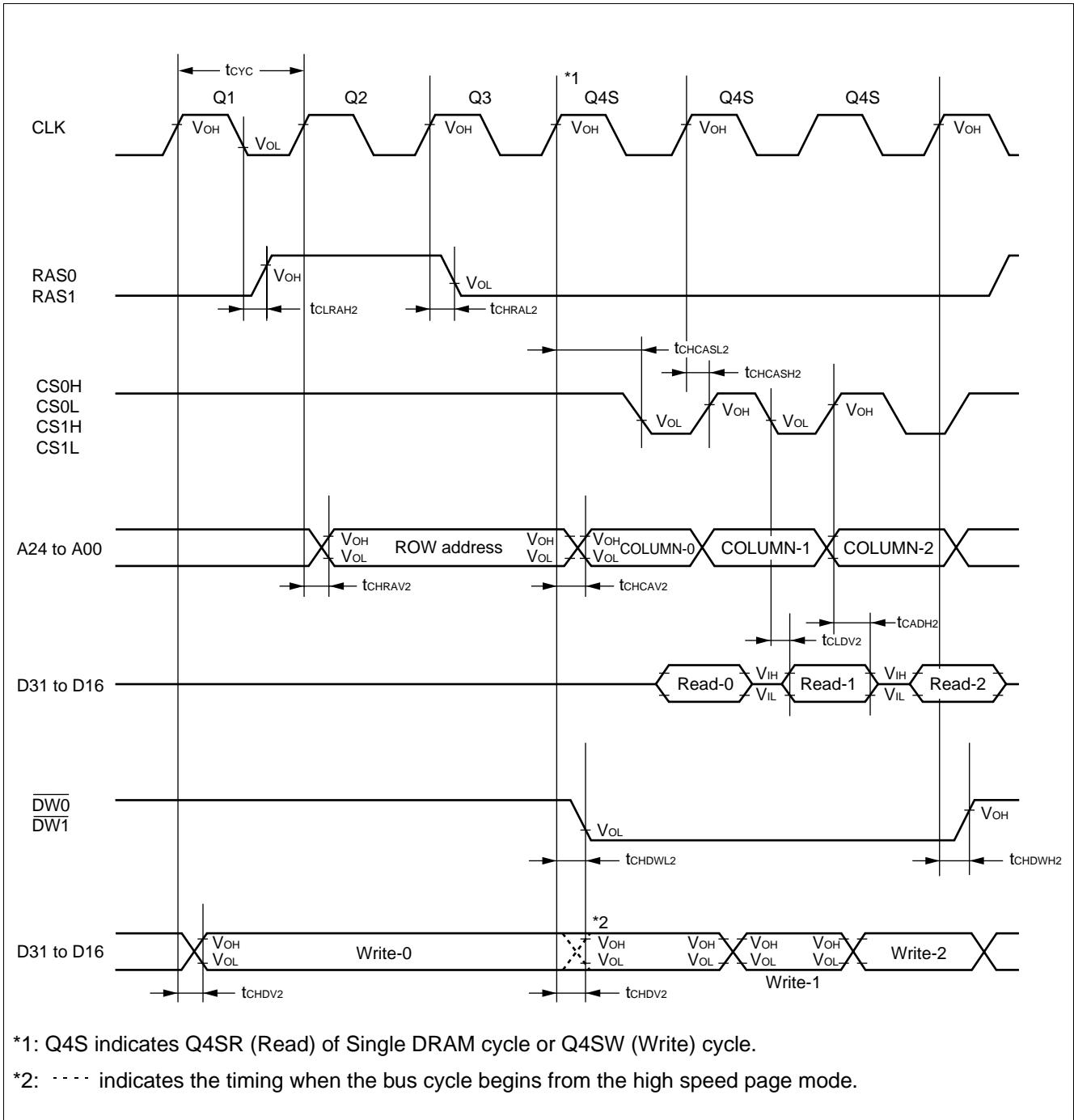*1: When Q1 cycle or Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.

*2: Rating at a gear cycle of $\times 1$.
 When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute "n" in the following equation with 1/2, 1/4, 1/8, respectively.

 Equation: $(3 - n/2) \times t_{CYC} - 16$

Q1   Q2   Q3   Q4   Q5

CLK

t_{CYC}

V_{OH} V_{OL} V_{OH} V_{OH} V_{OH} V_{OL} V_{OL} V_{OH}

RAS0
RAS1

V_{OH}
V_{OL}

t_{CLRAH} t_{CHRAL}

CS0H
CS0L
CS1H
CS1L

t_{CLCASH} t_{CLCASH}

V_{OL} V_{OH}

t_{CHRAV} t_{CHCAV}

A24 to A00

V_{OH}
V_{OL} ROW address V_{OH} V_{OH}
V_{OL} V_{OL} COLUMN address V_{OH}
V_{OL}

t_{RLDV}

t_{CLDV} t_{CADH}

D31 to D16

V_{IH}
V_{IL} Read V_{IH}
V_{IL}

$\overline{DW0}$
$\overline{DW1}$

V_{OL} V_{OH}

t_{CHDWL} t_{CHDWH}

D31 to D16

V_{OH}
V_{OL} Write V_{OH}
V_{OL}

t_{CHDV1}
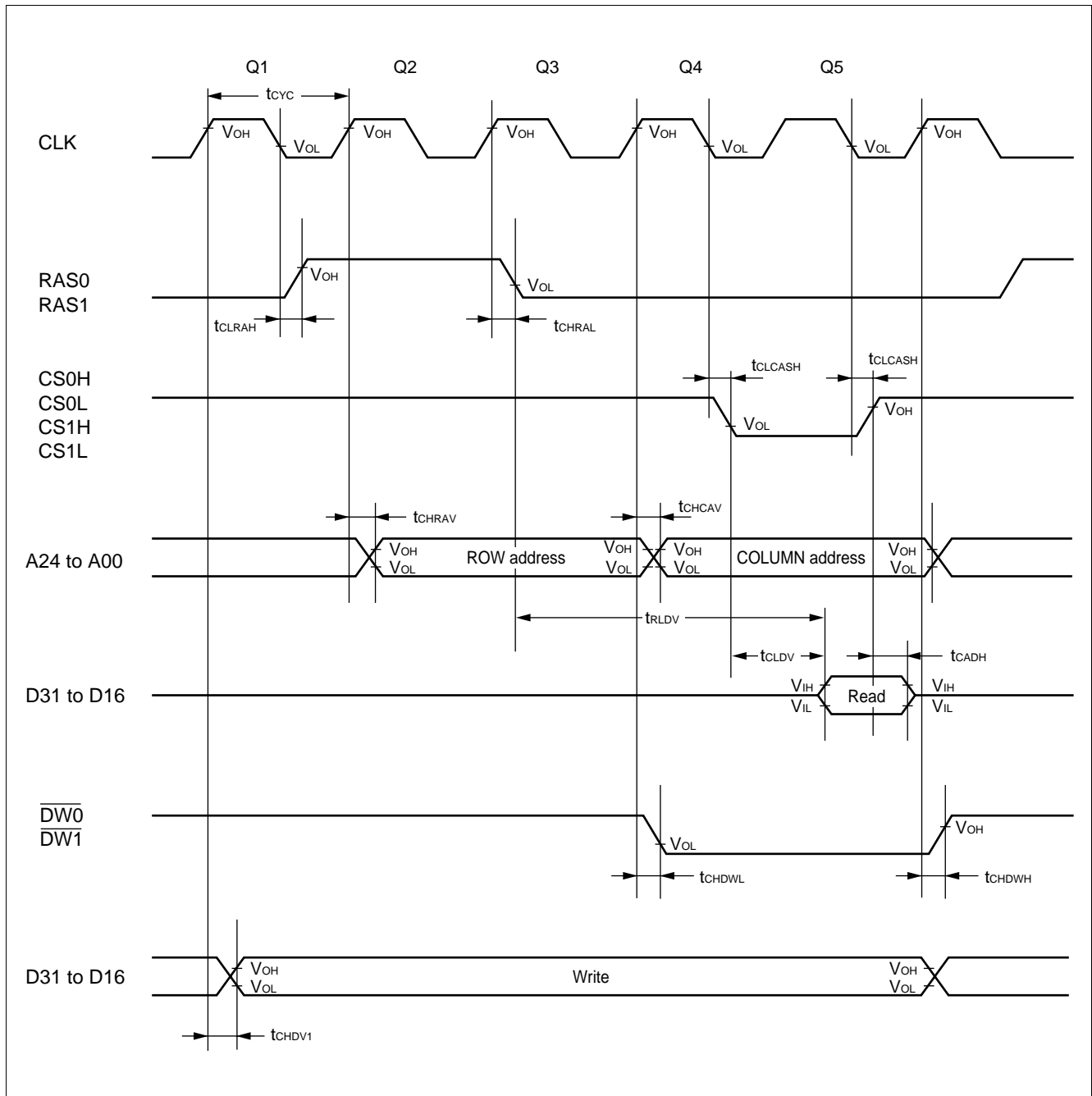
(9) Normal DRAM Mode Fast Page Read/Write Cycle

$(V_{CC}5 = 5.0\ V \pm 10\%, V_{SS} = AV_{SS} = 0.0\ V, T_A = -40°C\ to\ +70°C)$

$(V_{CC}5 = V_{CC}3 = 2.7\ V\ to\ 3.6\ V, V_{SS} = AV_{SS} = 0.0\ V, T_A = -40°C\ to\ +70°C)$

Parameter	Symbol	Pin name	Condition	Value Min	Value Max	Unit	Remarks
RAS delay time	t_{CLRAH}	CLK, RAS0, RAS1	—	—	6	ns	
CAS delay time	t_{CLCASL}	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
	t_{CLCASH}	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
COLUMN address delay time	t_{CHCAV}	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWH}	CLK, $\overline{DW0}$, $\overline{DW1}$		—	15	ns	
Output data delay time	t_{CHDV1}	CLK, D31 to D16		—	15	ns	
CAS $\downarrow\rightarrow$ valid data input time	t_{CLDV}	CS0H, CS0L, CS1H, CS1L, D31 to D16		—	$t_{CYC} - 17$	ns	*
CAS $\uparrow\rightarrow$ data hold time	t_{CADH}	CS0H, CS0L, CS1H, CS1L, D31 to D16		0	—	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to "(2) Clock Output Timing."

*: When Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.
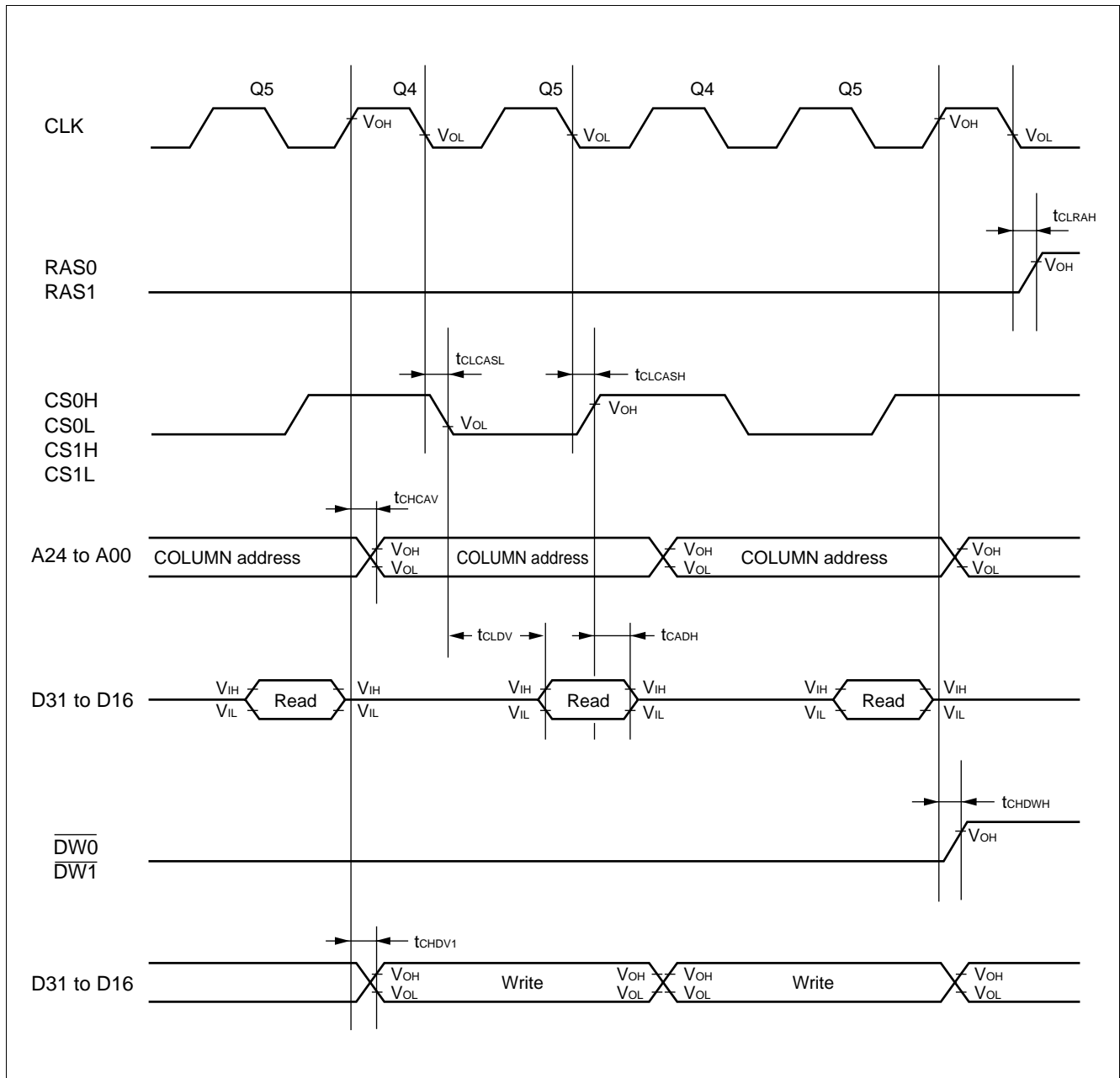
(10) Single DRAM Timing

$(V_{CC}5 = 5.0\ V \pm 10\%,\ V_{SS} = AV_{SS} = 0.0\ V,\ T_A = -40°C\ to\ +70°C)$
$(V_{CC}5 = V_{CC}3 = 2.7\ V\ to\ 3.6\ V,\ V_{SS} = AV_{SS} = 0.0\ V,\ T_A = -40°C\ to\ +70°C)$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	t_{CLRAH2}	CLK, RAS0, RAS1	—	—	6	ns	
	t_{CHRAL2}	CLK, RAS0, RAS1			6	ns	
CAS delay time	$t_{CHCASL2}$	CLK, CS0H, CS0L, CS1H, CS1L		—	$n/2 \times t_{CYC}$	ns	
	$t_{CHCASH2}$	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
ROW address delay time	t_{CHRAV2}	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV2}	CLK, A24 to A00		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWL2}	CLK, $\overline{DW0}$, $\overline{DW1}$		—	15	ns	
	t_{CHDWH2}	CLK, $\overline{DW0}$, $\overline{DW1}$		—	15	ns	
Output data delay time	t_{CHDV2}	CLK, D31 to D16		—	15	ns	
CAS $\downarrow\rightarrow$ Valid data input time	t_{CLDV2}	CS0H, CS0L, CS1H, CS1L, D31 to D16		—	$(1-n/2) \times t_{CYC} - 17$	ns	
CAS $\uparrow\rightarrow$ data hold time	t_{CADH2}	CS0H, CS0L, CS1H, CS1L, D31 to D16		0	—	ns	

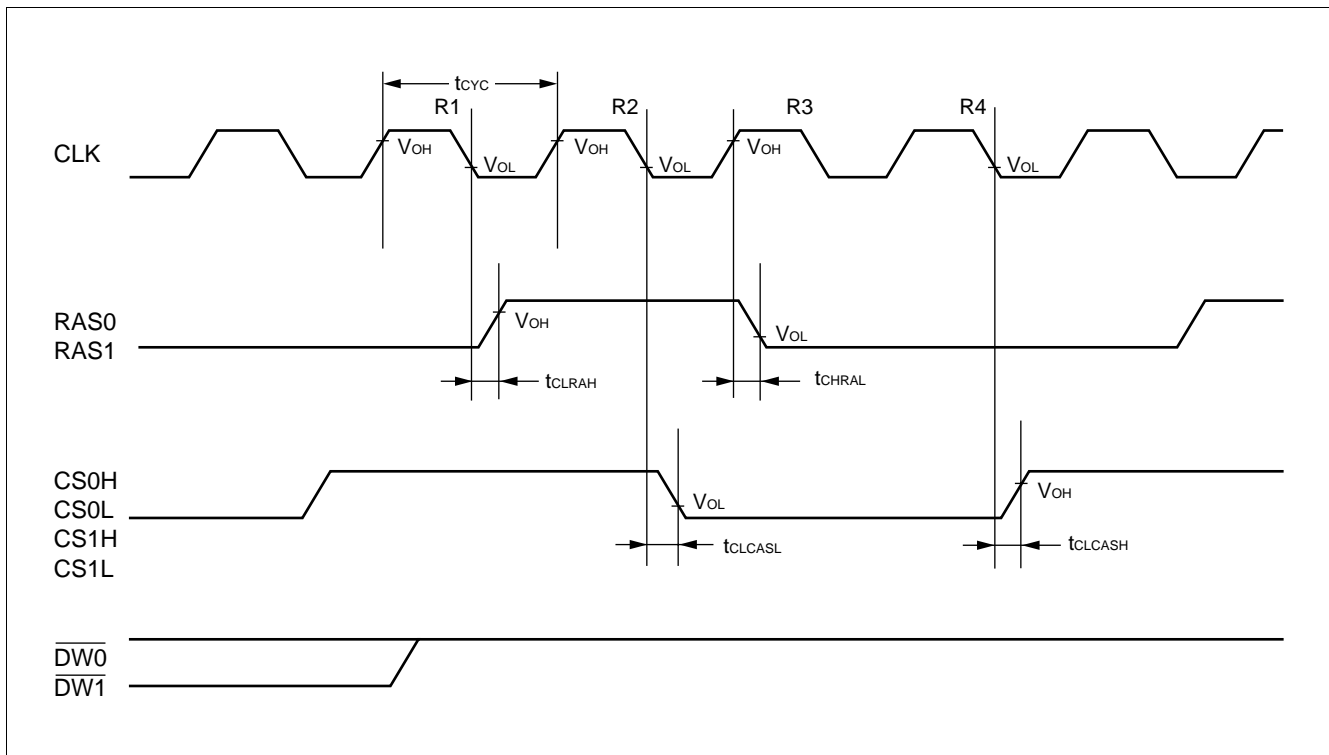t_{CYC} (a cycle time of peripheral system clock): Refer to "(2) Clock Output Timing."

*1: Q4S indicates Q4SR (Read) of Single DRAM cycle or Q4SW (Write) cycle.

*2: ‐ ‐ ‐ ‐ indicates the timing when the bus cycle begins from the high speed page mode.

(11) Hyper DRAM Timing

$(V_{CC}5 = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$

$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$

Parameter	Symbol	Pin name	Condition	Value Min	Value Max	Unit	Remarks
RAS delay time	t_{CLRAH3}	CLK, RAS0, RAS1	—	—	6	ns	
	t_{CHRAL3}	CLK, RAS0, RAS1		—	6	ns	
CAS delay time	$t_{CHCASL3}$	CLK, CS0H, CS0L, CS1H, CS1L		—	$n/2 \times t_{CYC}$	ns	
	$t_{CHCASH3}$	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
ROW address delay time	t_{CHRAV3}	CLK, A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV3}	CLK, A24 to A00		—	15	ns	
$\overline{RD}$ delay time	t_{CHRL3}	CLK, $\overline{RD}$		—	15	ns	
	t_{CHRH3}	CLK, $\overline{RD}$		—	15	ns	
	t_{CLRL3}	CLK, $\overline{RD}$		—	15	ns	
$\overline{DW}$ delay time	t_{CHDWL3}	CLK, $\overline{DW0}$, $\overline{DW1}$		—	15	ns	
	t_{CHDWH3}	CLK, $\overline{DW0}$, $\overline{DW1}$		—	15	ns	
Output data delay time	t_{CHDV3}	CLK, D31 to D16		—	15	ns	
CAS $\downarrow \rightarrow$ valid data input time	t_{CLDV3}	CS0H, CS0L, CS1H, CS1L, D31 to D16		—	$t_{CYC} - 17$	ns	
CAS $\downarrow \rightarrow$ data hold time	t_{CADH3}	CS0H, CS0L, CS1H, CS1L, D31 to D16		0	—	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to "(2) Clock Output Timing."

*1: Q4H indicates Q4HR (Read) of Hyper DRAM cycle or Q4HW (Write) cycle.

*2: - - - indicates the timing when the bus cycle begins from the high speed page mode.

(12) CBR Refresh

$(V_{CC}5 = 5.0\ V \pm 10\%, V_{SS} = AV_{SS} = 0.0\ V, T_A = -40°C\ to\ +70°C)$
$(V_{CC}5 = V_{CC}3 = 2.7\ V\ to\ 3.6\ V, V_{SS} = AV_{SS} = 0.0\ V, T_A = -40°C\ to\ +70°C)$

Parameter	Symbol	Pin name	Condition	Value Min	Max	Unit	Remarks
RAS delay time	t_{CLRAH}	CLK, RAS0, RAS1	—	—	6	ns	
	t_{CHRAL}	CLK, RAS0, RAS1		—	6	ns	
CAS delay time	t_{CLCASL}	CLK, CS0H, CS0L, CS1H, CS1L	—	—	6	ns	
	t_{CLCASH}	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	

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(13) Self Refresh

$(V_{CC}5 = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$
$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RAS delay time	t_{CLRAH}	CLK, RAS0, RAS1	—	—	6	ns	
	t_{CHRAL}	CLK, RAS0, RAS1		—	6	ns	
CAS delay time	t_{CLCASL}	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	
	t_{CLCASH}	CLK, CS0H, CS0L, CS1H, CS1L		—	6	ns	

(14) UART Timing

$(V_{CC}5 = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$
$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°C \text{ to } +70°C)$

Parameter	Symbol	Pin name	Condition	Value Min	Value Max	Unit	Remarks
Serial clock cycle time	t_{SCYC}	—	Internal shift clock mode	$8 \times t_{CYCP}$	—	ns	
SCLK $\downarrow\rightarrow$ SCLK $\uparrow$	t_{SCLCH}	—		$4 \times t_{CYCP} -10$	$4 \times t_{CYCP} +10$	ns	
SCLK $\uparrow\rightarrow$ SCLK $\downarrow$	t_{SCHCL}	—		$4 \times t_{CYCP} -10$	$4 \times t_{CYCP} +10$	ns	
SCLK $\downarrow\rightarrow$ SOUT delay time	t_{SLOV}	—		-80	$+80$	ns	
Valid SIN $\rightarrow$ SCLK $\uparrow$	t_{IVSH}	—		100	—	ns	
SCLK $\uparrow\rightarrow$ valid SIN hold time	t_{SHIX}	—		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	—	External shift clock mode	$4 \times t_{CYCP}$	—	ns	
Serial clock "L" pulse width	t_{SLSH}	—		$4 \times t_{CYCP}$	—	ns	
SCLK $\downarrow\rightarrow$ SOUT delay time	t_{SLOV}	—		—	150	ns	
Valid SIN $\rightarrow$ SCLK $\uparrow$	t_{IVSH}	—		60	—	ns	
SCLK $\uparrow\rightarrow$ valid SIN hold time	t_{SHIX}	—		60	—	ns	

t_{CYCP}: A cycle time of peripheral system clock

Note : This rating is for AC characteristics in CLK synchronous mode.

• Internal shift clock mode

• External shift clock mode
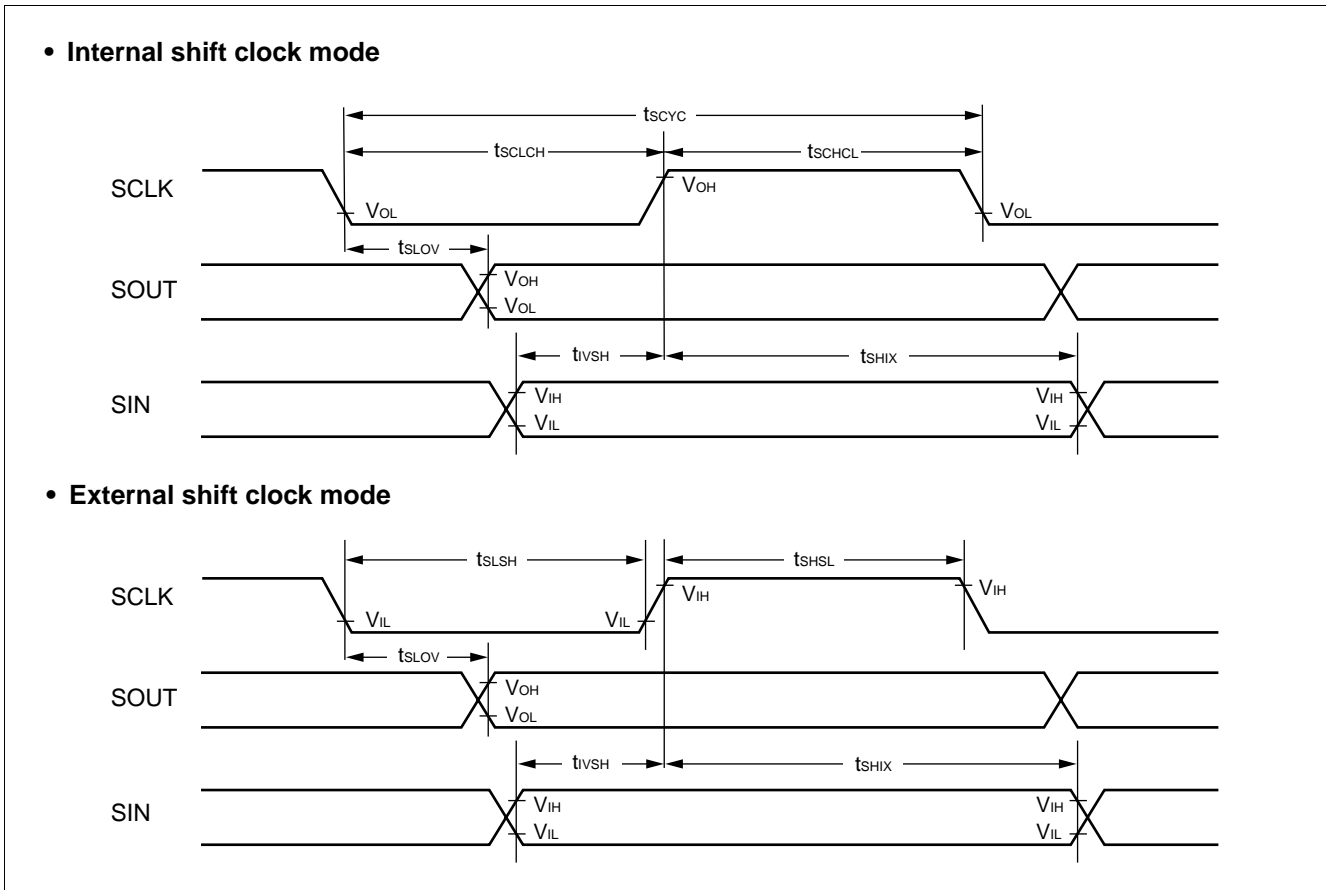
(15) Trigger System Input Timing

$(V_{CC}5 = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°\text{C to } +70°\text{C})$
$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°\text{C to } +70°\text{C})$

Parameter	Symbol	Pin name	Condition	Value Min	Value Max	Unit	Remarks
A/D start trigger input time	t_{TRGH}, t_{TRGL}	$\overline{ATG}$	—	$5 \times t_{CYCP}$	—	ns	
PWM external trigger input time	t_{TRGH}, t_{TRGL}	TRG0 to TRG3	—	$5 \times t_{CYCP}$	—	ns	

t_{CYCP}: A cycle time of peripheral system clock
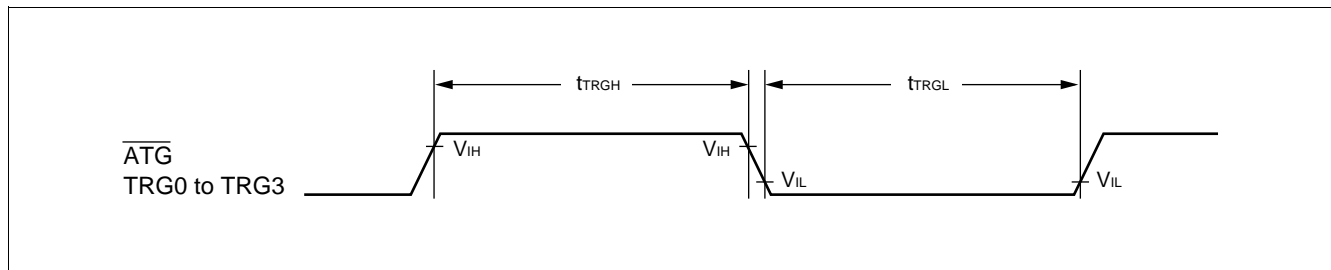
(16) DMA Controller Timing

$(V_{CC}5 = 5.0 \text{ V} \pm 10\%, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°\text{C to } +70°\text{C})$
$(V_{CC}5 = V_{CC}3 = 2.7 \text{ V to } 3.6 \text{ V}, V_{SS} = AV_{SS} = 0.0 \text{ V}, T_A = -40°\text{C to } +70°\text{C})$

Parameter	Symbol	Pin name	Condition	Value Min	Max	Unit	Remarks
DREQ input pulse width	t_{DRWH}	DREQ0 to DREQ2	—	$2 \times t_{CYC}$	—	ns	
DACK delay time (Normal bus) (Normal DRAM)	t_{CLDL}	CLK, DACK0 to DACK2		—	6	ns	
	t_{CLDH}	CLK, DACK0 to DACK2		—	6	ns	
EOP delay time (Normal bus) (Normal DRAM)	t_{CLEL}	CLK, EOP0 to EOP2		—	6	ns	
	t_{CLEH}	CLK, EOP0 to EOP2		—	6	ns	
DACK delay time (Single DRAM) (Hyper DRAM)	t_{CHDL}	CLK, DACK0 to DACK2		—	$n/2 \times t_{CYC}$	ns	
	t_{CHDH}	CLK, DACK0 to DACK2		—	6	ns	
EOP delay time (Single DRAM) (Hyper DRAM)	t_{CHEL}	CLK, EOP0 to EOP2		—	$n/2 \times t_{CYC}$	ns	
	t_{CHEH}	CLK, EOP0 to EOP2		—	6	ns	

t_{CYC} (a cycle time of peripheral system clock): Refer to "(2) Clock Output Timing."
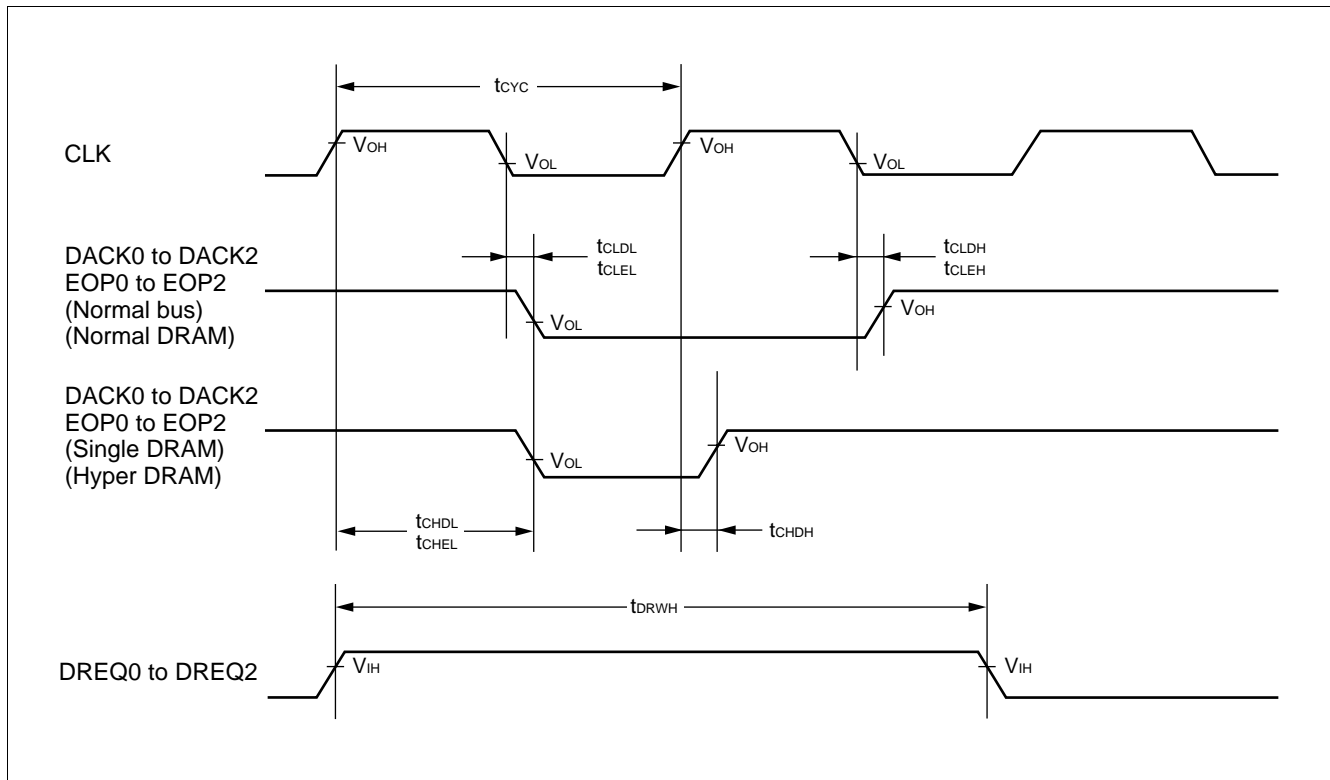
5. A/D Converter Block Electrical Characteristics

(AV$_{CC}$ = 2.7 V to 3.6 V, AV$_{SS}$ = 0.0 V, AVRH = 2.7 V, T$_A$ = –40°C to +70°C)

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Resolution	—	—	—	10	10	bit
Total error	—	—	—	—	±4.0	LSB
Linearity error	—	—	—	—	±3.5	LSB
Differentiation linearity error	—	—	—	—	±2.0	LSB
Zero transition voltage	V$_{OT}$	AN0 to AN3	−1.5	+0.5	+2.5	LSB
Full-scale transition voltage	V$_{FST}$	AN0 to AN3	AVRH – 4.5	AVRH – 1.5	AVRH + 0.5	LSB
Conversion time	—	—	5.6 [*1]	—	—	µs
Analog port input current	I$_{AIN}$	AN0 to AN3	—	0.1	10	µA
Analog input voltage	V$_{AIN}$	AN0 to AN3	AV$_{SS}$	—	AVRH	V
Reference voltage	—	AVRH	AV$_{SS}$	—	AV$_{CC}$	V
Power supply current	I$_A$	AV$_{CC}$	—	4	—	mA
	I$_{AH}$	AV$_{CC}$	—	—	5 [*2]	µA
Reference voltage supply current	I$_R$	AVRH	—	200	—	µA
	I$_{RH}$	AVRH	—	—	5 [*2]	µA
Conversion variance between channels	—	AN0 to AN3	—	—	4	LSB

*1: AV$_{CC}$ = 2.7 V to 3.6 V

*2 Current value for A/D converters not in operation, CPU stop mode (V$_{CC}$ = AV$_{CC}$ = AVRH = 3.6 V)

Notes: • As the absolute value of AVRH decreases, relative error increases.
 • Output impedance of external circuit of analog input under following conditions;
  Output impedance of external circuit < 10 kΩ.
  If output impedance of external circuit is too high, analog voltage sampling time may be too short for accurate sampling (sampling time is 5.6 µs for a machine clock of 25 MHz).

• **Analog input circuit**

Analog input

⇨Sample and hold circuit

R$_{ON1}$ R$_{ON2}$ R$_{ON3}$ R$_{ON4}$

C$_0$

C$_1$

Comparator

R$_{ON1}$: 0.2 kΩ
R$_{ON2}$: 1.4 kΩ
R$_{ON3}$: 1.4 kΩ   C$_0$: 16.6 pF
R$_{ON4}$: 0.2 kΩ   C$_1$: 4.0 pF
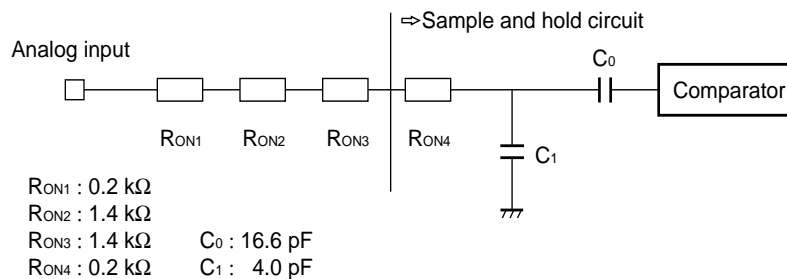
Note: Listed values are for reference purposes only.

6. A/D Converter Glossary

- Resolution
  The smallest change in analog voltage detected by A/D converter.
- Linearity error
  A deviation of actual conversion characteristic from a line connecting the zero-traction point (between "00 0000 0000" $\leftrightarrow$ "00 0000 0001") to the full-scale transition point (between "11 1111 1110" $\leftrightarrow$ "11 1111 1111").
- Differential linearity error
  A deviation of a step voltage for changing the LSB of output code from ideal input voltage.
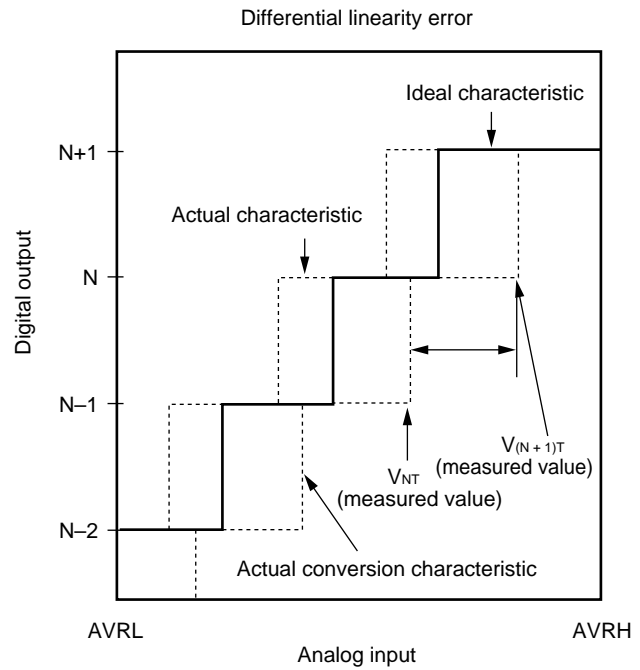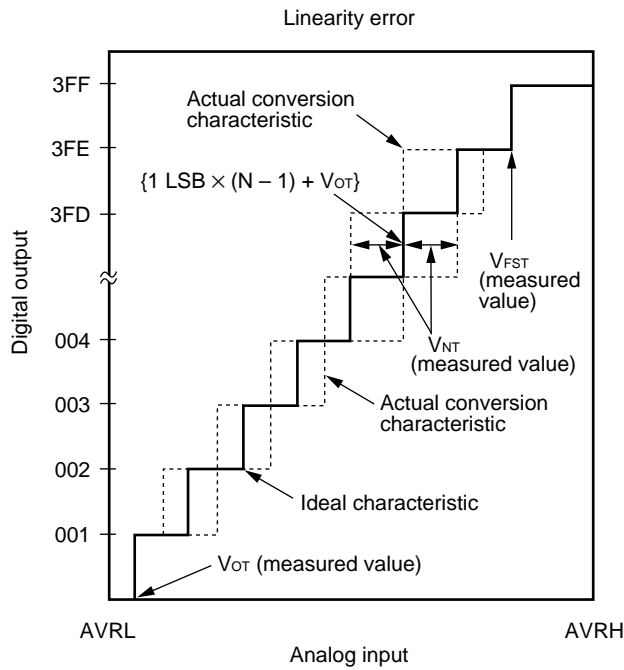
$$\text{Linearity error of digital output N} \quad = \quad \frac{V_{NT} - \{1\ LSB \times (N - 1) + V_{OT}\}}{1\ LSB} \quad [LSB]$$

$$\text{Differential linearity error of digital output N} \quad = \quad \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} \ - 1 \ \ [LSB]$$

$$1\ LSB \ = \ \frac{V_{FST} - V_{OT}}{1022} \quad [V]$$

V_{OT}: A voltage for causing transition of digital output from $(000)_H$ to $(001)_H$

V_{FST}: A voltage for causing transition of digital output from $(3FE)_H$ to $(3FF)_H$

V_{NT}: A voltage for causing transition of digital output from $(N - 1)$ to N

- Total error
  A difference between actual value and theoretical value. The overall error includes zero-transition error, full-scale transition error and linearity error.

Total error

3FF

1.5 LSB'

3FE

Actual conversion
characteristic

3FD

{1 LSB' × (N – 1)
+ 0.5 LSB'}

Digital output

004

V_{NT}
(measured value)

003

Actual conversion
characteristic

002

001

Ideal characteristic

0.5 LSB'

AVRL   AVRH

Analog input
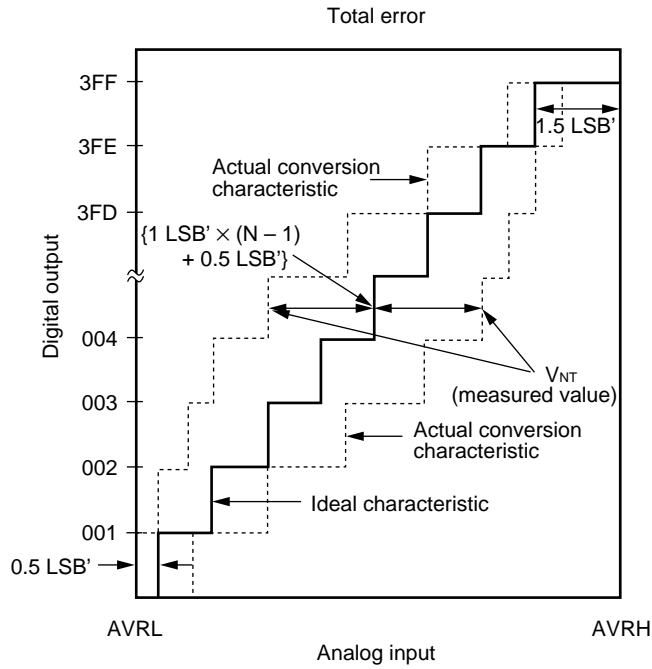
$$\text{Total error of digital output N} \quad = \quad \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'} \quad [LSB]$$

$$1\ LSB'\ (\text{ideal value}) \ = \ \frac{AVRH - AVRL}{1024} \ [V]$$

$$V_{OT}' \quad (\text{ideal value}) = \ AVRL + 0.5\ LSB'\ [V]$$

$$V_{FST}' \quad (\text{ideal value}) = \ AVRL - 1.5\ LSB'\ [V]$$

V_{NT}: A voltage for causing transition of digital output from (N – 1) to N

■ REFERENCE DATA

(1) Operating frequency vs. Icc characteristics

Internal DC - DC regulator is not used (Vcc5 = Vcc3 = 3 V)

Internal DC - DC regulator is used (Vcc5 = 5 V)

(Vcc)
3.6 V
3.3 V
3.0 V
2.7 V

(Vcc)
4.5 V to 5.5 V

Icc (mA)

f (MHz)

Operating conditions : Source oscillation 12.5 MHz (crystal), PLL is used (50 MHz, 25 MHz, 12.5 MHz)
Gear : CPU = 1/1, Peripherals = 1/1
(Doubler is used for 50MHz, Gear peripherals = 1/2)

(2) Vcc vs. Icc characteristics

Internal DC - DC regulator is not used (Vcc5 = Vcc3 = 3 V)

Internal DC - DC regulator is used (Vcc5= 5 V)

Icc (mA)

Gear : 1/1
Gear : 1/2
Gear : 1/4
Gear : 1/8
Gear : 1/8
(PLL : off)

Vcc (V)

Operating conditions : Source oscillation 12.5 MHz (crystal), divide-by-2 input, PLL : ON
Gear : CPU = Peripherals

95

■ **ORDERING INFORMATION**

Part number	Package	Remarks
MB91101APFV	100-pin Plastic LQFP (FPT-100P-M05)	
MB91101APF	100-pin Plastic QFP (FPT-100P-M06)	

■ PACKAGE DIMENSIONS

100-pin Plastic LQFP
(FPT-100P-M05)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

16.00±0.20(.630±.008)SQ

*14.00±0.10(.551±.004)SQ

INDEX

0.50(.020)

0.20±0.05
(.008±.002)

⊕ 0.08(.003) Ⓜ

0.08(.003)

"A"

0.145±0.055
(.0057±.0022)

Details of "A" part

$1.50^{+0.20}_{-0.10}$ ($.059^{+.008}_{-.004}$)
(Mounting height)

0°~8°

0.50±0.20
(.020±.008)

0.60±0.15
(.024±.006)

0.10±0.10
(.004±.004)
(Stand off)

0.25(.010)
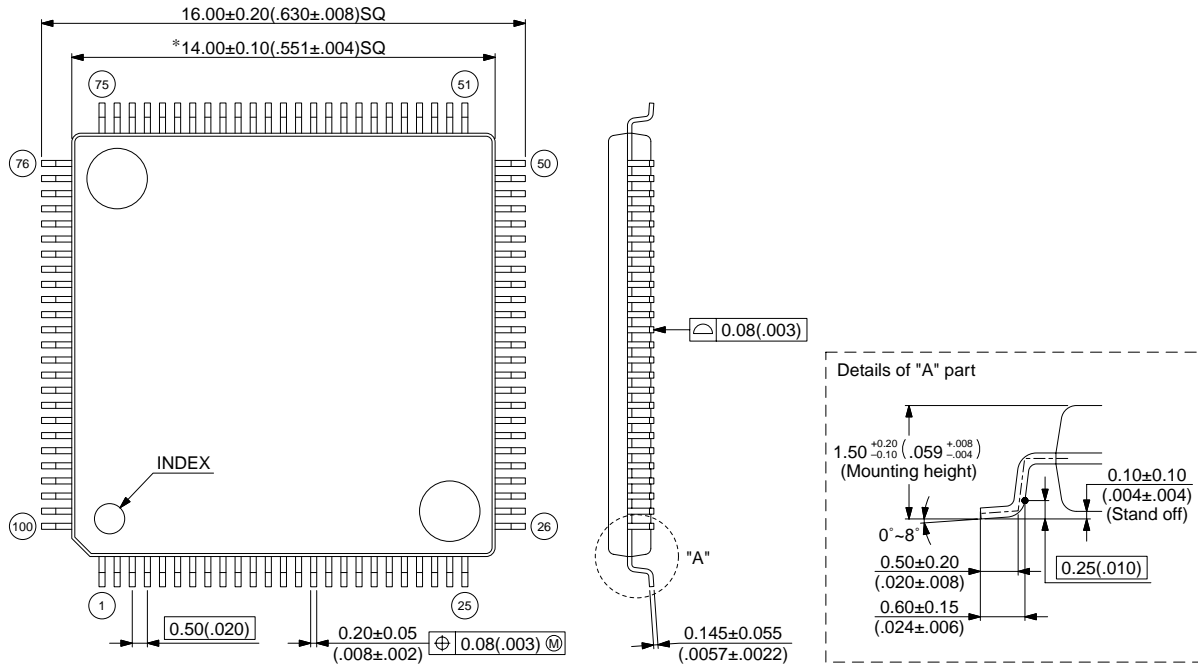
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Dimensions in mm (inches)
Note : The values in parentheses are reference values.

(Continued)

(Continued)

100-pin Plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

23.90±0.40(.941±.016)

*20.00±0.20(.787±.008)

80   51

81   50

100   31

1   30

INDEX

"A"

17.90±0.40
(.705±.016)

*14.00±0.20
(.551±.008)

0.65(.026)

0.32±0.05
(.013±.002)

$\oplus$ 0.13(.005) Ⓜ

0.10(.004)

0.17±0.06
(.007±.002)

Details of "A" part

$3.00^{+0.35}_{-0.20}$
$(.118^{+.014}_{-.008})$
(Mounting height)

0.25(.010)

0~8°

0.80±0.20
(.031±.008)

0.88±0.15
(.035±.006)

0.25±0.20
(.010±.008)
(Stand off)
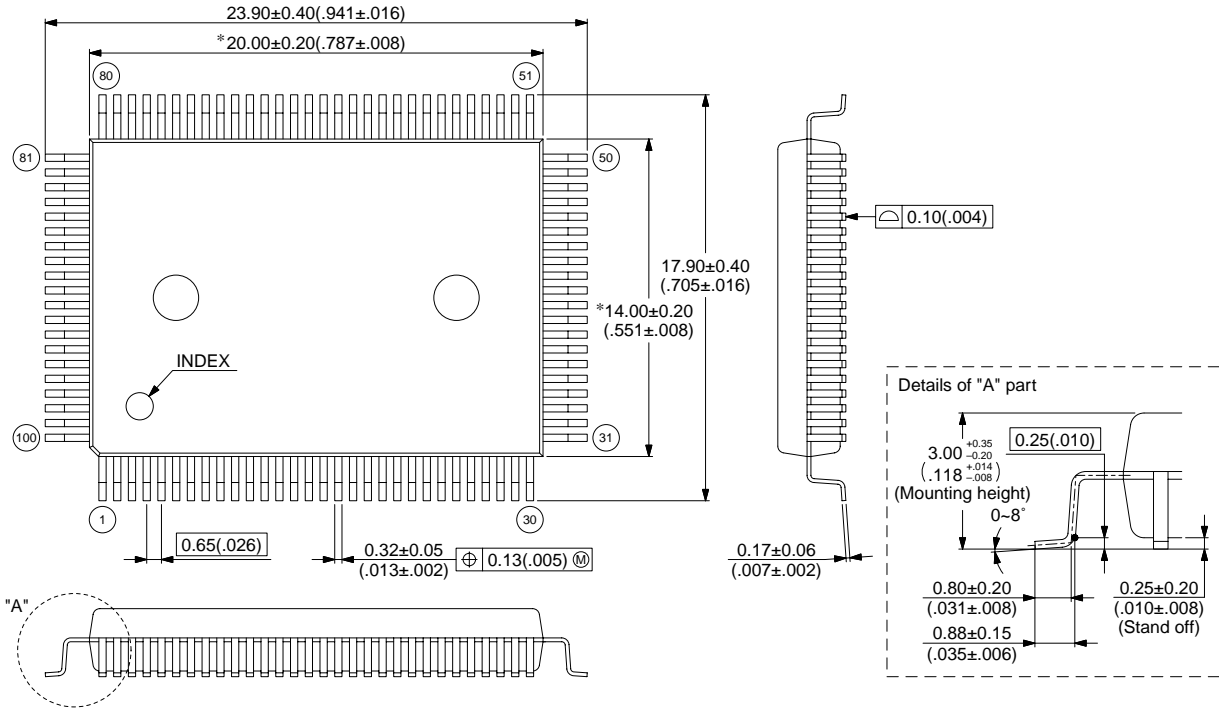
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Dimensions in mm (inches)
Note : The values in parentheses are reference values.

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