*16-bit Proprietary Microcontroller*

**CMOS**

# F²MC-16LX MB90495 Series

# MB90497/F497

## 1. OUTLINE

The MB90495-series with FULL-CAN interface and FLASH ROM is especially designed for automotive and industrial applications. Its main feature is the on-chip CAN Interface, which conforms to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme, including 8 message buffers, and so offering more functions than a normal full CAN approach.

With the new 0.5 mm CMOS technology, Fujitsu now also offers on-chip FLASH-ROM program memory. An internal voltage booster removes the necessity for a second programming voltage. An on-chip voltage regulator provides 3V to the internal MCU core. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 62.5 nsec instruction cycle time from an external 4 MHz clock. A 32kHz Subsystem clock has been included for power saving modes and real time measurement.

There are 2 on-chip UART's, which also provide synchronous communication modes. Furthermore the MCU features an 8 channel ADC, 8 channel External interrupt controller, two 16 bit PPG channels, 4 channel Input Capture Unit and a 16-bit free running I/O-timer.

## 2. FEATURES

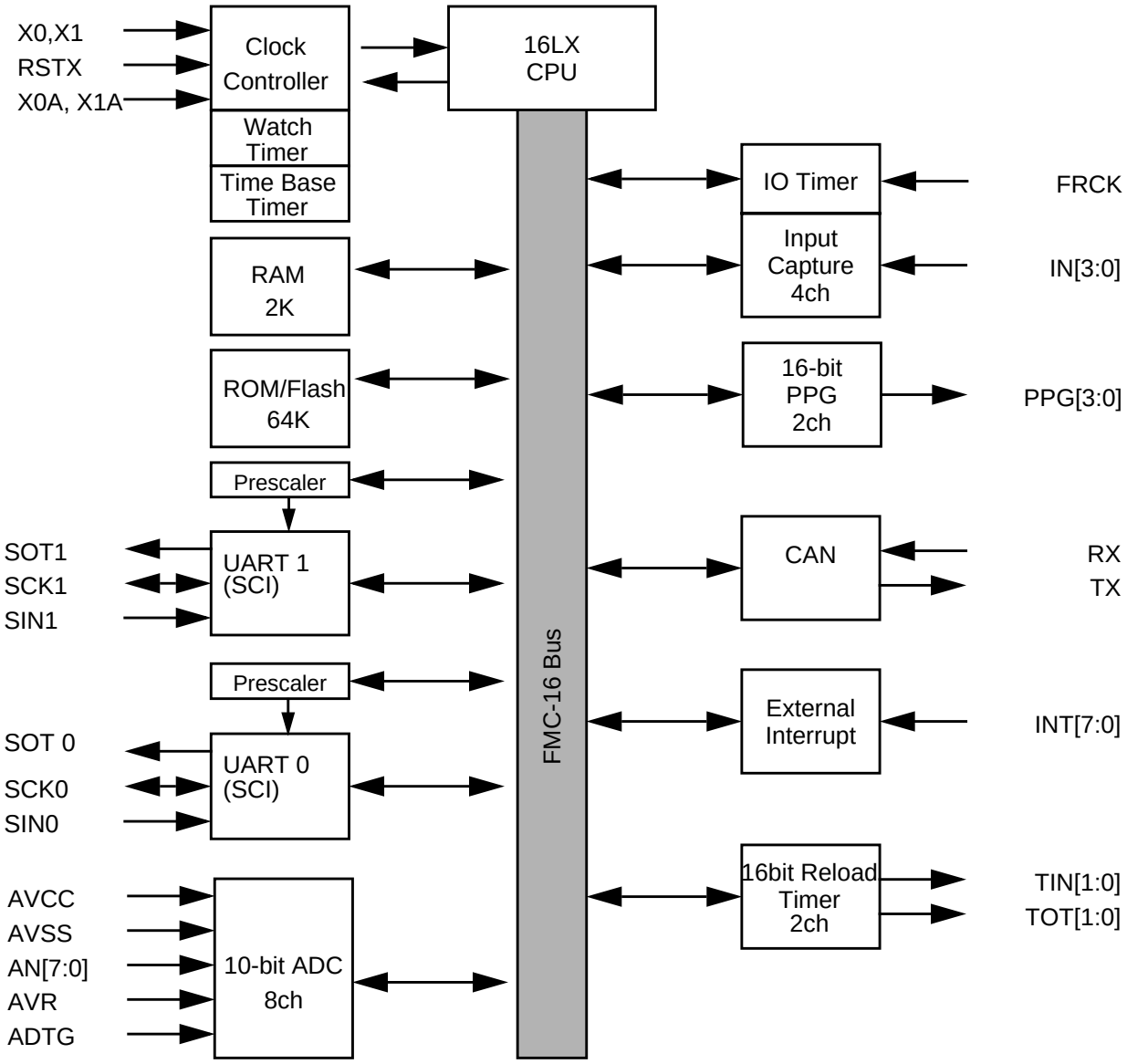
- 16-bit core CPU; 4MHz external clock (16 MHz internal, 62.5 ns instruction cycle time)
- 32kHz Subsystem Clock
- 0.5 mm CMOS Technology
- Internal voltage regulator supports 3V MCU core, offering low EMI and low power consumption figures
- 64 KB FLASH ROM; supports automatic programming, 10.000 erase cycles, 10 year data retention time and no second programming voltage required
- 2 KB static RAM
- FULL-CAN interface; conforming to Version 2.0 Part A and Part B, flexible message buffering (mailbox and FIFO buffering can be mixed)
- 2 UART's; both offering synchronous communication modes.
- Powerful interrupt functions (8 programmable priority levels; 8 external interrupts)
- I/O Timer
- A/D Converter: 8 channel analogue inputs (Resolution 10 bits or 8 bits)
- ICU (Input capture) 16bit * 4ch
- PPG (Programmable Pulse Generator) 16bit * 2ch; Can be configured as 8bit * 4ch
- Optimised instruction set for controller applications
  (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
- 4-byte instruction execution queue
- Signed multiply (16bit*16bit) and divide (32bit/16bit) instructions available
- Program Patch Function
- Fast Interrupt processing
- 16-bit reload timer: 2 channels
- Low Power Consumption - Several different Lo-Power modes: (Sleep, Stop, Watch,...)
- Package: QFP-64; 12mm x 12mm body, 0.65mm pin pitch
- QFP-64; 20mm x 18mm body, 1.0mm pin pitch

## 3. PRODUCT LINEUP

The following table provides an overview of the MB90495 Series

| Features | MB90F497 | MB90497 |
|---|---|---|
| CPU | F2MC-16LX CPU | |
| System clock | On-chip PLL clock multiplier (x1, x2, x3, x4, 1/2 when PLL stop)<br>Minimum instruction execution time: 62.5 ns (4 MHz osc. PLL x4) | |
| ROM | Boot-block<br>Flash memory 64 Kbytes | Mask ROM 64 Kbytes |
| RAM | 2 Kbytes | 2 Kbytes |
| Technology | 0.5 mm CMOS with on-chip voltage regulator for internal power supply + Flash memory On-chip charge pump for programming voltage | 0.5 mm CMOS with on-chip voltage regulator for internal power supply |
| Operating voltage range | 5 V +/- 10% | |
| Temperature range | - 40 to 85 °C | |
| Package | QFP64 | |

## 4. BLOCK DIAGRAM



## 5. PIN ASSIGNMENT

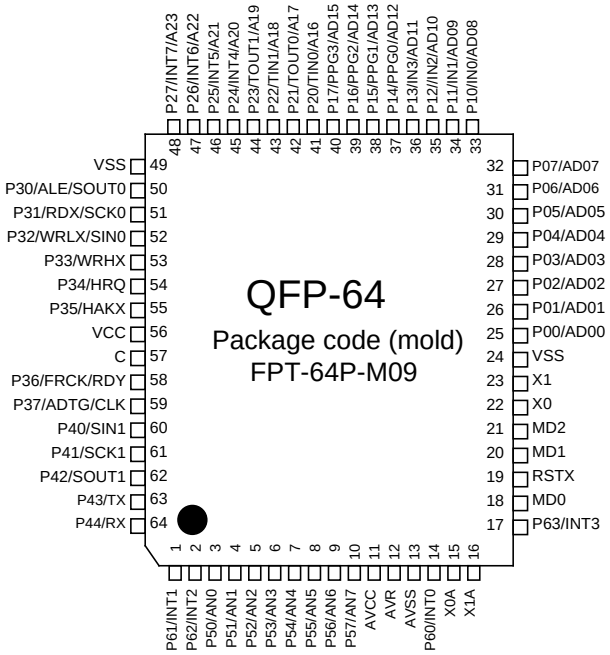



**Figure 5.1 FPT-64P-M09**

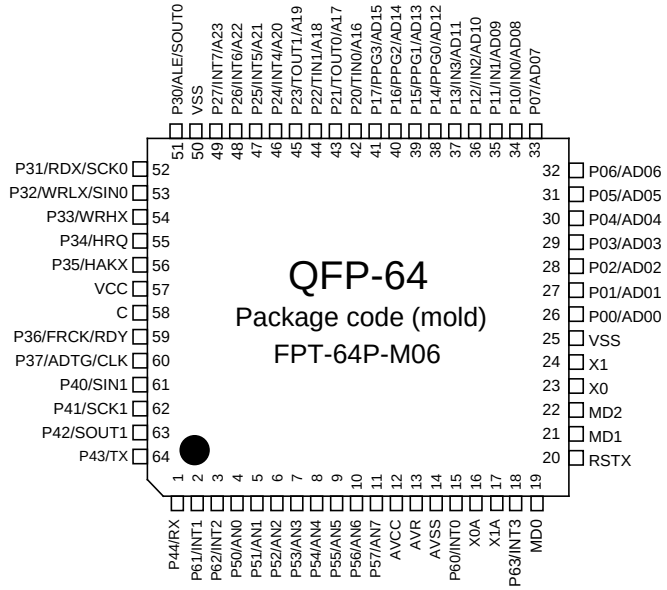



**Figure 5.2 FPT-64P-M06**

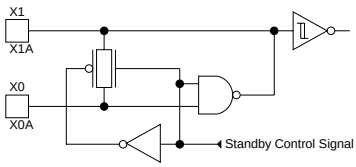
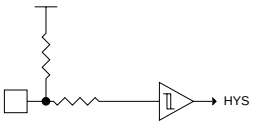
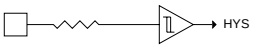
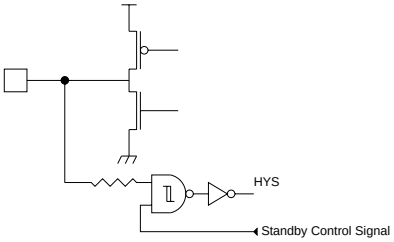
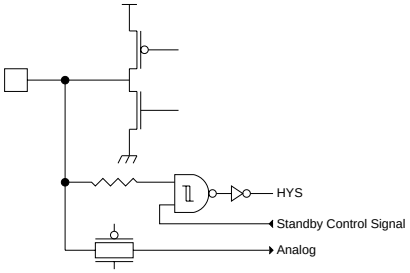
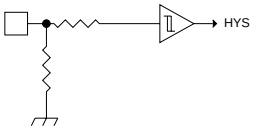
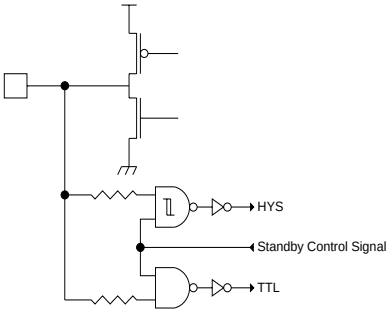
## 6. PIN DESCRIPTION

## 6.1 Pin Function

| Pin No. | | Pin Name | Circuit Type | Active | Level | at RST | Priority | Function |
|---|---|---|---|---|---|---|---|---|
| M06 | M09 | | | | | | | |
| 2 | 1 | P61 | D | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | INT1 | | | | | | External Interrupt input 1 |
| 3 | 2 | P62 | D | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | INT2 | | | | | | External interrupt 2 |
| 4 to 11 | 3 to 10 | P50 to P57 | E | H | CMOS | High-Z | Port | General pupose IO |
| | | AN0 to AN7 | | | | | | Inputs for A/D Converter |
| 12 | 11 | AVCC | | | | | | Dedicated power supply for A/D Converter |
| 13 | 12 | AVR | | | | | | Reference Volgate inupt for A/D Converter |
| 14 | 13 | AVSS | | | | | | Dedicated power ground for A/D Converter |
| 15 | 14 | P60 | D | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | INT0 | | | | | | External interrupt input 0 |
| 16 | 15 | X0A | A | | | | | Low frequency oscillation input |
| 17 | 16 | X1A | A | | | | | Low frequency oscillation output |
| 18 | 17 | P63 | D | H | CMOS/ TTL | High-Z | Port | General purpose IO |
| | | INT3 | | | | | | External interrupt 3 |
| 19 | 18 | MD0 | C | H | CMOS | | | Mode input |
| 20 | 19 | RSTX | B | L | CMOS | | | Reset input |
| 21 | 20 | MD1 | C | H | CMOS | | | Mode input |
| 22 | 21 | MD2 | F | H | CMOS | | | Mode input |
| 23 | 22 | X0 | A | | | | | High frequency oscillation input |
| 24 | 23 | X1 | A | | | | | High frequency oscillation output |
| 25 | 24 | VSS | | | | | | Power ground |
| 26 to 33 | 25 to 32 | P00 to P07 | G | H | CMOS/ TTL | High-Z | Port | General purpose IO |
| | | AD00 to AD07 | | | | | | Addresss Data Bus |
| 34 to 37 | 33 to 36 | P10 to P13 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | IN0 to IN3 | | | | | | Inputs for Input Captures |
| | | AD08 to AD11 | | | | | | Address Data Bus |
| 38 to 41 | 37 to 40 | P14 to P17 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | PPG0 to PPG3 | | | | | | Outputs for Programable Pulse Generators |
| | | AD12 to AD15 | | | | | | Address Data Bus |
| 42 | 41 | P20 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | TIN0 | | | | | | Input for 16-bit Reload Timer 0 |
| | | A16 | | | | | | Address Bus |
| 43 | 42 | P21 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | TOT0 | | | | | | Output for 16-bit Reload Timer 0 |
| | | A17 | | | | | | Address Bus |
| 44 | 43 | P22 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | TIN1 | | | | | | Input for 16-bit Reload Timer 1 |
| | | A18 | | | | | | Address Bus |

| Pin No. | | Pin Name | Circuit Type | Active | Level | at RST | Priority | Function |
|---|---|---|---|---|---|---|---|---|
| M06 | M09 | | | | | | | |
| 45 | 44 | P23 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | TOT1 | | | | | | Output for 16-bit Reload Timer 1 |
| | | A19 | | | | | | Address Bus |
| 46 to 49 | 45 to 48 | P24 to P25 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | INT4 to INT 7 | | | | | | Inputs for External Interrupt |
| | | A20 to A23 | | | | | | Address Bus |
| 50 | 49 | VSS | | | | | | Ground |
| 51 | 50 | P30 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | SOT0 | | | | | | Output for UART 0 |
| | | ALE | | | | | | Address Latch Enable output |
| 52 | 51 | P31 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | SCK0 | | | | | | Input/Output for UART 0 |
| | | RDX | | | | | | Read Enable output |
| 53 | 52 | P32 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | SIN0 | | | | | | Input for UART 0 |
| | | WRLX | | | | | | Write Enable Low-byte output |
| 54 | 53 | P33 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | WRHX | | | | | | Write Enable High-byte output |
| 55 | 54 | P34 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | HRQ | | | | | | Halt Request input |
| 56 | 55 | P35 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | HAKX | | | | | | Halt Acknowledge output |
| 57 | 56 | VCC | | | | | | Power supply |
| 58 | 57 | C | | | | | | Pin for capacitor for the internal power supply. |
| 59 | 58 | P36 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | FRCK | | | | | | Inupt for IO Timer |
| | | RDY | | | | | | Ready input |
| 60 | 59 | P37 | D | H | CMOS | High-Z | Port | General pupose IO |
| | | ADTG | | | | | | Trigger inupt for A/D Converter |
| | | CLK | | | | | | Clock output |
| 61 | 60 | P40 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | SIN1 | | | | | | Input for UART 1 |
| 62 | 61 | P41 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | SCK1 | | | | | | Input/Output for UART 1 |
| 63 | 62 | P42 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | SOT1 | | | | | | Output for UART 1 |
| 64 | 63 | P43 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | Tx | | | | | | CAN Transmit pin |
| 1 | 64 | P44 | G | H | CMOS/ TTL | High-Z | Port | General pupose IO |
| | | Rx | | | | | | CAN receive pin |

## 6.2 I/O Circuit Types

| Circuit | Drawing | Comment |
|---|---|---|
| A |  | |
| B |  | |
| C |  | |
| D |  | |
| E |  | |
| F |  | |
| G |  | |

## 7. HANDLING DEVICES

(1) Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions:

A voltage higher than Vcc or lower than Vss is applied to an input or output pin.

A voltage higher than the rated voltage is applied between Vcc and Vss.

The AVcc power supply is applied before the Vcc voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

(2) Handling unused input pins

Do not leave unused input pins open, as doing so may cause misoperation of the device. Use a pull-up or pull-down resistor.

(3) Using external clock

To use external clock, drive the X0 and X1 pins in reverse phase.

Below is a diagram of how to use external clock.

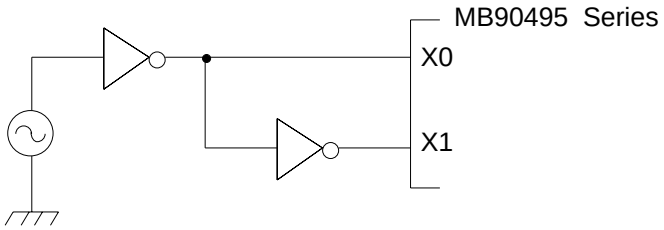



**Figure 7.1 Using external clock**

(4) Power supply pins (Vcc/Vss)

Ensure that all Vcc-level power supply pins are at the same potential. In addition, ensure the same for all Vss-level power supply pins. (See the figure below.) If there are more than one Vcc or Vss system, the device may operate incorrectly even within the guaranteed operating range. Note that this product may not have as many power pins as pictured in the figure.

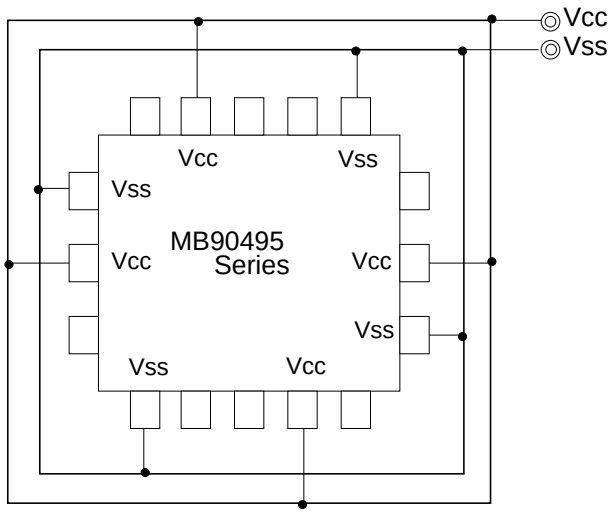
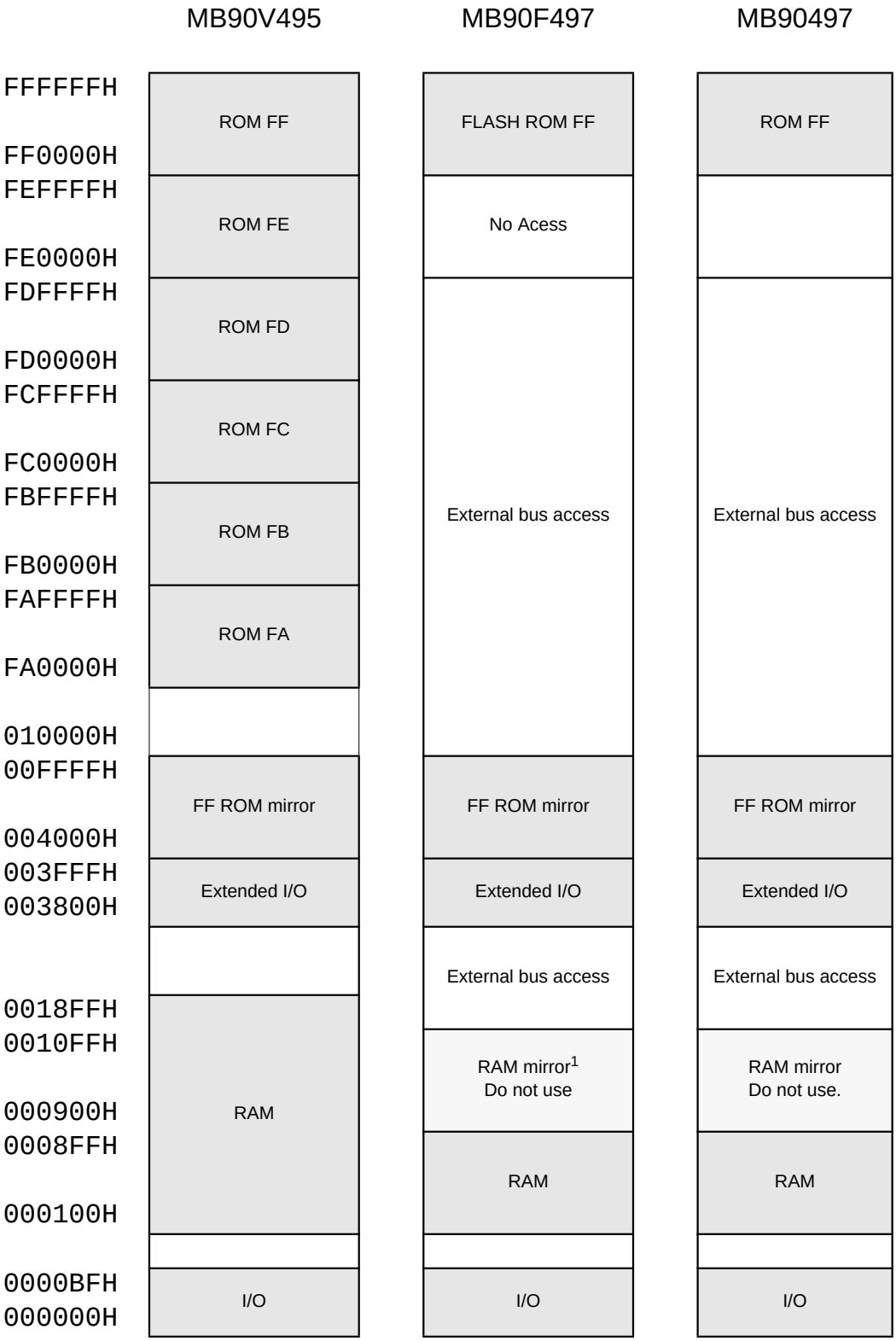



**Figure 7.2 Power pin connections**

(5) Pull-up/down resistors

The MB90495 Series does not support internal pull-up/down resistors. Use external components where needed.

## 8. ADDRESS SPACE




1. The RAM contents of $0000_H$ - $08FF_H$ is mirrored to $0900_H$ - $10FF_H$. The RAM mirror area should not be accessed for proper operation.

## 9. REGISTER MAP

| Address | Register | Abbreviation | Peripheral | Access | Initial value |
|---|---|---|---|---|---|
| 00 H | Port 0 data register | PDR0 | Port 0 | R/W | XXXXXXXX |
| 01 H | Port 1 data register | PDR1 | Port 1 | R/W | XXXXXXXX |
| 02 H | Port 2 data register | PDR2 | Port 2 | R/W | XXXXXXXX |
| 03 H | Port 3 data register | PDR3 | Port 3 | R/W | XXXXXXXX |
| 04 H | Port 4 data register | PDR4 | Port 4 | R/W | XXXXXXXX |
| 05 H | Port 5 data register | PDR5 | Port 5 | R/W | XXXXXXXX |
| 06 H | Port 6 data register | PDR6 | Port 6 | R/W | XXXXXXXX |
| 07-0F H | Reserved | | | | |
| 10 H | Port 0 direction register | DDR0 | Port 0 | R/W | 00000000 |
| 11 H | Port 1 direction register | DDR1 | Port 1 | R/W | 00000000 |
| 12 H | Port 2 direction register | DDR2 | Port 2 | R/W | 00000000 |
| 13 H | Port 3 direction register | DDR3 | Port 3 | R/W | 00000000 |
| 14 H | Port 4 direction register | DDR4 | Port 4 | R/W | 00000000 |
| 15 H | Port 5 direction register | DDR5 | Port 5 | R/W | 00000000 |
| 16 H | Port 6 direction register | DDR6 | Port 6 | R/W | 00000000 |
| 17-1A H | Reserved | | | | |
| 1B H | Analog Input Enable | ADER | Port 5, A/D | R/W | 11111111 |
| 1C - 1F H | Reserved | | | | |
| 20 H | Serial Mode Register 1 | SMR0 | UART0 | R/W | 00000000 |
| 21 H | Serial Control Register 1 | SCR0 | | R/W | 00000100 |
| 22 H | Input/Output Data Register 1 | SIDR0/SODR0 | | R/W | XXXXXXXX |
| 23 H | Serial Status Register 1 | SSR0 | | R/W | 00001_00 |
| 24 H | UART 0 Prescaler Control Register | CDCR0 | | R/W | 0___1111 |
| 25 H | UART 0 edge select | SES0 | | R/W | _____1 |
| 26 H | Serial Mode Control Register 1 | SMC1 | UART1 | R/W | 00XXXX00 |
| 27 H | Serial Control Register | SRC1 | | R/W | 00000X00 |
| 28 H | Input/Output Data Register 1 | SIDR1/SODR1 | | R/W | XXXXXXXX |
| 29 H | Serial Status Register 1 | SMC1 | | R/W | XXXXX000 |
| 2A H | Reserved | | | | |
| 2B H | UART 1 Prescaler Control Register | CDCR0 | Prescaler UART 1 | R/W | 0___0000 |
| 2C - 2F H | Reserved | | | | |
| 30 H | External Interrupt Enable | ENIR | External Interrupt | R/W | 00000000 |
| 31 H | External Interrupt Request | EIRR | | R/W | XXXXXXXX |
| 32 H | External Interrupt Level | ELVR | | R/W | 00000000 |
| 33 H | External Interrupt Level | ELVR | | R/W | 00000000 |
| 34 H | A/D Control Status 0 | ADCS0 | A/D Converter | R/W | 00000000 |
| 34 H | A/D Control Status 1 | ADCS1 | | R/W | 00000100 |
| 36 H | A/D Data 0 | ADCR0 | | R | XXXXXXXX |
| 37 H | A/D Data 1 | ADCR1 | | R/W | 00000_XX |
| 38-3FH | Reserved | | | | |
| 40 H | PPG0 operation mode control register | PPGC0 | 16-bit Programable Pulse Generator 0/1 | R/W | 0_00X__1 |
| 41 H | PPG1 operation mode control register | PPGC1 | | R/W | 0_00X001 |
| 42 H | PPG0 and PPG1 clock select register | PPG01 | | R/W | 000000__ |

| Address | Register | Abbreviation | Peripheral | Access | Initial value |
|---|---|---|---|---|---|
| 43 H | Reserved | | | | |
| 44 H | PPG2 operation mode control register | PPGC2 | 16-bit Programable Pulse Generator 2/3 | R/W | 0_00X__1 |
| 45 H | PPG3 operation mode control register | PPGC3 | | R/W | 0_00X001 |
| 46 H | PPG2 and PPG3 clock select register | PPG23 | | R/W | 000000__ |
| 47-4FH | Reserved | | | | |
| 50 H | Input Capture 0 | IPCP0 | Input Captue 0/1 | R | XXXXXXXX |
| 51 H | Input Capture 0 | IPCP0 | | R | XXXXXXXX |
| 52 H | Input Capture 1 | IPCP1 | | R | XXXXXXXX |
| 53 H | Input Capture 1 | IPCP1 | | R | XXXXXXXX |
| 54 H | Input Capture Control Status 0/1 | ICS01 | Input Capture 0/1/2/3 | R/W | XX000000 |
| 55 H | Input Capture Control Status 2/3 | ICS23 | | R/W | XX000000 |
| 56 H | Timer Data | TCDT | I/O Timer | R/W | 00000000 |
| 57 H | Timer Data | TCDT | | R/W | 00000000 |
| 58 H | Timer Control | TCCS | | R/W | 00000000 |
| 59 H | Timer Control | TCCS | | R/W | 0__00000 |
| 5A H | Input Capture 2 | IPCP2 | Input Captue 2/3 | R | XXXXXXXX |
| 5B H | Input Capture 2 | IPCP2 | | R | XXXXXXXX |
| 5C H | Input Capture 3 | IPCP3 | | R | XXXXXXXX |
| 5D H | Input Capture 3 | IPCP3 | | R | XXXXXXXX |
| 5E - 65 H | Reserved | | | | |
| 66 H | Timer Control Status 0 | TMCSR0 | 16-bit Reload Timer 0 | R/W | 00000X00 |
| 67 H | Timer Control Status 0 | TMCSR0 | | R/W | ____0000 |
| 68 H | Timer Control Status 1 | TMCSR1 | 16-bit Reload Timer 1 | R/W | 00000X00 |
| 69 H | Timer Control Status 1 | TMCSR1 | | R/W | ____0000 |
| 6A - 6E H | Reserved | | | | |
| 6F H | ROM Mirror | ROMM | ROM Mirror | R/W | 000____1 |
| 70-7F H | Reserved | | | | |
| 80-8F H | Reserved for CAN 1 Interface . Refer to “CAN Controller” | | | | |
| 90-9D H | Reserved | | | | |
| 9E H | ROM Correction Control Status | PACSR | ROM Correction | R/W | 11000000 |
| 9F H | Delayed Interrupt/release | DIRR | Delayed Interrupt | R/W | _______0 |
| A0 H | Low-power Mode | LPMCR | Low Power Controller | R/W | 00011000 |
| A1 H | Clock Selector | CKSCR | Low Power Controller | R/W | 11111100 |
| A2-A4 H | Reserved | | | | |
| A5 H | Automatic ready function select reg. | ARSR | W | External Memory Access | 0011__00 |
| A6 H | External address output control reg. | HACR | W | | 00000000 |
| A7 H | Bus control signal select register | ECSR | W | | 0000000_ |
| A8 H | Watchdog Control | WDTC | Watchdog Timer | R/W | XXXXX111 |
| A9 H | Time Base Timer Control | TBTC | Time Base Timer | R/W | 1__0X100 |
| AA-AD H | Reserved | | | | |
| AE H | Flash Control Status (Flash only, otherwise reserved) | FMCS | Flash Memory | R/W | 000X0000 |
| AF H | Reserved | | | | |

| Address | Register | Abbreviation | Peripheral | Access | Initial value |
|---|---|---|---|---|---|
| B0 H | Interrupt control register 00 | ICR00 | Interrupt controller | R/W | 11000111 |
| B1 H | Interrupt control register 01 | ICR01 | | R/W | 11000111 |
| B2 H | Interrupt control register 02 | ICR02 | | R/W | 11000111 |
| B3 H | Interrupt control register 03 | ICR03 | | R/W | 11000111 |
| B4 H | Interrupt control register 04 | ICR04 | | R/W | 11000111 |
| B5 H | Interrupt control register 05 | ICR05 | | R/W | 11000111 |
| B6 H | Interrupt control register 06 | ICR06 | | R/W | 11000111 |
| B7 H | Interrupt control register 07 | ICR07 | | R/W | 11000111 |
| B8 H | Interrupt control register 08 | ICR08 | | R/W | 11000111 |
| B9 H | Interrupt control register 09 | ICR09 | | R/W | 11000111 |
| BA H | Interrupt control register 10 | ICR10 | | R/W | 11000111 |
| BB H | Interrupt control register 11 | ICR11 | | R/W | 11000111 |
| BC H | Interrupt control register 12 | ICR12 | | R/W | 11000111 |
| BD H | Interrupt control register 13 | ICR13 | | R/W | 11000111 |
| BE H | Interrupt control register 14 | ICR14 | | R/W | 11000111 |
| BF H | Interrupt control register 15 | ICR15 | | R/W | 11000111 |
| CO-FF H | Reserved | | | | |
| 1FF0H-1FF5H | ROM correction | | | | |
| 3900 H | Timer 0/Reload 0 | TMR0/TMRL0 | 16-bit Reload Timer 0 | R/W | XXXXXXXX |
| 3901 H | Timer 0/Reload 0 | TMR0/TMRL0 | | R/W | XXXXXXXX |
| 3902 H | Timer 1/Reload 1 | TMR1/TMRL1 | 16-bit Reload Timer 1 | R/W | XXXXXXXX |
| 3903 H | Timer 1/Reload 1 | TMR1/TMRL1 | | R/W | XXXXXXXX |
| 3904-390FH | Reserved | | | | |
| 3910 H | PPG0 Reload L | PRLL0 | 16-bit Programable Pulse Generator 0/1 | R/W | XXXXXXXX |
| 3911 H | PPG0 Reload H | PRLH0 | | R/W | XXXXXXXX |
| 3912 H | PPG1 Reload L | PRLL1 | | R/W | XXXXXXXX |
| 3913 H | PPG1 Reload H | PRLH1 | | R/W | XXXXXXXX |
| 3914 H | PPG2 Reload L | PRLL2 | 16-bit Programable Pulse Generator 2/3 | R/W | XXXXXXXX |
| 3915 H | PPG2 Reload H | PRLH2 | | R/W | XXXXXXXX |
| 3916 H | PPG3 Reload L | PRLL3 | | R/W | XXXXXXXX |
| 3917 H | PPG3 Reload H | PRLH3 | | R/W | XXXXXXXX |
| 3918-392FH | Reserved | | | | |
| 3930-3BFFH | Reserved | | | | |
| 3C00-3CFFH | Reserved for CAN 1 Interface. Refer to “CAN Controller” | | | | |
| 3D00-3DFFH | Reserved for CAN 1 Interface. Refer to “CAN Controller” | | | | |
| 3E00-3EFFH | Reserved | | | | |
| 3FF0-3FFFH | Reserved | | | | |

## 10. CAN CONTROLLER

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 8 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as 1D acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbits/s to 2 Mbits/s (when input clock is at 16 MHz)

## 10.1 List of Control Registers

| Address | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 000080H | Message buffer valid register | BVALR | R/W | 00000000 |
| 000081H | Unused | | | |
| 000082H | Transmit request register | TREQR | R/W | 00000000 |
| 000083H | Unused | | | |
| 000084H | Transmit cancel register | TCANR | W | 00000000 |
| 000085H | Unused | | | |
| 000086H | Transmit complete register | TCR | R/W | 00000000 |
| 000087H | Unused | | | |
| 000088H | Receive complete register | RCR | R/W | 00000000 |
| 000089H | Unused | | | |
| 00008AH | Remote request receiving register | RRTRR | R/W | 00000000 |
| 00008BH | Unused | | | |
| 00008CH | Receive overrun register | ROVRR | R/W | 00000000 |
| 00008DH | Unused | | | |
| 00008EH | Receive interrupt enable register | RIER | R/W | 00000000 |
| 00008FH | Unused | | | |
| 003D00H | Control status register | CSR | R/W, R | 00---000 0----0-1 |
| 003D01H | | | | |
| 003D02H | Last event indicator register | LEIR | R/W | -------- 000-0000 |
| 003D03H | | | | |
| 003D04H | Receive/transmit error counter | RTEC | R | 00000000 00000000 |
| 003D05H | | | | |
| 003D06H | Bit timing register | BTR | R/W | -1111111 11111111 |
| 003D07H | | | | |
| 003D08H | **IDE** register | IDER | R/W | XXXXXXXX |
| 003D09H | Unused | | | |
| 003D0AH | Transmit **RTR** register | TRTRR | R/W | 00000000 |
| 003D0BH | Unused | | | |
| 003D0CH | Remote frame receive waiting register | RFWTR | R/W | XXXXXXXX |
| 003D0DH | Unused | | | |
| 003D0EH | Transmit interrupt enable register | TIER | R/W | 00000000 |
| 003D0FH | Unused | | | |
| 003D10H | Acceptance mask select register | AMSR | R/W | XXXXXXXX XXXXXXXX |
| 003D11H | | | | |
| 003D12H | Unused | | | |
| 003D13H | | | | |
| 003D14H | Acceptance mask register 0 | AMR0 | R/W | XXXXXXXX XXXXXXXX |
| 003D15H | | | | |
| 003D16H | | | | XXXXX--- XXXXXXXX |
| 003D17H | | | | |
| 003D18H | Acceptance mask register 1 | AMR1 | R/W | XXXXXXXX XXXXXXXX |
| 003D19H | | | | |
| 003D1AH | | | | XXXXX--- XXXXXXXX |
| 003D1BH | | | | |

## 10.2 List of Message Buffers (ID Registers)

| Address | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 003C00H to 003C0FH | General-purpose RAM | -- | R/W | XXXXXXXX to XXXXXXXX |
| 003C10H | **ID** register 0 | IDR0 | R/W | XXXXXXXX XXXXXXXX |
| 003C11H | | | | |
| 003C12H | | | | XXXXX--- XXXXXXXX |
| 003C13H | | | | |
| 003C14H | **ID** register 1 | IDR1 | R/W | XXXXXXXX XXXXXXXX |
| 003C15H | | | | |
| 003C16H | | | | XXXXX--- XXXXXXXX |
| 003C17H | | | | |
| 003C18H | **ID** register 2 | IDR2 | R/W | XXXXXXXX XXXXXXXX |
| 003C19H | | | | |
| 003C1AH | | | | XXXXX--- XXXXXXXX |
| 003C1BH | | | | |
| 003C1CH | **ID** register 3 | IDR3 | R/W | XXXXXXXX XXXXXXXX |
| 003C1DH | | | | |
| 003C1EH | | | | XXXXX--- XXXXXXXX |
| 003C1FH | | | | |
| 003C20H | **ID** register 4 | IDR4 | R/W | XXXXXXXX XXXXXXXX |
| 003C21H | | | | |
| 003C22H | | | | XXXXX--- XXXXXXXX |
| 003C23H | | | | |
| 003C24H | **ID** register 5 | IDR5 | R/W | XXXXXXXX XXXXXXXX |
| 003C25H | | | | |
| 003C26H | | | | XXXXX--- XXXXXXXX |
| 003C27H | | | | |
| 003C28H | **ID** register 6 | IDR6 | R/W | XXXXXXXX XXXXXXXX |
| 003C29H | | | | |
| 003C2AH | | | | XXXXX--- XXXXXXXX |
| 003C2BH | | | | |
| 003C2CH | **ID** register 7 | IDR7 | R/W | XXXXXXXX XXXXXXXX |
| 003C2DH | | | | |
| 003C2EH | | | | XXXXX--- XXXXXXXX |
| 003C2FH | | | | |

## 10.3 List of Message Buffers (DLC Registers and Data Registers)

| Address | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 003C30H<br>003C31H | **DLC** register 0 | DLCR0 | R/W | ----XXXX |
| 003C32H<br>003C33H | **DLC** register 1 | DLCR1 | R/W | ----XXXX |
| 003C34H<br>003C35H | **DLC** register 2 | DLCR2 | R/W | ----XXXX |
| 003C36H<br>003C37H | **DLC** register 3 | DLCR3 | R/W | ----XXXX |
| 003C38H<br>003C39H | **DLC** register 4 | DLCR4 | R/W | ----XXXX |
| 003C3AH<br>003C3BH | **DLC** register 5 | DLCR5 | R/W | ----XXXX |
| 003C3CH<br>003C3DH | **DLC** register 6 | DLCR6 | R/W | ----XXXX |
| 003C3EH<br>003C3FH | **DLC** register 7 | DLCR7 | R/W | ----XXXX |
| 003C40H<br>to<br>003C47H | Data register 0 (8 bytes) | DTR0 | R/W | XXXXXXXX<br>to<br>XXXXXXXX |
| 003C48H<br>to<br>003C4FH | Data register 1 (8 bytes) | DTR1 | R/W | XXXXXXXX<br>to<br>XXXXXXXX |
| 003C50H<br>to<br>003C57H | Data register 2 (8 bytes) | DTR2 | R/W | XXXXXXXX<br>to<br>XXXXXXXX |
| 003C58H<br>to<br>003C5FH | Data register 3 (8 bytes) | DTR3 | R/W | XXXXXXXX<br>to<br>XXXXXXXX |
| 003C60H<br>to<br>003C67H | Data register 4 (8 bytes) | DTR4 | R/W | XXXXXXXX<br>to<br>XXXXXXXX |
| 003C68H<br>to<br>003C6FH | Data register 5 (8 bytes) | DTR5 | R/W | XXXXXXXX<br>to<br>XXXXXXXX |
| 003C70H<br>to<br>003C77H | Data register 6 (8 bytes) | DTR6 | R/W | XXXXXXXX<br>to<br>XXXXXXXX |
| 003C78H<br>to<br>003C7FH | Data register 7 (8 bytes) | DTR7 | R/W | XXXXXXXX<br>to<br>XXXXXXXX |

## 11. INTERRUPTS

| Interrupt cause | DMA Ch. | Interrupt vector | | Interrupt control register | |
|---|---|---|---|---|---|
| | | Number | Address | Number | Address |
| Reset | —— | # 08 | FFFFDCH | —— | —— |
| INT9 instruction | —— | # 09 | FFFFD8H | —— | —— |
| Exception | —— | # 10 | FFFFD4H | —— | —— |
| CAN RX | —— | # 11 | FFFFD0H | ICR00 | 0000B0H |
| CAN TX/NS | —— | # 12 | FFFFCCH | | |
| Reserved | —— | # 13 | FFFFC8H | ICR01 | 0000B1H |
| Reserved | —— | # 14 | FFFFC4H | | |
| External Interrupt INT0/INT1 | —— | # 15 | FFFFC0H | ICR02 | 0000B2H |
| Time Base Timer | —— | # 16 | FFFFBCH | | |
| 16-bit Reload Timer 0 | —— | # 17 | FFFFB8H | ICR03 | 0000B3H |
| A/D Converter | —— | # 18 | FFFFB4H | | |
| I/O Timer | —— | # 19 | FFFFB0H | ICR04 | 0000B4H |
| External Interrupt INT2/INT3 | —— | # 20 | FFFFACH | | |
| Reserved | —— | # 21 | FFFFA8H | ICR05 | 0000B5H |
| PPG 0/1 | —— | # 22 | FFFFA4H | | |
| Input Capture 0 | —— | # 23 | FFFFA0H | ICR06 | 0000B6H |
| External Interrupt INT4/INT5 | —— | # 24 | FFFF9CH | | |
| Input Capture 1 | —— | # 25 | FFFF98H | ICR07 | 0000B7H |
| PPG 2/3 | —— | # 26 | FFFF94H | | |
| External Interrupt INT6/INT7 | —— | # 27 | FFFF90H | ICR08 | 0000B8H |
| Watch Timer | —— | # 28 | FFFF8CH | | |
| Reserved | —— | # 29 | FFFF88H | ICR09 | 0000B9H |
| Input Capture 2/3 | —— | # 30 | FFFF84H | | |
| Reserved | —— | # 31 | FFFF80H | ICR10 | 0000BAH |
| Reserved | —— | # 32 | FFFF7CH | | |
| Reserved | —— | # 33 | FFFF78H | ICR11 | 0000BBH |
| Reserved | —— | # 34 | FFFF74H | | |
| Reserved | —— | # 35 | FFFF70H | ICR12 | 0000BCH |
| 16-bit Reload Timer 1 | —— | # 36 | FFFF6CH | | |
| UART 0 RX | —— | # 37 | FFFF68H | ICR13 | 0000BDH |
| UART 0 TX | —— | # 38 | FFFF64H | | |
| UART 1 RX | —— | # 39 | FFFF60H | ICR14 | 0000BEH |
| UART 1 TX | —— | # 40 | FFFF5CH | | |
| Flash Memory | —— | # 41 | FFFF58H | ICR15 | 0000BFH |
| Delayed interrupt | —— | # 42 | FFFF54H | | |

## 12. ELECTRICAL CHARACTERISTICS

## 12.1 Absolute Maximum Ratings

($V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Power supply voltage | $V_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | |
| | $AV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $V_{CC}$ = $AV_{CC}$ *1 |
| | AVR | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | $AV_{CC}$ AVR AVss |
| Input voltage | $V_I$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *2 |
| Output voltage | $V_O$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | *2 |
| "L" level max. output current | $I_{OL}$ | — | 15 | mA | |
| "L" level avg. output current | $I_{OLAV}$ | — | 4 | mA | Average value over a period of 100ms |
| "L" level max. overall output current | $I_{OL}$ | — | 100 | mA | |
| "L" level avg. overall output current | $I_{OLAV}$ | — | 50 | mA | Average value over a period of 100ms |
| "H" level max. output current | $I_{OH}$ | — | –15 | mA | |
| "H" level avg. output current | $I_{OHAV}$ | — | –4 | mA | Average value over a period of 100ms |
| "H" level max. overall output current | $I_{OH}$ | — | -100 | mA | |
| "H" level avg. overall output current | $I_{OHAV}$ | — | -50 | mA | Average value over a period of 100ms |
| Power consumption | $P_D$ | — | 300 | mW | |
| Operating temperature | $T_A$ | –40 | +85 | °C | |
| Storage temperature | $T_{STG}$ | –55 | +150 | °C | |

*1: Set $AV_{CC}$ and $V_{CC}$ to the same voltage. Make sure that $AV_{CC}$ does not exceed $V_{CC}$ and that the voltage at the analog inputs does not exceed $AV_{CC}$ when the power is switched on.

*2: $V_I$ and $V_O$ should not exceed $V_{CC}$ + 0.3 V. VI should not exceed the specified ratings. However if the maximun current to/from a input is limited by some means with external components, the II rating supercedes the VI rating.

## 12.2 Recommended Conditions

($V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Sym-bol | Rated Value | | | Units | Remarks |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power supply voltage | $V_{CC}$ $AV_{CC}$ | 4.5 | 5.0 | 5.5 | V | Normal operating conditions |
| | | 3.0 | | 5.5 | V | Maintains RAM data in stop mode. |
| Input H voltage | $V_{IHS}$ | 0.8 $V_{CC}$ | | $V_{CC}$ + 0.3 | V | CMOS hysteresis input pin |
| | $V_{IHM}$ | $V_{CC}$ – 0.3 | | $V_{CC}$ + 0.3 | V | MD input pin |
| Input L voltage | $V_{ILS}$ | $V_{SS}$ – 0.3 | | 0.2 $V_{CC}$ | V | CMOS hysteresis input pin |
| | $V_{ILM}$ | $V_{SS}$ – 0.3 | | $V_{SS}$ + 0.3 | V | MD input pin |
| Smooth capacitor | $C_S$ | 0.022 | 0.1 | 1.0 | µF | Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the VCC should be greater than this capacitor. |
| Operating temperature | $T_A$ | –40 | | +85 | °C | |

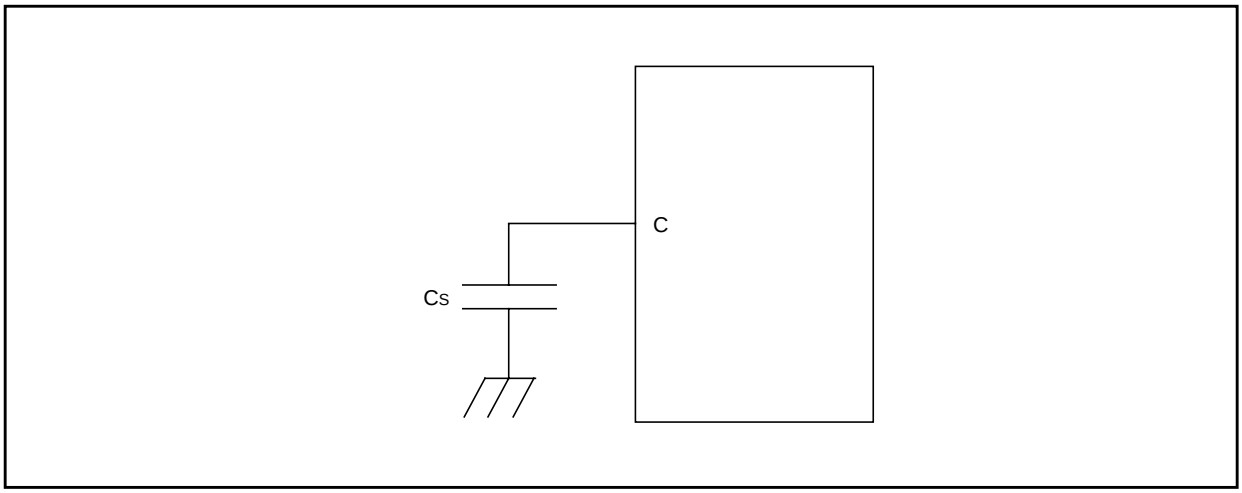



**Figure 12.1 C-Pin Connection Diagram**

## 13. DC CHARACTERISTICS

($T_A$ = –40 to +85°C, $V_{CC}$ = 5.0 V 10%, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Sym-bol | Pin | Test Condition | Rated Value | | | Units | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| Output H voltage | $V_{OH}$ | All output pins | $V_{CC}$ = 4.5 V, $I_{OH}$ = –4.0 mA | $V_{CC}$ – 0.5 | — | — | V | |
| Output L voltage | $V_{OL}$ | All output pins | $V_{CC}$ = 4.5 V, $I_{OL}$ = 4.0 mA | — | — | 0.4 | V | |
| Input leak current | $I_{IL}$ | | $V_{CC}$ = 5.5 V, $V_{SS}$ < $V_I$ < $V_{CC}$ | –5 | — | 5 | µA | |
| Power supply current * | $I_{CC}$ | $V_{CC}$ | $V_{CC}$ = 5.0 V±10%, Int. frequency: 16 MHz, At normal operating | — | 35 | 40 | mA | MB90497 |
| | | | | — | 35 | 40 | mA | MB90F497 |
| | | | VCC = 5.0 V±10%, Int. frequency: 16 MHz, At flash programming | | 45 | 50 | mA | MB90F497 |
| | | | VCC = 5.0 V±10%, Int. frequency: 16 MHz, At flash erasing | | 45 | 50 | mA | MB90F497 |
| | $I_{CCS}$ | | $V_{CC}$ = 5.0 V±10%, Int. frequency: 16 MHz, At sleep | — | 11 | 18 | mA | MB90497 |
| | | | | — | 11 | 18 | mA | MB90F497 |
| | $I_{CTS}$ | | VCC = 5.0 V 10%, Int. frequency: 16 MHz, At timer mode | | 0.6 | 1.2 | mA | MB90497 |
| | | | | | 0.6 | 1.2 | mA | MB90F497 |
| | | | | | | | | |
| | $I_{CCL}$ | | $V_{CC}$ = 5.0 V, Int. frequency: 8 kHz, At sub operation | — | 16 | 20 | µA | MB90497 |
| | | | | — | 116 | 220 | µA | MB90F497 |
| | $I_{CCLS}$ | | $V_{CC}$ = 5.0 V, Int. frequency: 8 kHz, At sub sleep | — | 7.5 | 10 | µA | MB90497 |
| | | | | — | 8 | 20 | µA | MB90F497 |
| | $I_{CCT}$ | | $V_{CC}$ = 5.0 V, Int. frequency: 8 kHz, At watch mode | — | 3 | 5 | µA | MB90497 |
| | | | | — | 3 | 10 | µA | MB90F497 |
| | $I_{CCH}$ | | $V_{CC}$ = 5.0 V±10%, At stop, $T_A$ = 25°C | — | 2 | 20 | µA | MB90497 |
| | | | | — | 2 | 20 | µA | MB90F497 |
| Input capacity | $C_{IN}$ | Other than $AV_{CC}$, $AV_{SS}$, AVR, C, $V_{CC}$, $V_{SS}$ | — | — | 10 | 80 | pF | |

*: Current values are tentative. They are subject to change without notice according to improvements in the characteristics. The power supply current testing conditions are when using the external clock with square pulses.

## 14. AC CHARACTERISTICS

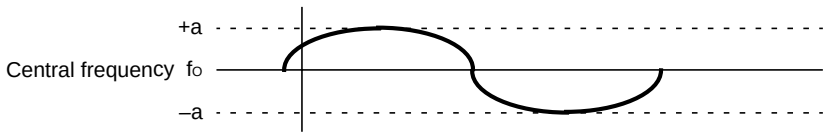
## 14.1 Clock Timing

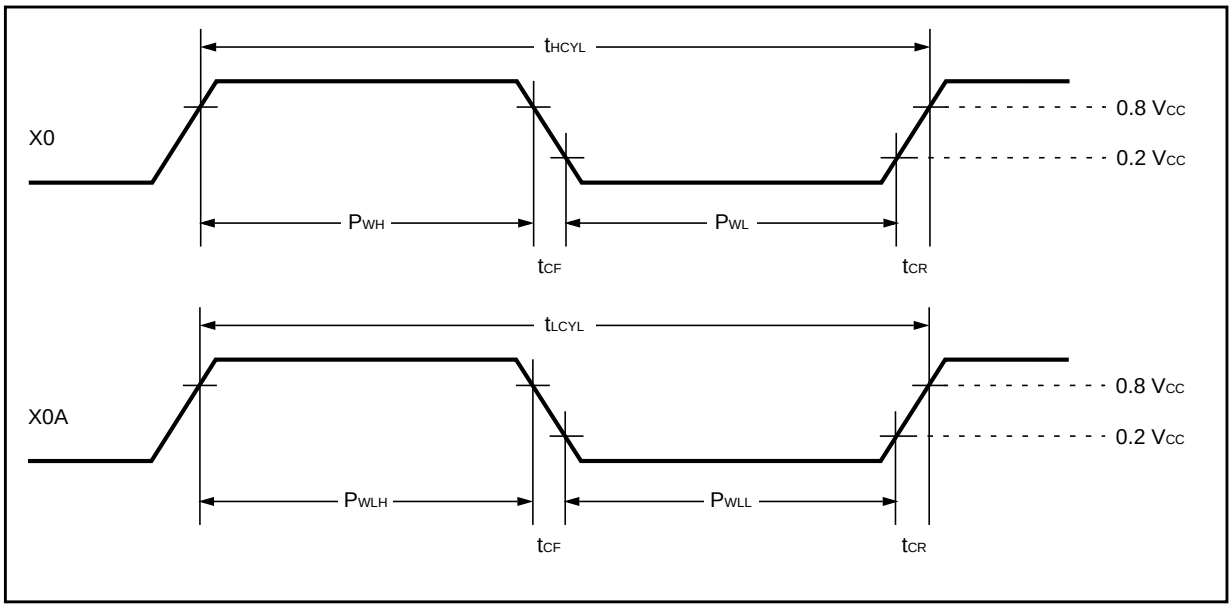
($T_A$ = –40 to +85°C, $V_{CC}$ = 5.0 V 10%, $V_{SS}$ = $AV_{SS}$ = 0 V)

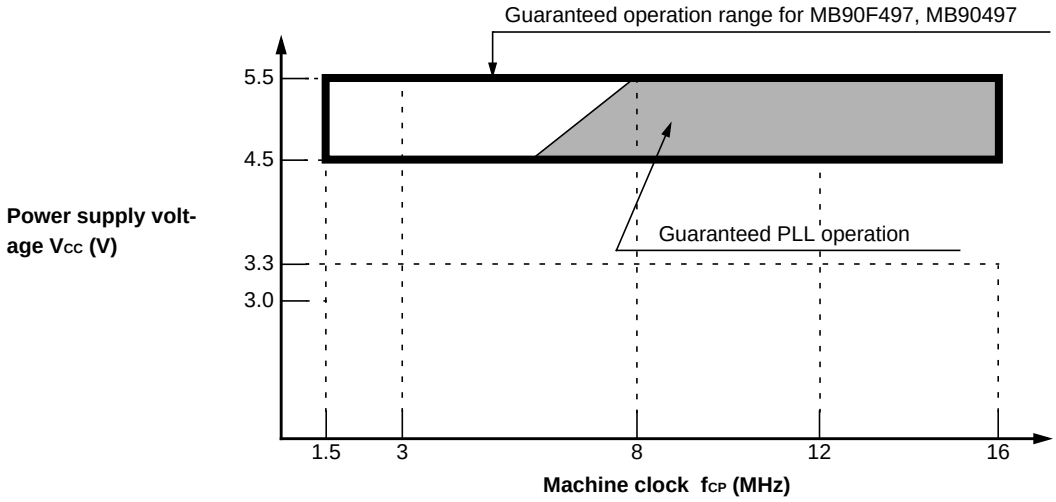
| Parameter | Symbol | Pin | Rated Value | | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Oscillation frequency | $f_C$ | X0, X1 | 3 | — | 16 | MHz | |
| | $f_{CL}$ | X0A, X1A | — | 32.768 | — | kHz | |
| Oscillation cycle time | $t_{HCYL}$ | X0, X1 | 62.5 | — | 333 | ns | |
| | $t_{LCYL}$ | X0A, X1A | — | 30.5 | — | µs | |
| Frequency deviation with PLL * | Δf | — | — | — | 5 | % | |
| Input clock pulse width | $P_{WH}$, $P_{WL}$ | X0 | 10 | — | — | ns | Duty ratio is about 30 to 70%. |
| | $P_{WLH}$,$P_{WLL}$ | X0A | — | 15.2 | — | µs | |
| Input clock rise and fall time | $t_{CR}$, $t_{CF}$ | X0 | — | — | 5 | ns | When using external clock |
| Machine clock frequency | $f_{CP}$ | — | 1.5 | — | 16 | MHz | When using main clock |
| | $f_{LCP}$ | — | — | 8.192 | — | kHz | When using sub-clock |
| Machine clock cycle time | $t_{CP}$ | — | 62.5 | — | 666 | ns | When using main clock |
| | $t_{LCP}$ | — | — | 122.1 | — | µs | When using sub-clock |

*: Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.

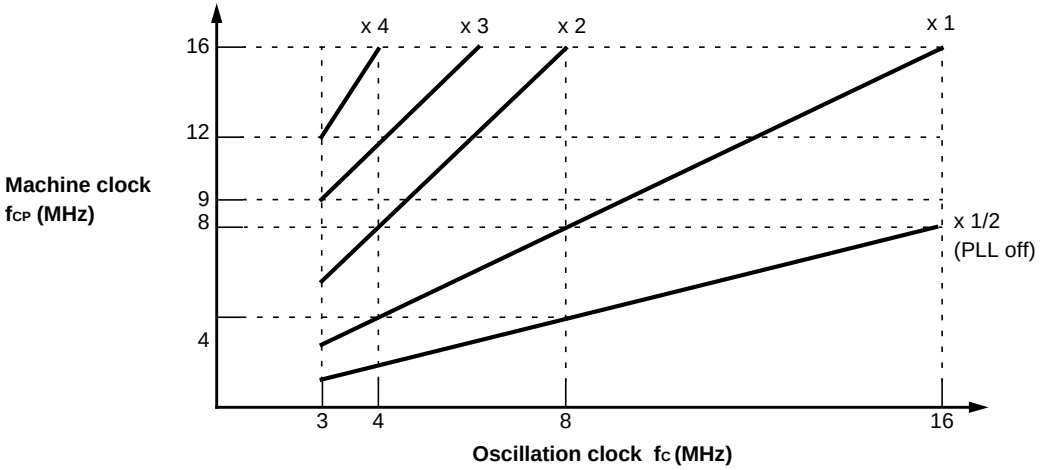
$$\Delta f = \frac{|a|}{f_O} \times 100\%$$






**Guaranteed operation range**



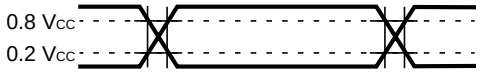

**Ocsillation clock frequency and Machine clock frequency**

**Figure 14.1 Clock Timing**

AC characteristics are set to the measured reference voltage values below.

- **Input signal waveform**

**Hysteresis Input Pin**




- **Output signal waveform**

**Output Pin**

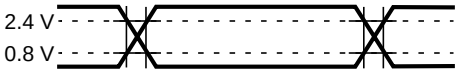



**Figure 14.2 Measured Reference Voltages**

## 14.2 Clock Output Timing

($T_A$ = –40 to +85°C, $V_{CC}$ = 5.0 V ±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin | Test Condition | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| Cycle time | $t_{CYC}$ | CLK | VCC = 5 V ±10% | 62.5 | — | ns | |
| CLK↑ ⇒ CLK↓ | $t_{CHCL}$ | | | 20 | — | ns | |

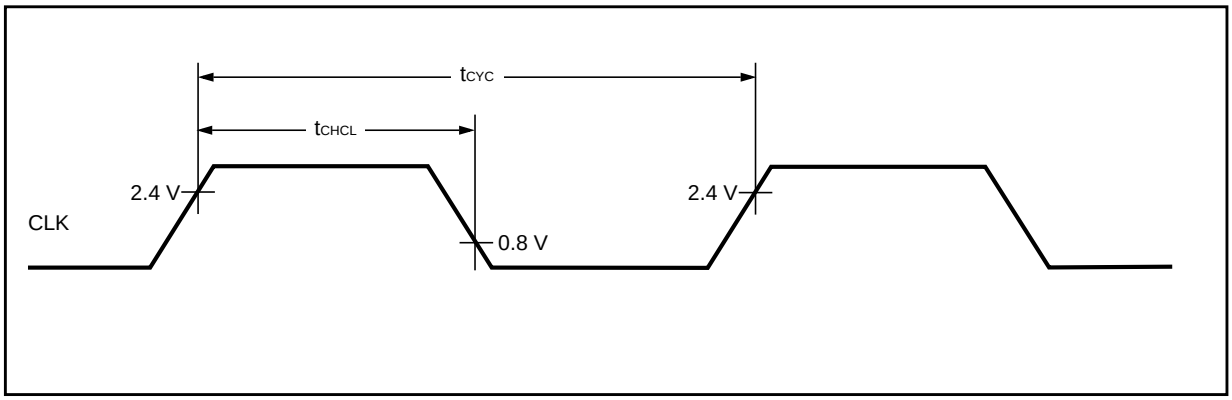



**Figure 14.3 Measured CLK timing**

## 14.3 Reset Input

($T_A$ = –40 to +85°C, $V_{CC}$ = 5.0 V 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Reset input time | $t_{RSTL}$ | RST | 16 $t_{CP}$ | — | ns | |

“tcp” represents one cycle time of the machine clock.

Any reset can not fully initialize the Flash Memory if it is performing the automatic algorithm.

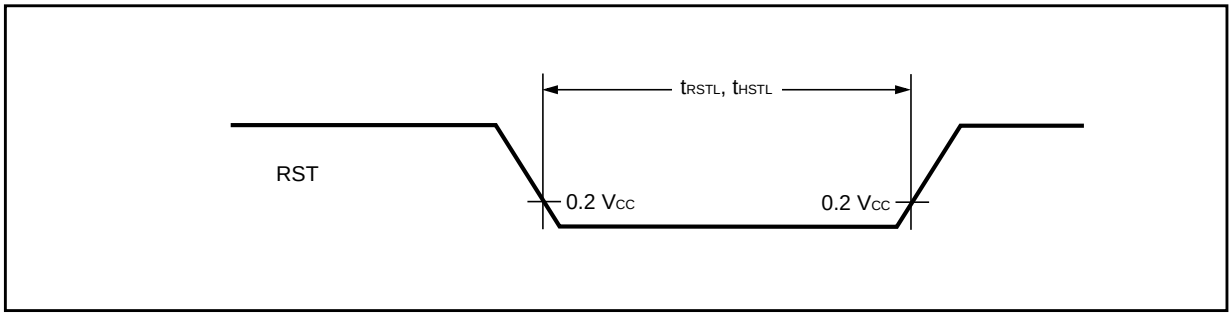
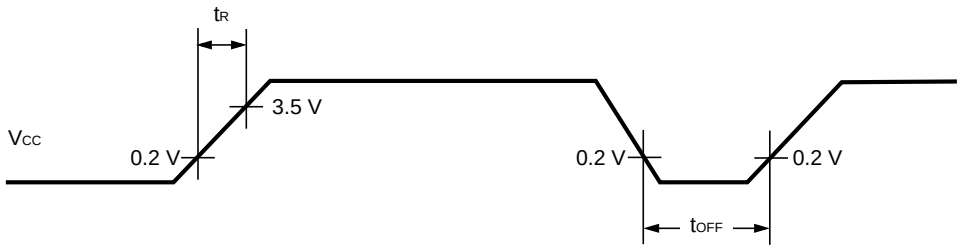



**Figure 14.4 Measured RST timing**

## 14.4 Power On Reset

($T_A$ = –40 to +85°C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V)

| Parameter | Symbol | Pin | Test Condition | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| Power on rise time | $t_R$ | $V_{CC}$ | — | 0.05 | 30 | ms | |
| Power off time | $t_{OFF}$ | $V_{CC}$ | | 50 | — | ms | Due to repetitive operation |




If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 mV/sec, you can operate while using the PLL clock.

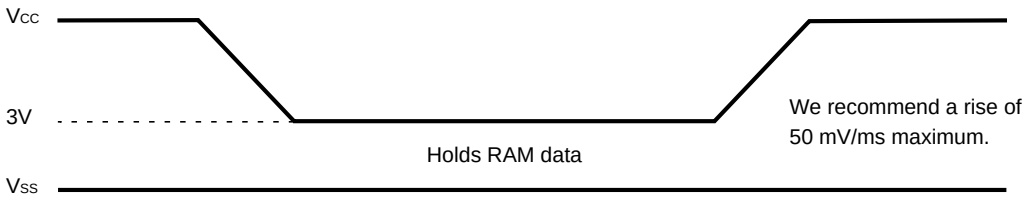



**Figure 14.5 Power On Reset Timing**

## 14.5 External Bus Timing (Read)

($T_A$ = –40 to +85°C, $V_{CC}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Test Condition | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| ALE pulse width | $t_{LHLL}$ | ALE | — | $t_{CP}/2 - 20$ | | ns | |
| Valid address ⇒ ALE ↓ time | $t_{AVLL}$ | ALE, A23 - A16, AD15 - AD00 | | $t_{CP}/2 - 20$ | — | ns | |
| ALE ↓ ⇒ Address valid time | $t_{LLAX}$ | ALE, AD15 - AD00 | | $t_{CP}/2 - 15$ | — | ns | |
| Valid address ⇒ $\overline{RD}$ ↓ time | $t_{AVRL}$ | A23 - A16, AD15 - AD00, $\overline{RD}$ | | $t_{CP} - 15$ | — | ns | |
| Valid address ⇒ Valid data input | $t_{AVDV}$ | A23 - A16, AD15 - AD00 | | — | $5\ t_{CP}/2 - 60$ | ns | |
| $\overline{RD}$ pulse width | $t_{RLRH}$ | $\overline{RD}$ | | $3\ t_{CP}/2 - 20$ | — | ns | |
| $\overline{RD}$ ↓ ⇒ Valid data input | $t_{RLDV}$ | $\overline{RD}$, AD15 - AD00 | | — | $3\ t_{CP}/2 - 60$ | ns | |
| $\overline{RD}$ ↑ ⇒ Data hold time | $t_{RHDX}$ | $\overline{RD}$, AD15 - AD00 | | 0 | — | ns | |
| $\overline{RD}$ ↓ ⇒ ALE ↑ time | $t_{RHLH}$ | $\overline{RD}$, ALE | | $t_{CP}/2 - 15$ | — | ns | |
| $\overline{RD}$ ↑ ⇒ Address valid time | $t_{RHAX}$ | $\overline{RD}$, A23 - A16 | | $t_{CP}/2 - 10$ | — | ns | |
| Valid address ⇒ CLK ↑ time | $t_{AVCH}$ | A23 - A16, AD15 - AD00, CLK | | $t_{CP}/2 - 20$ | — | ns | |
| $\overline{RD}$ ↓ ⇒ CLK ↑ time | $t_{RLCH}$ | $\overline{RD}$, CLK | | $t_{CP}/2 - 20$ | — | ns | |
| ALE ↓ ⇒ $\overline{RD}$ ↓ time | $t_{LLRL}$ | ALE, $\overline{RD}$ | | $t_{CP}/2 - 15$ | — | ns | |

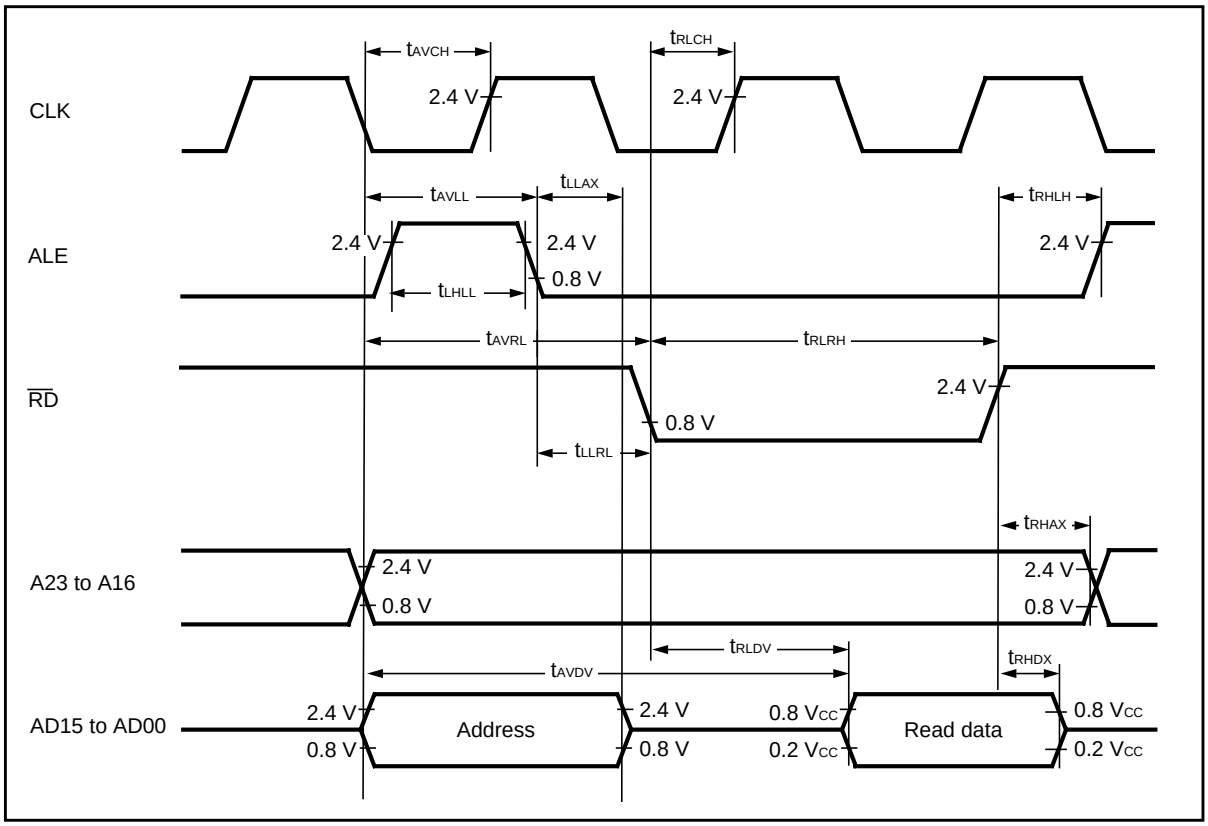



**Figure 14.6 Bus Timing (Read)**

## 14.6 External Bus Timing (Write)

($T_A$ = –40 to +85°C, $V_{CC}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Test Condition | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| Valid address ⇒ $\overline{WR}$ ↓ time | $t_{AVWL}$ | A23 - A16, AD15 - AD00, $\overline{WR}$ | — | $t_{CP}$ – 15 | — | ns | |
| $\overline{WR}$ pulse width | $t_{WLWH}$ | $\overline{WR}$ | | 3 $t_{CP}$/2 – 20 | — | ns | |
| Valid data output ⇒ $\overline{WR}$ ↑ time | $t_{DVWH}$ | AD15 - AD00, $\overline{WR}$ | | 3 $t_{CP}$/2 – 20 | — | ns | |
| $\overline{WR}$ ↑ ⇒ Data hold time | $t_{WHDX}$ | AD15 - AD00, $\overline{WR}$ | | 20 | — | ns | |
| $\overline{WR}$ ↑ ⇒ Address valid time | $t_{WHAX}$ | A23 - A16, $\overline{WR}$ | | $t_{CP}$/2 – 10 | — | ns | |
| $\overline{WR}$ ↑ ⇒ ALE ↑ time | $t_{WHLH}$ | $\overline{WR}$, ALE | | $t_{CP}$/2 – 15 | — | ns | |
| $\overline{WR}$ ↓ ⇒ CLK ↑ time | $t_{WLCH}$ | $\overline{WR}$, CLK | | $t_{CP}$/2 – 20 | — | ns | |

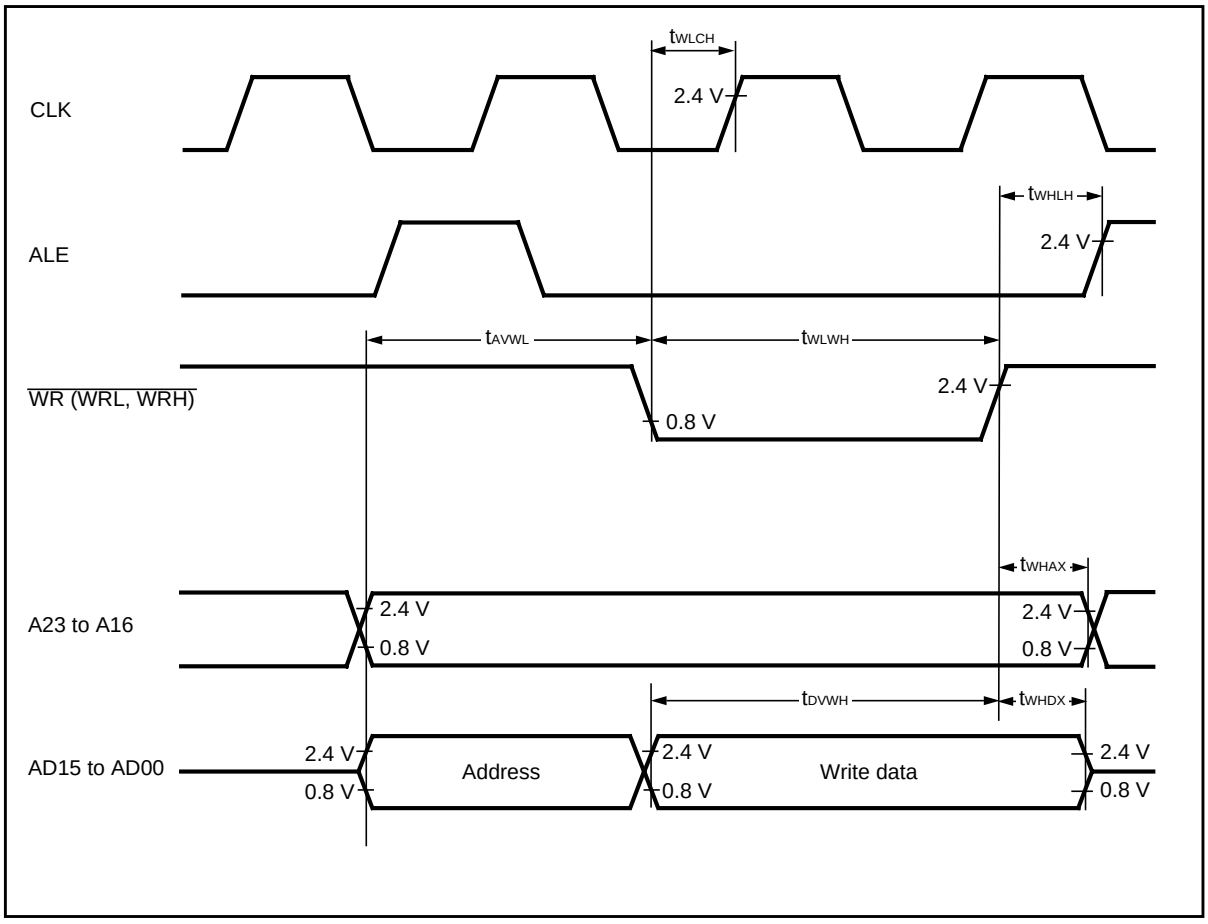



**Figure 14.7 Bus Timing (Write)**

## 14.7 External Bus Ready Input Timing

($T_A$ = –40 to +85°C, $V_{CC}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Test Condition | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| RDY setup time | $t_{RYHS}$ | RDY | — | 45 | — | ns | |
| RDY hold time | $t_{RYHH}$ | RDY | | 0 | — | ns | |

Note: If the RDY setup time is insufficient, use the auto-ready function.

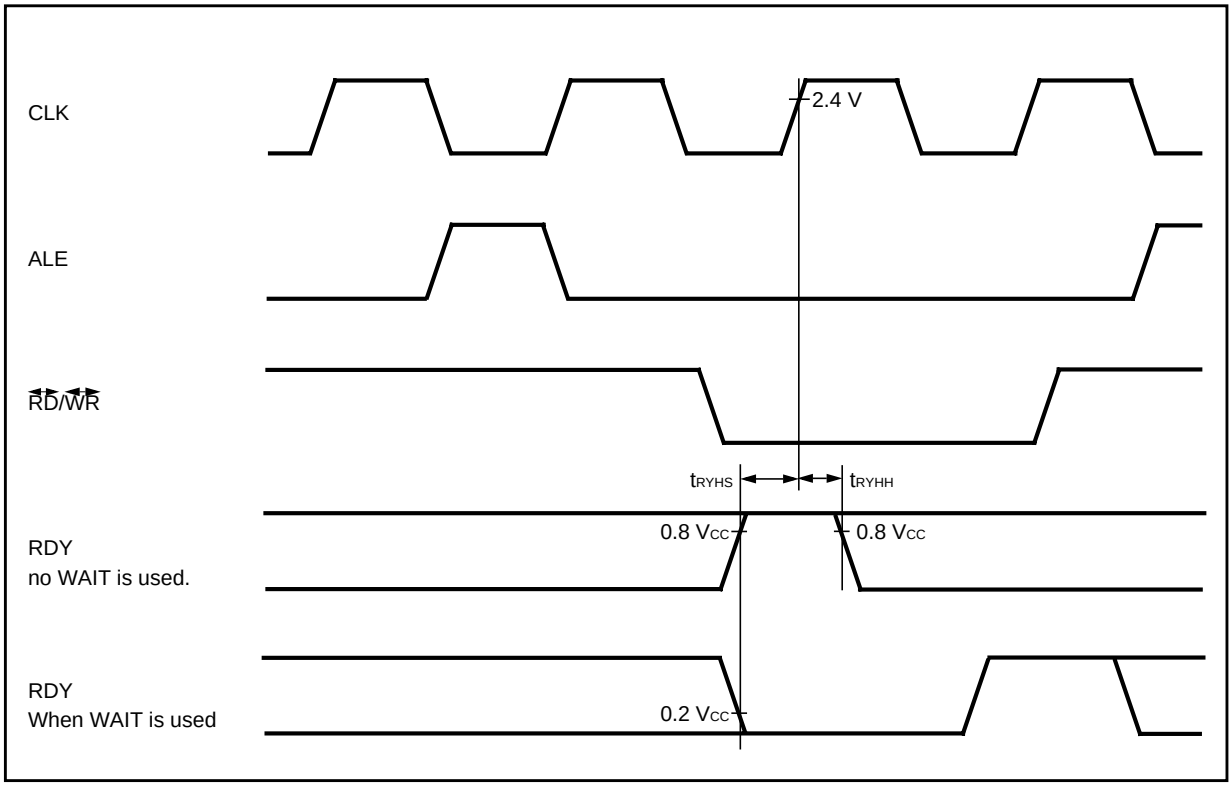



**Figure 14.8 Ready Input Timing**

## 14.8 External Bus Hold Timing

($T_A$ = –40 to +85°C, $V_{CC}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Test Condition | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| Pin floating ⇒ $\overline{HAK}$ ↓ time | $t_{XHAL}$ | $\overline{HAK}$ | — | 30 | $t_{CP}$ | ns | |
| $\overline{HAK}$ ↑ time ⇒ Pin valid time | $t_{HAHV}$ | $\overline{HAK}$ | | $t_{CP}$ | 2 $t_{CP}$ | ns | |

Note: There is more than 1 cycle from when HRQ reads in until the HAK is changed.

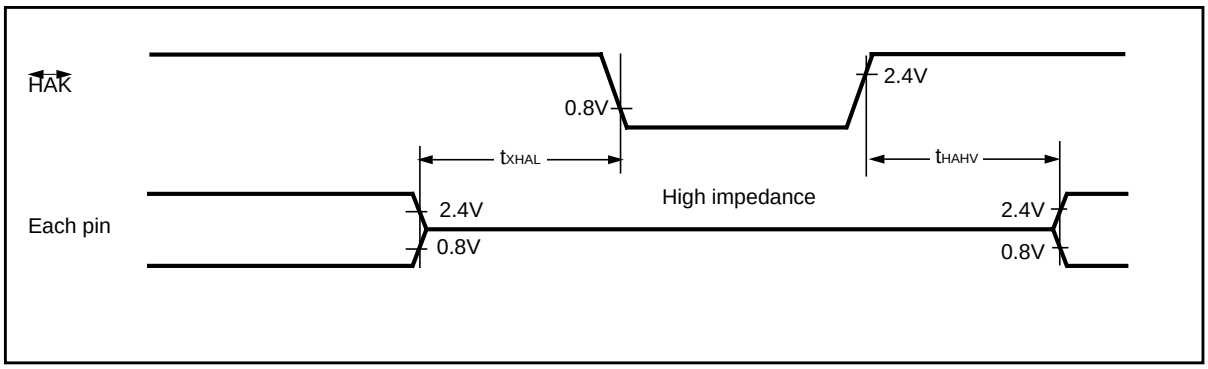



**Figure 14.9 Hold Timing**

## 14.9 UART1 Timing

($T_A$ = –40 to +85°C, $V_{CC}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin Symbol | Test Condition | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK1 | Internal clock operation output pins are $C_L$ = 80 pF + 1 TTL. | 8 $t_{CP}$ | — | ns | |
| SCK ↓ ⇒ SOT delay time | $t_{SLOV}$ | SCK1, SOT1 | | –80 | 80 | ns | |
| Valid SIN ⇒ SCK ↑ | $t_{IVSH}$ | SCK1, SIN1 | | 100 | — | ns | |
| SCK ↑ ⇒ Valid SIN hold time | $t_{SHIX}$ | SCK1, SIN1 | | 60 | — | ns | |
| Serial clock "H" pulse width | $t_{SHSL}$ | SCK1 | External clock operation output pins are $C_L$ = 80 pF + 1 TTL. | 4 $t_{CP}$ | — | ns | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK1 | | 4 $t_{CP}$ | — | ns | |
| SCK ↓ ⇒ SOT delay time | $t_{SLOV}$ | SCK1, SOT1 | | — | 150 | ns | |
| Valid SIN ⇒ SCK ↑ | $t_{IVSH}$ | SCK1, SIN1 | | 60 | — | ns | |
| SCK ↑ ⇒ Valid SIN hold time | $t_{SHIX}$ | SCK1, SIN1 | | 60 | — | ns | |

Notes:

1. AC characteristic in CLK synchronized mode.
2. $C_L$ is load capacity value of pins when testing.
3. $t_{CP}$ is the machine cycle (Unit: ns).

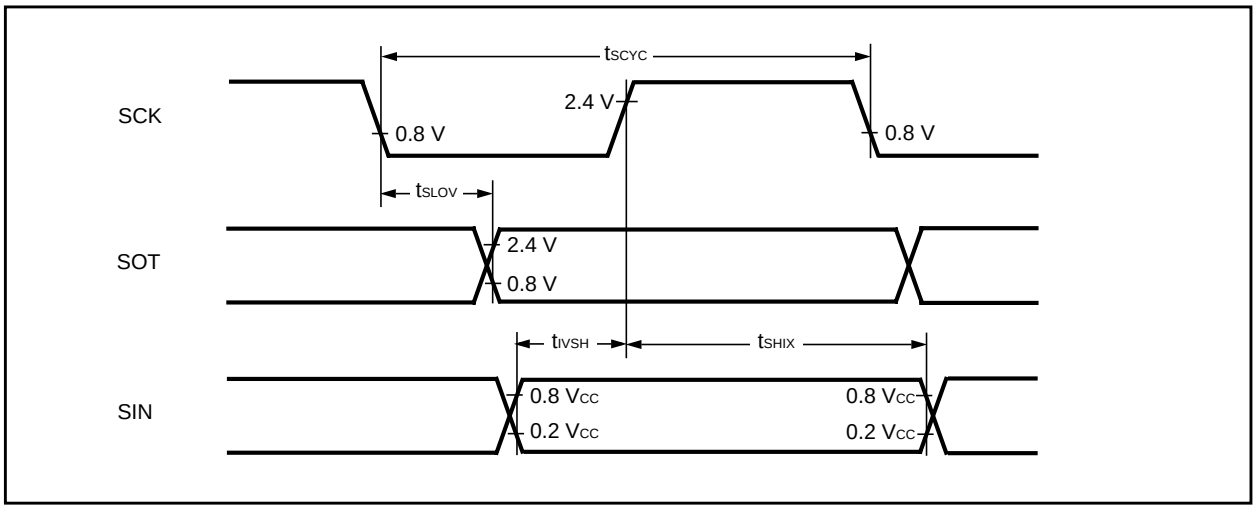



**Figure 14.10 Internal Shift Clock Mode**

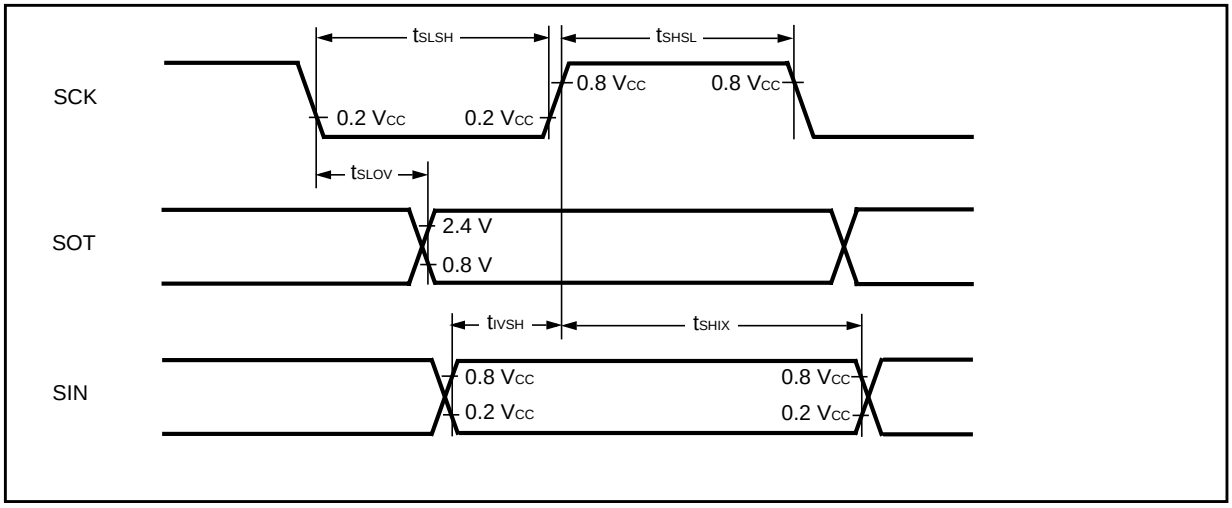



**Figure 14.11 External Shift Clock Mode**

## 14.10 Timer Related Resource Input Timing

($T_A$ = –40 to +85°C, $V_{CC}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Test Condition | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| Input pulse width | $t_{TIWH}$ | TIN0, TIN1 | — | 4 $t_{CP}$ | — | ns | |
| | $t_{TIWL}$ | IN0 to IN3 | | | | | |

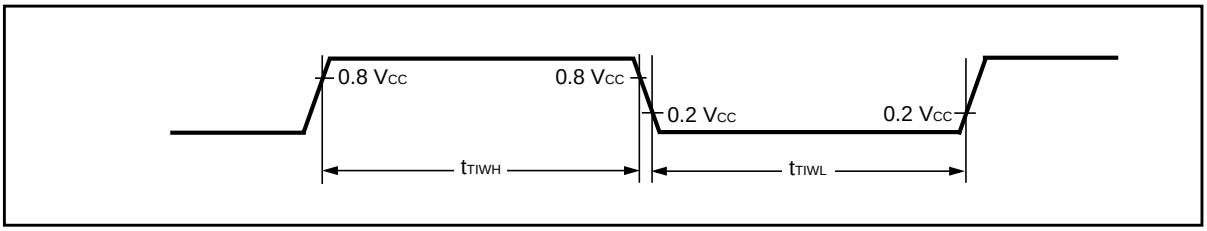



**Figure 14.12 Timer Input Timing**

## 14.11 Timer Related Resource Output Timing

($T_A$ = –40 to +85°C, $V_{CC}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Test Condition | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| CLK ↑ ⇒ $T_{OUT}$ change time | $t_{TO}$ | TOT0 to TOT1, PPG0 to PPG3 | — | 30 | — | ns | |

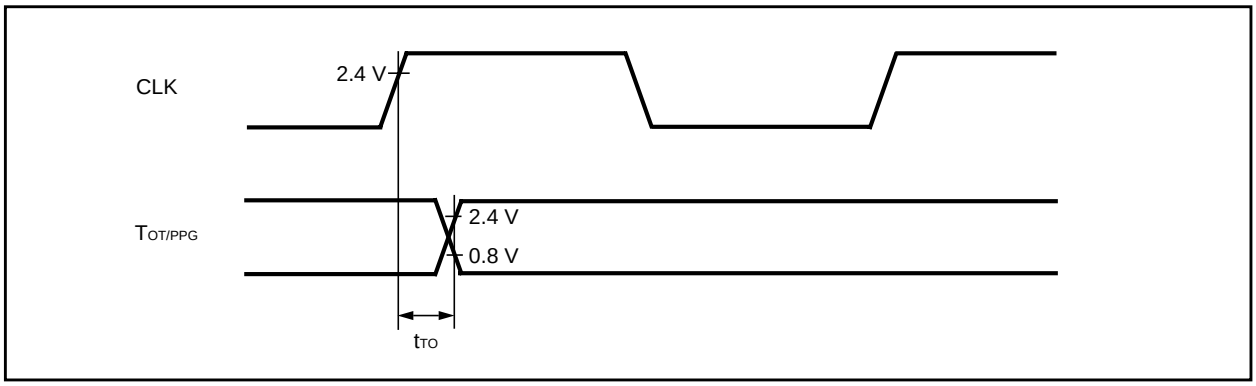



**Figure 14.13 Timer Output Timing**

## 14.12 External Trigger Input Timing

($T_A$ = –40 to +85°C, $V_{CC}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Test Condition | Rated Value | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | | |
| Input pulse width | $t_{TRGH}$<br>$t_{TRGL}$ | INT0 to INT7, ADTG | — | 5 $t_{CP}$ | — | ns | |

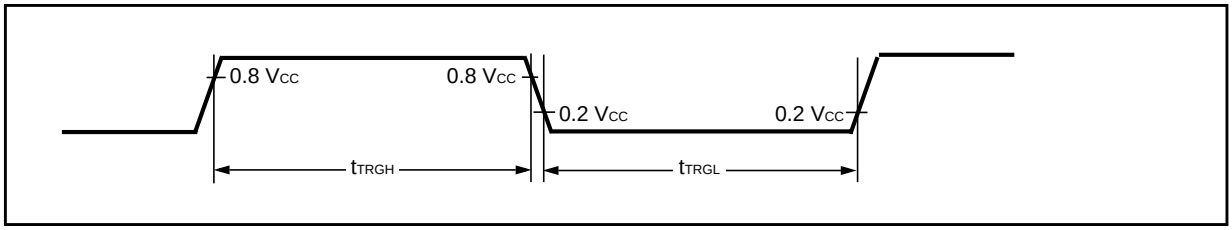



**Figure 14.14 External Trigger Input Timing**

## 14.13 A/D Converter

($T_A$ = –40 to +85°C, 3.0 V ≤ AVR – AVSS, $V_{CC}$ = $AV_{CC}$ = 5.0 V 10%, $V_{SS}$ = $AV_{SS}$ = 0 V)

| Parameter | Symbol | Pin | Rated Value | | | Units | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Resolution | — | — | — | | 10 | bit | |
| Conversion error | — | — | — | — | 5.0 | LSB | |
| Nonlinearity error | — | — | — | — | 2.5 | LSB | |
| Differential nonlinearity error | — | — | — | — | 1.9 | LSB | |
| Zero reading voltage | $V_{OT}$ | AN0 to AN7 | AVSS – 3.5 | AVSS +0.5 | AVSS + 4.5 | LSB | 1 LSB = AVR/1024 |
| Full scale reading voltage | $V_{FST}$ | AN0 to AN7 | AVR – 6.5 | AVR –1.5 | AVR + 1.5 | LSB | |
| Conversion time | — | — | — | 176$t_{CP}$ | — | ns | |
| Sampling time | — | — | — | 64$t_{CP}$ | — | ns | |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | — | — | 10 | µA | |
| Analog input voltage range | $V_{AIN}$ | AN0 to AN7 | AVSS | — | AVR | V | |
| Reference voltage range | — | AVR | AVSS + 2.7 | — | AVCC | V | |
| Power supply current | $I_A$ | AVCC | — | 5 | — | mA | |
| | $I_{AH}$ | AVCC | — | — | 5 | µA | *1 |
| Reference voltage current | $I_R$ | AVR | 200 | 400 | 600 | µA | |
| | $I_{RH}$ | AVR | — | — | 5 | µA | *1 |
| Offset between input channels | — | AN0 to AN7 | — | — | 4 | LSB | |

*1: When not operating A/D converter, this is the current ($V_{CC}$ = $AV_{CC}$ = AVR = 5.0 V) when the CPU is stopped.

Terminology:

Conversion error : Absolute maximum conversion deviation with respect to the theoretical conversion line.

Nonlinearlity : Relative maximum conversion deviation with respect to the theoretical conversion line connecting to the device-unique zero reading voltage and full-scale reading voltage.

Differential non-linearlity : Maximum conversion deviation in any two adjacent reading voltages with respect to the theoretical LSB conversion step.

Zero-reading voltage : Input voltage which results in the minimum conversion value.

Full-scale reading voltage : Input voltage which results in the maximum coversion value.

Notes:

1. The accuracy gets worse as AVR - AVSS becomes smaller.
2. Analog input external circuit output impedance should use the following conditions:
   External circuit output impedance less than 15 kΩ
3. If the external circuit output impedance is too high, there may be insufficient time for sampling of the analog voltage.

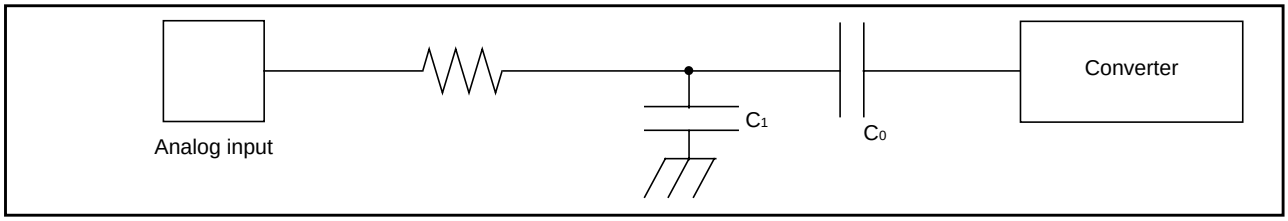



**Figure 14.15 Analog Input pin**

## 15. PACKAGE DIMENSIONS

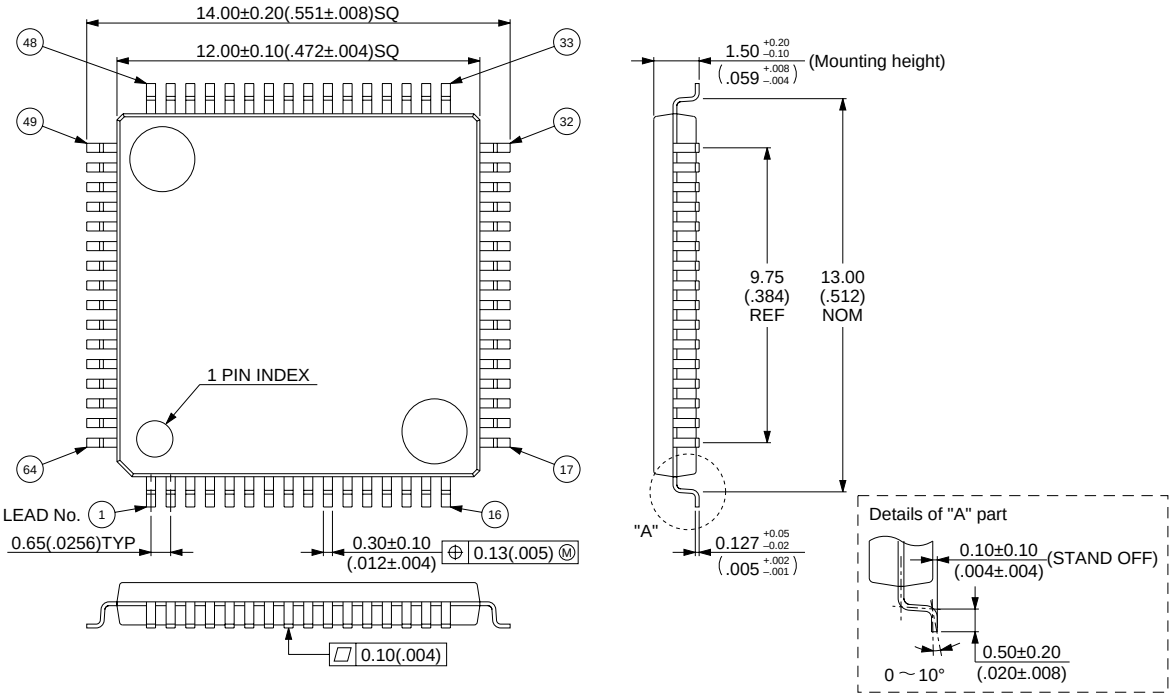





**Figure 15.1 Package Code: FPT-64P-M09**

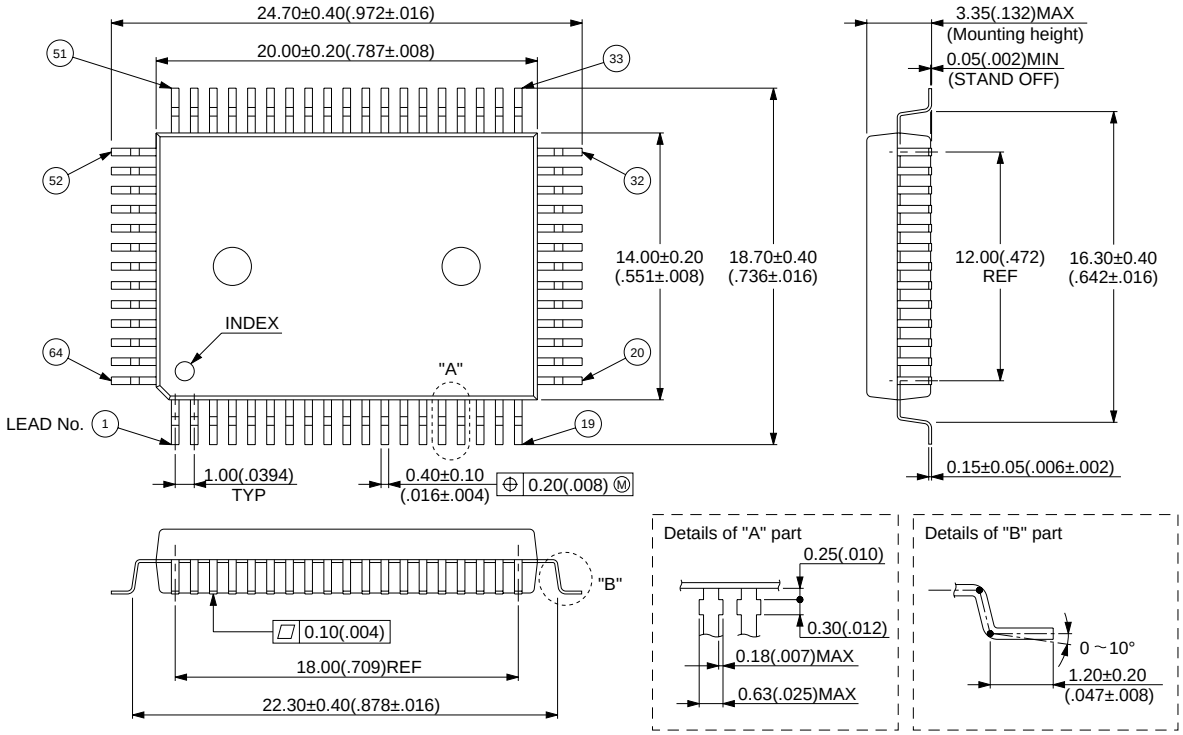





**Figure 15.2 Package Code FPT-64P-M06**