FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12538-1E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89990 Series

MB89997

■ OUTLINE

The MB89990 series microcontrollers contain various resources such as timers, external interrupts, and remote-control functions, as well as an F²MC*-8L CPU core for low-voltage and high-speed operations. These single-chip microcontrollers are suitable for small devices such as remote controllers incorporating compact packages.

*: F²MC stands for FUJITSU Flexible Microcontroller.

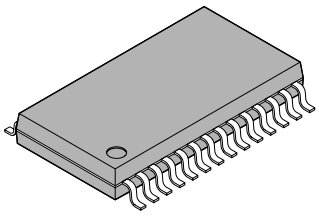
■ FEATURES

- Minimum execution time: 0.95 µs at 4.2 MHz (V_{CC} = 2.7 V)
- F²MC-8L family CPU core
- Two timers
  8/16-bit timer/counter
  20-bit timebase counter

(Continued)

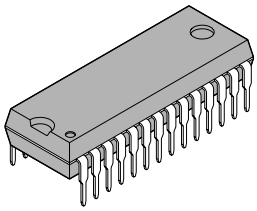
■ PACKAGE

28-pin Plastic SOP



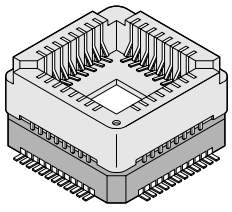
(FPT-28P-M17)

28-pin Plastic SH-DIP



(DIP-28P-M03)

48-pin Ceramic MQFP



(MQP-48C-P01)

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- External interrupts
  Edge detection (Edge selection enabled): 3 channels
  Low-level interrupt (Wake-up function): 8 channels
- Internal remote-control transmission frequency generator
- Low-power consumption modes
  Stop mode (Almost no current consumption occurs because oscillation stops.)
  Sleep mode (The current consumption is about 1/3 of that during normal operation because the CPU stops.)
- Packages
  SOP-28 and SH-DIP-28

■ PRODUCT LINEUP

Part number / Item	MB89997	MB89P195*1	MB89PV190*2
Classification	Mass-produced products (mask ROM products)	One-time PROM product	For development and evaluation
ROM size	32 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal PROM, to be programmed with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	128 × 8 bits	256 × 8 bits	
CPU functions	The number of basic instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, and 16 bits Minimum execution time: 0.95 µs at 4.2 MHz Interrupt processing time: 8.57 µs at 4.2 MHz		
Ports	I/O port (N channel open drain): 6 I/O port (CMOS): 16 (13 serves as resources) Total: 22		
8/16-bit timer/ counter	2 channels for 8-bit timer counter or for 16-bit event counter (operation clock: 1.9 µs, 30.4 µs, and 487.6 µs at 4.2 MHz, and external clock)		
External interrupt 1	3 independent channels (edge selection, interrupt vector, and interrupt source flag) Rising edge/falling edge/both edge selectability Used for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)		
External interrupt 2 (Wake-up function)	8 channels (low-level interrupt only)		
Remote-control transmission frequency generation	The pulse width and cycle are software-programmable.		

(Continued)

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Part number / Item	MB89997	MB89P195*1	MB89PV190*2
Low-power consumption (standby mode)	Sleep mode and stop mode		
Process	CMOS		
Power supply voltage*3	2.2 V to 6.0 V	2.7 V to 6.0 V	
EPROM for use			MBM27C256A-20TVM

*1 : The MB89P195 microtroller is the one-time product for the MB89190 series which can be also be used for the MB89990 series.

*2 : The MB89PV190 microtroller is the evaluation and development product for the MB89190 series which can be also be used for the MB89990 series.

*3 : Varies with conditions such as operating frequencies (see "■ Electrical Characteristics.")

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89997	MB89P195	MB89PV190
DIP-28P-M03	○	×	×
FPT-28P-M17	○	○	×
MQP-48C-P01	×	×	○ *

○ : Available × : Not available

* : A socket (manufacturer: Sun Hayato Co., Ltd.) for pin pitch conversion is available.
480F-28SOP-8L: (MQP-48C-P01) → for conversion to FPT-28P-M02

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106

Note: For more information on each package, see "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback model, verify its difference from the model that will actually be used. Take particular care on the following points:

- On the MB89997, addresses 0140_H to 0180_H cannot be used for register banks.
- The stack area, etc., is set in the upper limit of the RAM.

2. Current Consumption

- In the case of MB89PV190, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, a model with an OTPROM (EPROM) will consume more current than a model with a mask ROM.
  However, current consumption in the sleep/stop mode in the same. (For more information, see "■ Electrical Characteristics.")

3. Mask Options

Functions that can be selected as options and how to designate these options vary by model.

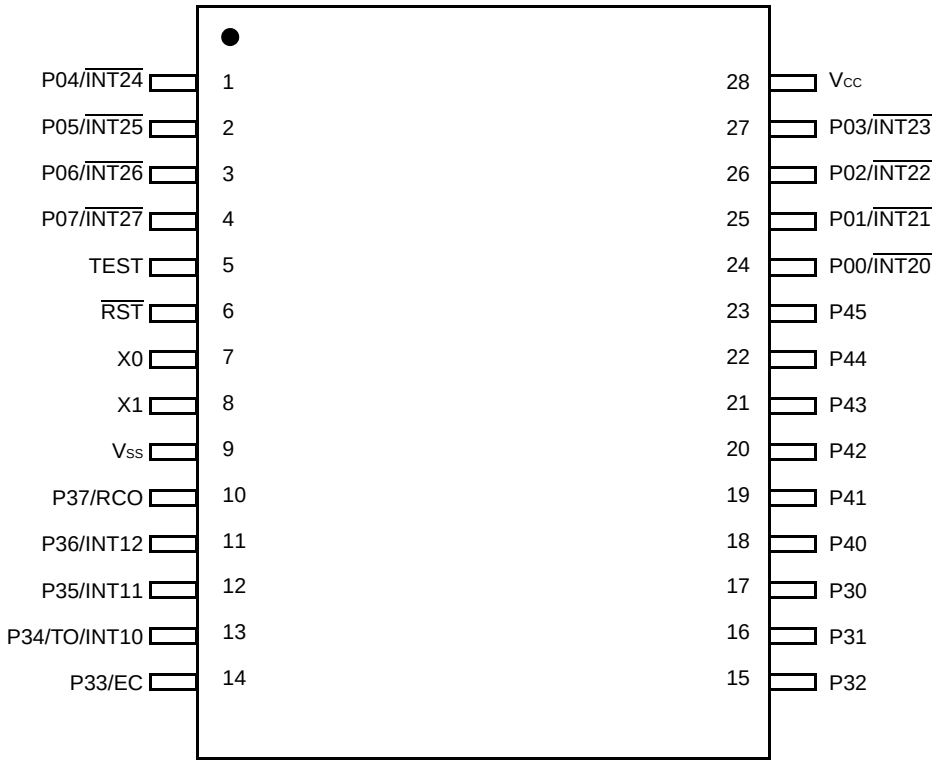
Before using options check "■ Mask Options."

Take particular care on the following points:

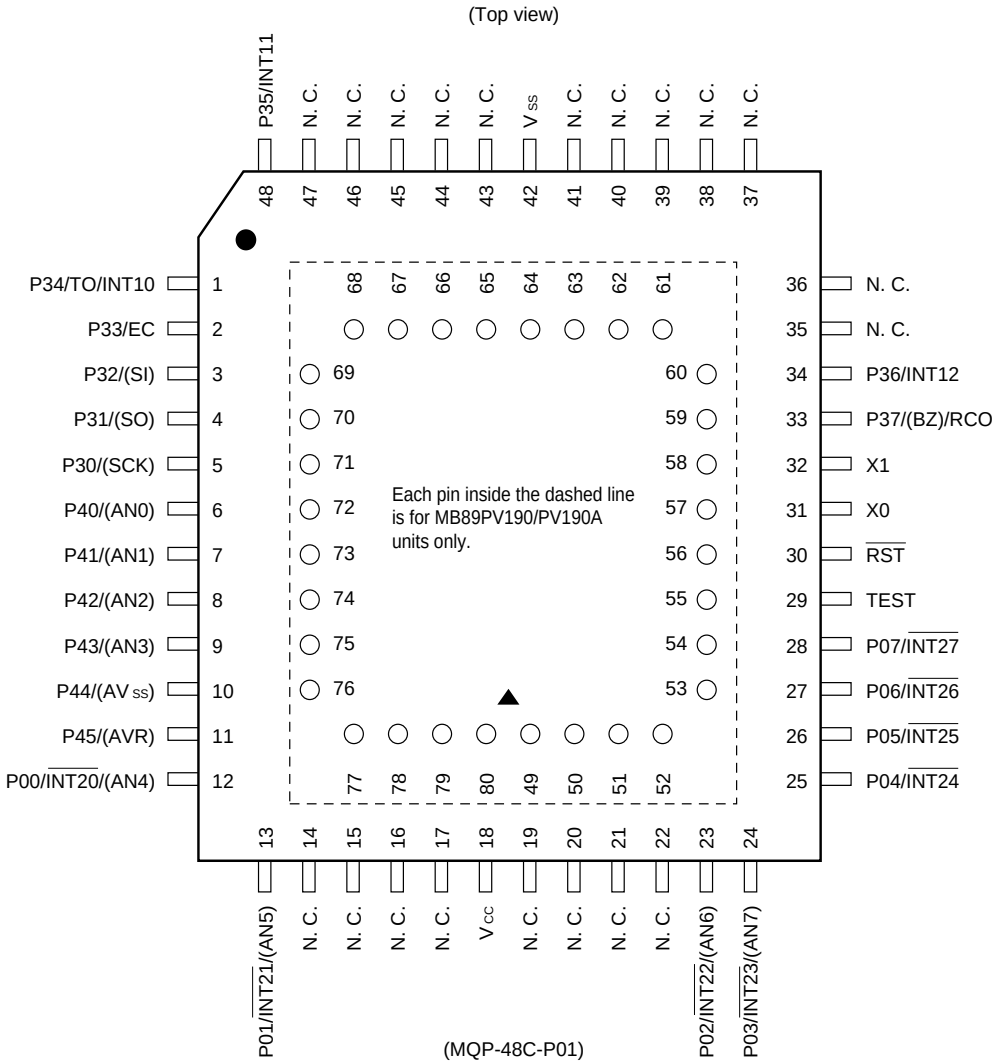
- The power-on reset option is fixed as "enabled" for MB89P195.
- Options are fixed on the MB89PV190.

■ PIN ASSIGNMENT

(Top view)



(FPT-28P-M17)
(DIP-28P-M03)



- **Pin assignment on the package top (MB89PV190/PV190A only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
49	V_{PP}	57	N.C.	65	O4	73	$\overline{OE}$
50	A12	58	A2	66	O5	74	N.C.
51	A7	59	A1	67	O6	75	A11
52	A6	60	A0	68	O7	76	A9
53	A5	61	O1	69	O8	77	A8
54	A4	62	O2	70	$\overline{CE}$	78	A13
55	A3	63	O3	71	A10	79	A14
56	N.C.	64	V_{SS}	72	N.C.	80	V_{CC}

N.C.: Internally connected. Do not use.

Note: Parenthesized pin function is only for the MB89PV190A.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
SOP*1, SH-DIP*2	MQFP*3			
7	31	X0	A	Clock oscillation pins
8	32	X1		
5	29	TEST	B	Test input pin This pin is connected directly to V_{SS}.
6	30	$\overline{RST}$	C	Reset I/O pin This pin consists of an N-ch open-drain output with a pull-up resistor and hysteresis input. A low level is output from this pin by internal source. The internal circuit is initialized at the input of a low level.
24, 25, 26, 27	12, 13, 23, 24	P00/$\overline{INT20}$, P01/$\overline{INT21}$, P02/$\overline{INT22}$, P03/$\overline{INT23}$	G	General-purpose I/O ports Also serve as external interrupt input pins. External interrupt input is hysteresis input type.
1 to 4	25 to 28	P04/$\overline{INT24}$ to P07/$\overline{INT27}$	D	General-purpose I/O ports Also serve as external interrupt input. External interrupt input is hysteresis input type.
17	5	P30	D	General-purpose I/O port Also serves as a serial I/O clock I/O. The serial I/O clock input is hysteresis input type with a built-in noise filter.
16	4	P31	E	General-purpose I/O port Also serves as a serial I/O data output pin.
15	3	P32	D	General-purpose I/O port Also serves as a serial I/O data input pin. The serial I/O data input is hysteresis input type with a built-in noise filter.
14	2	P33/EC	D	General-purpose I/O port Also serves as an external clock input pin for the 8-bit timer/counter. External clock input of the 8-bit timer/counter is hysteresis input type with a built-in noise filter.
13	1	P34/TO/INT10	D	General-purpose I/O port Also serves as the overflow output and external interrupt input for the 8-bit timer/counter. External interrupt input is hysteresis input type with a built-in noise filter.
12, 11	48, 34	P35/INT11, P36/INT12	D	General-purpose I/O port Also serve as external interrupt input pins. External interrupt input is hysteresis input type with a built-in noise filter.

(Continued)

*1: FPT-28P-M17
*2: DIP-28P-M03
*3: MQP-48C-P01

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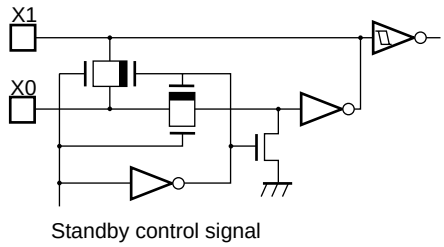
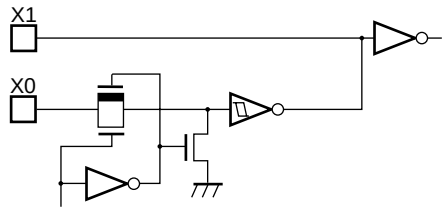
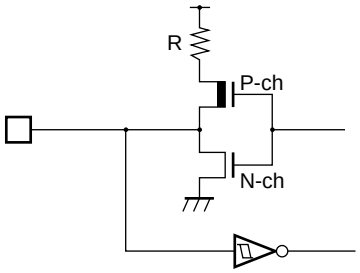
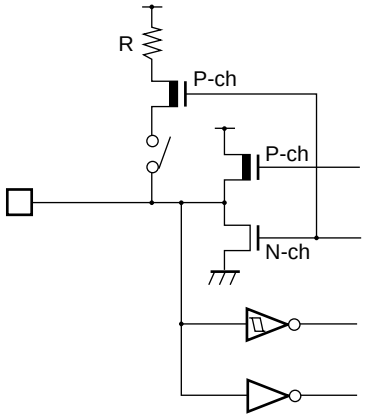
Pin no.		Pin name	Circuit type	Function
SOP*1, SH-DIP*2	MQFP*3			
10	33	P37//RCO	E	General-purpose I/O port Also serves as remote-control output pin.
18 to 21	6 to 9	P40 to P43	F	N-ch open-drain I/O ports
23	11	P45	F	N-ch open-drain type I/O port
22	10	P44	F	N-ch open-drain type I/O port
28	18	V_{CC}	—	Power supply pin
9	42	V_{SS}	—	Power supply (GND) pin

*1: FPT-28P-M17
*2: DIP-28P-M03
*3: MQP-48C-P01

- **External EPROM pins (MB89PV190 only)**

Pin no.	Pin name	I/O	Function
49	V_{PP}	O	“H” level output pin
79 78 50 75 71 76 77 51 52 53 54 55 58 59 60	A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
61 62 63 65 66 67 68 69	O1 O2 O3 O4 O5 O6 O7 O8	I	Data input pins
70	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
73	$\overline{OE}$	O	ROM output enable pin Outputs “L” at all times.
80	V_{CC}	O	EPROM power pin
64	V_{SS}	O	Power supply (GND) pin

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• At an oscillation feedback registor of approximately 1 MΩ at 5.0 V • When crystal and ceramic oscillators are selected optionally
		• When CR oscillation is selected optionally
B		
C		• Output pull-up resistor (P-ch): About 50 kΩ at 5.0 V • Hysteresis input • Pull-up resistor optional
D		• CMOS output • CMOS input • Hysteresis input (resource input) • Pull-up resistor optional

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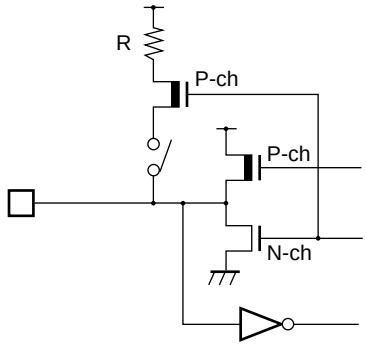
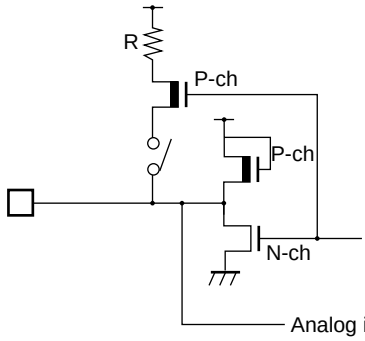
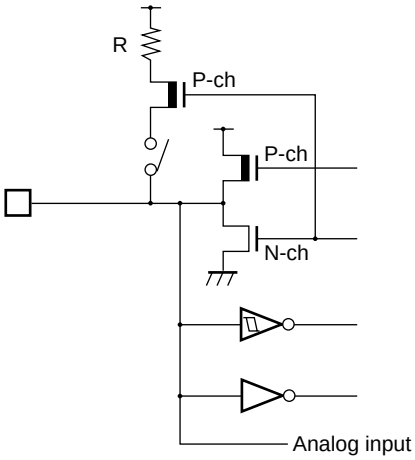
Type	Circuit	Remarks
E		• CMOS output • CMOS input • Pull-up resistor optional
F		• N-ch open-drain output • Analog input • Pull-up resistor optional (MB89990 series only)
G		• CMOS output • CMOS input • Hysteresis input (resource input) • Analog input • Pull-up resistor optional (MB89990 series only)

■ HANDLING DEVICES

1. Preventing Latch-up

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input or output pins other than medium-to high-voltage pins or if higher than the voltage which shows on " 1. Absolute Maximum Ratings" in "■ Electrical Characteristics" is applied between V_{CC} to V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to pull-up or pull-down resistor.

3. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

4. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

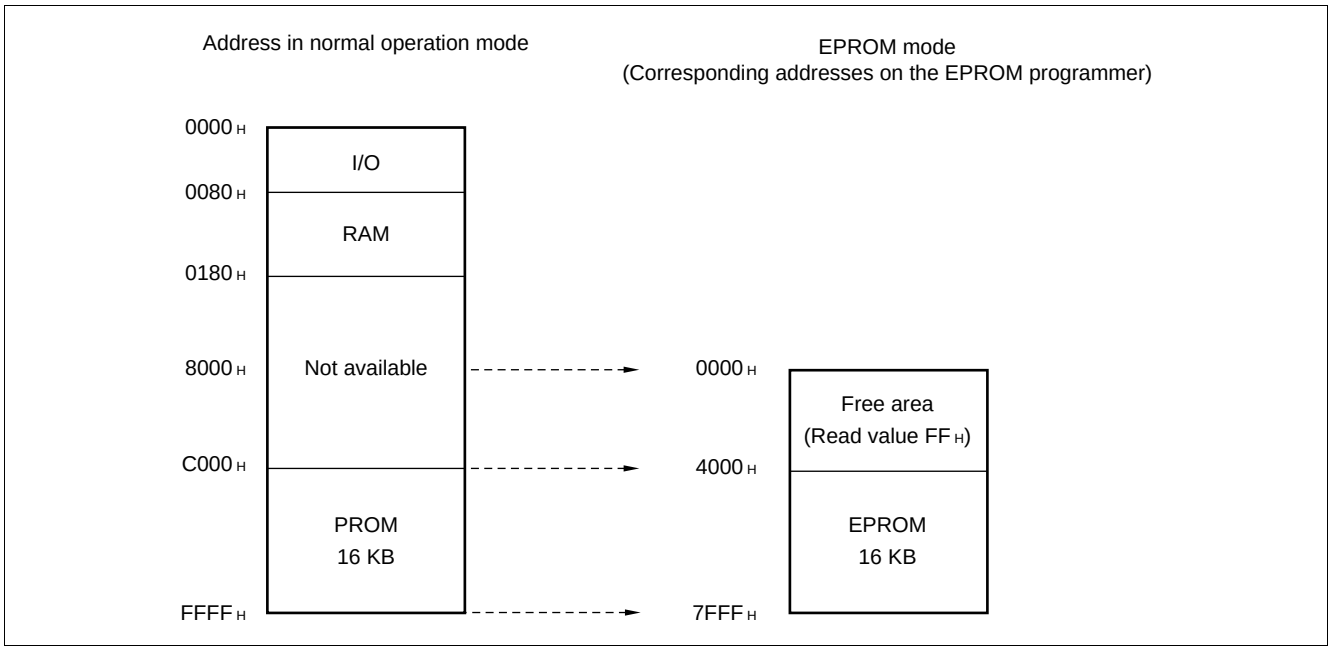
5. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (option selection) and release from stop mode.

■ PROGRAMMING TO PROM ON THE MB89P195

The MB89P195 can program data in the internal PROM using a dedicated conversion adaptor and specified general-purpose EPROM programmer.

1. Memory Space



2. Specified ROM Programmer Manufacturer, Model Name, and Programming in ROM

- **Recommended ROM programmer**

Manufacturer	Model
ADVANTEST	R4945

- **Programming procedure**

(1) Load program data into the ROM programmer at addresses 4000_H to $7FFF_H$. (Addresses $0C000_H$ to $0FFFF_H$ in the operation mode assign to 4000_H to $7FFF_H$ in ROM programmer. See the illustration above.)

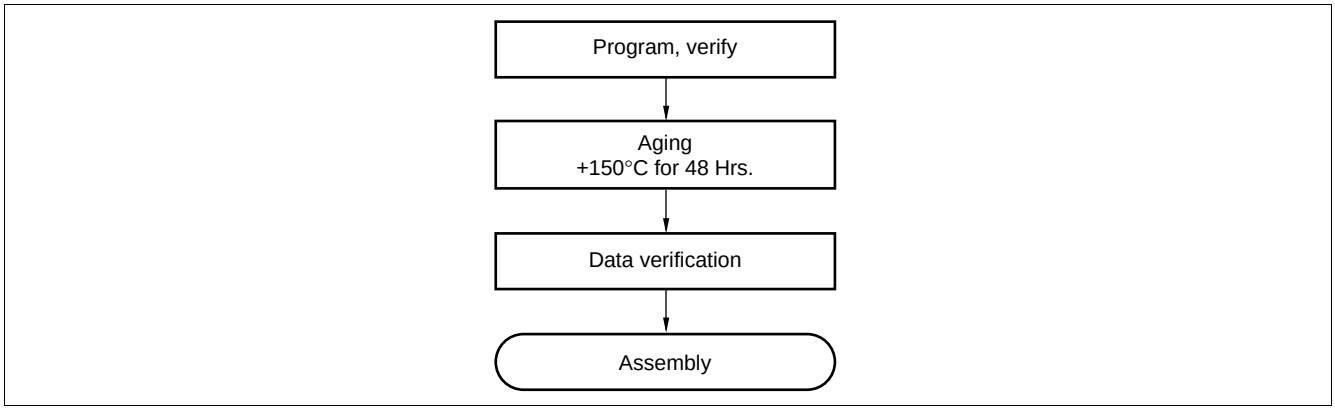
(2) Set the data at addresses 0000_H to $3FFF_H$ of the programmer ROM in the ROM programmer, to FF_H.

(3) To set up the successive-address write mode of the ROM programmer, press the DEVICE, PROG, SET, SELECT, E and SET keys in this order.

Note: Program must be started at the address 0000_H.
For details, contact our Sales Division.

3. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcontroller program.



4. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature (one time PROM). For this reason, a programming yield of 100% cannot be assured at all times.

5. EPROM Programmer Socket Adapter and Recommended Programmer Manufacturer

Part no.			MB89P195PF
Package			SOP-28
Compatible socket adapter Sun Hayato Co., Ltd.			ROM-28SOP-28DP-8L
Recommended programmer manufacturer and programmer name	**Minato Electronics Inc.**	**MODEL 1890A (ver. 2.2) + OU-910 (ver. 4.1)**	Recommended
	Data I/O Co., Ltd.	**UNISITE (ver. 5.0 or later)**	Recommended
		3900 (ver. 2.8 or later)	
		2900 (ver. 3.8 or later)	

Inquiry: Sun Hayato Co., Ltd. : TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106

Minato Electronics Inc. : TEL: USA (1)-916-348-6066
JAPAN (81)-45-591-5611

Data I/O Co., Ltd. : TEL: USA/ASIA (1)-206-881-6444
EUROPE (49)-8-985-8580

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TVM

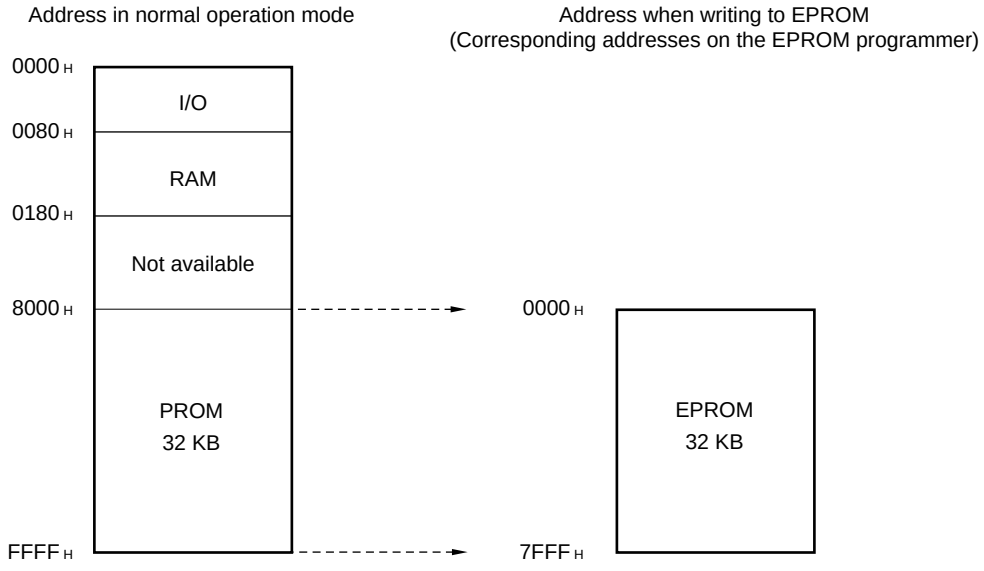
2. Programming Socket Adapter

To program to the EPROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106

3. Memory Space



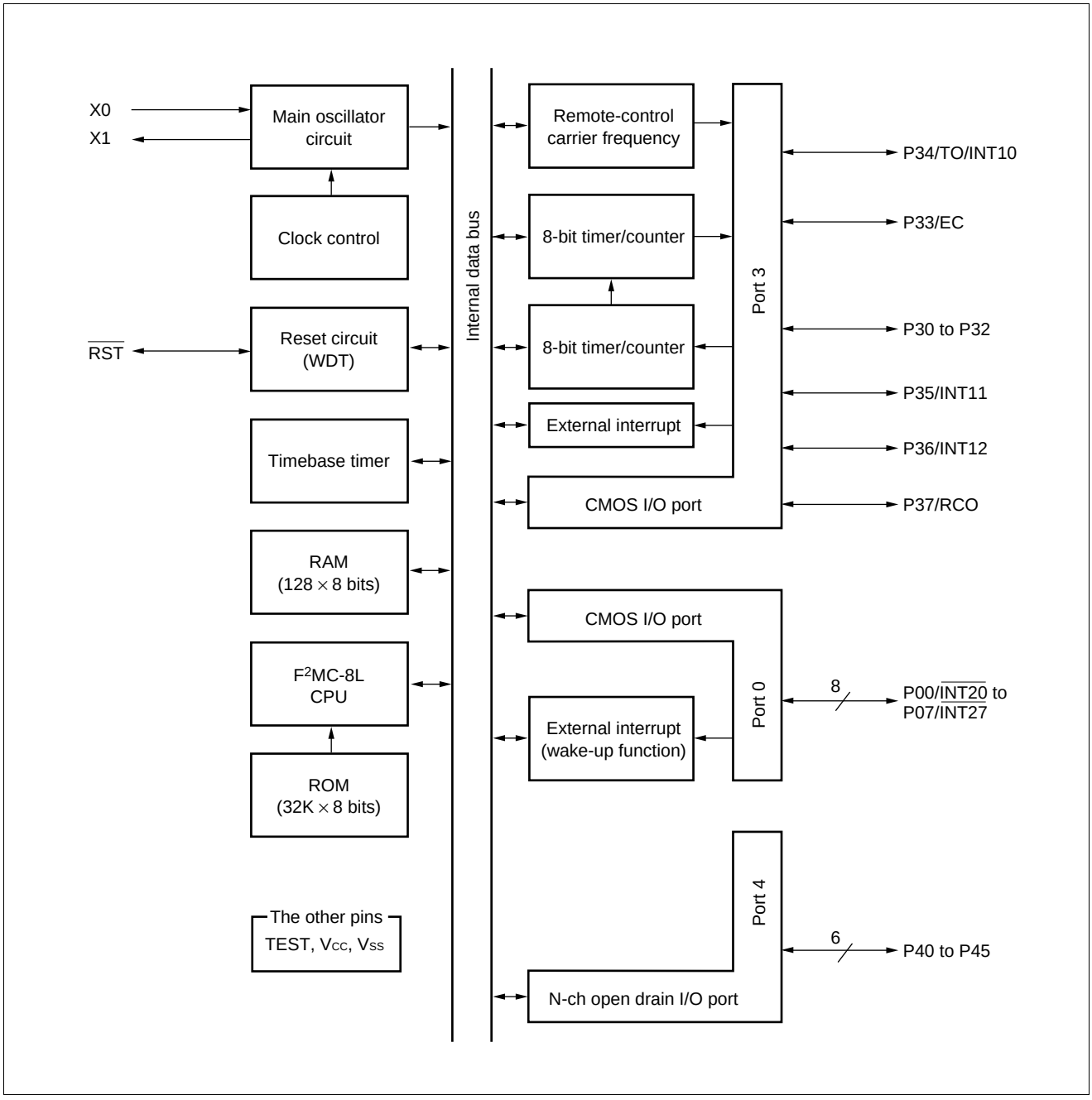
4. Programming to the EPROM

(1) Set the EPROM programmer to MBM27C256A.

(2) Load program data into the EPROM programmer at 0006_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

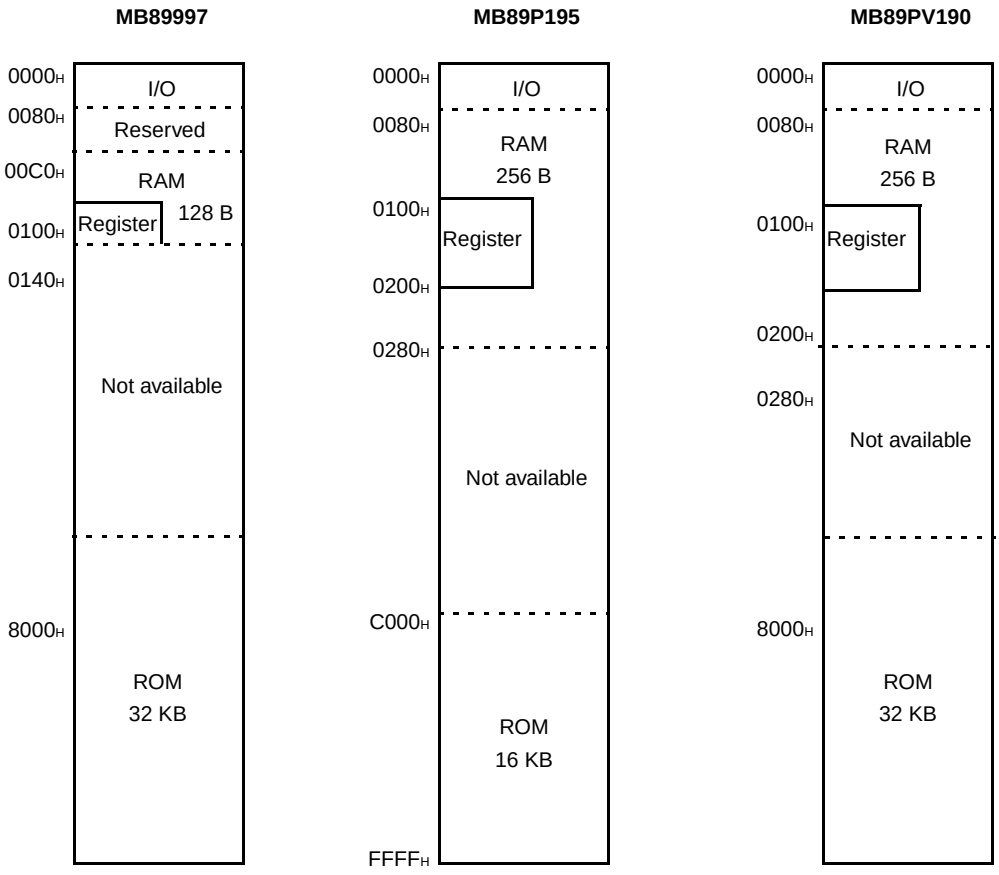


■ CPU CORE

1. Memory Space

The microcontrollers of MB89990 series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provide immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end of I/O area, that is, near the highest address. Provide the tables of interrupt reset vectors, and vector call instructions toward the highest address within the program area. The memory space of the MB89990 series is structured below:

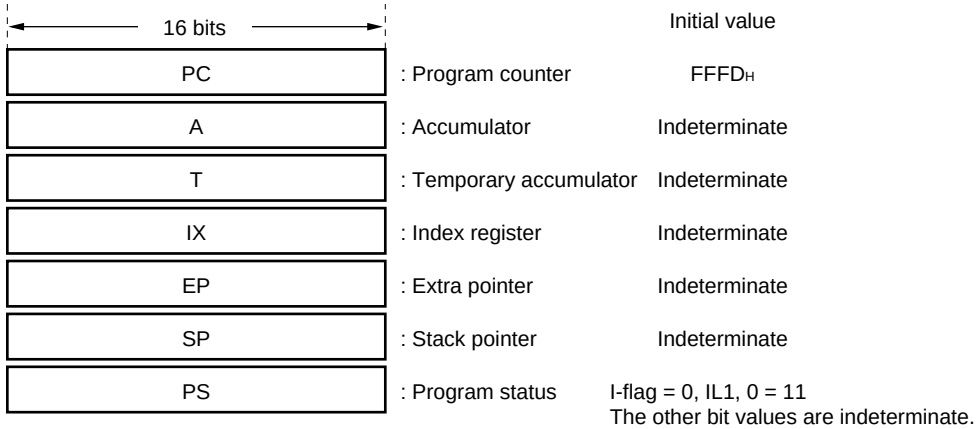
• **Memory Space**



2. Registers

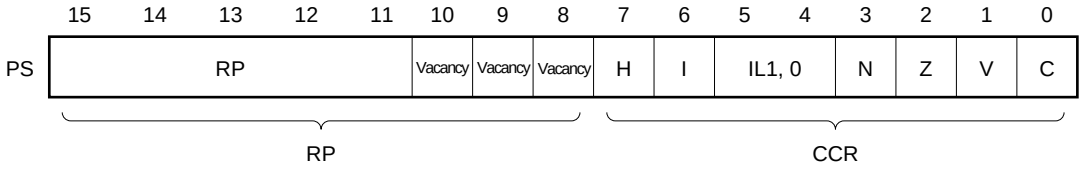
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit-long register for indicating the instruction storage positions
Accumulator (A):	A 16-bit-long temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit-long register which performs arithmetic operations with the accumulator. When the instruction is an 18-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit-long register for index modification
Extra pointer (EP) :	A 16-bit-long pointer for indicating a memory address
Stack pointer (SP) :	A 16-bit-long register for indicating a stack area
Program status (PS) :	A 16-bit-long register for storing a register pointer, a condition code



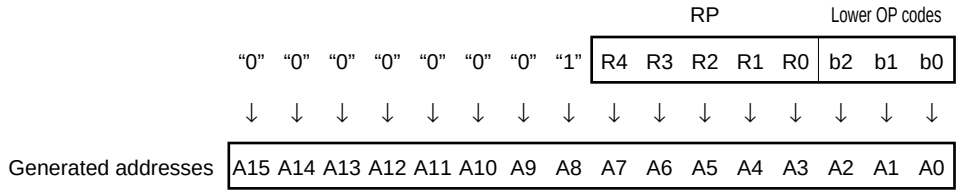
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR) (see the diagram below).

• **Structure of the Program Status Register**



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

- **Rule for Conversion of Actual Addresses of the General-purpose Register Area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the rest.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes 1 as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise.
Set the shift-out value in the case of a shift instruction.

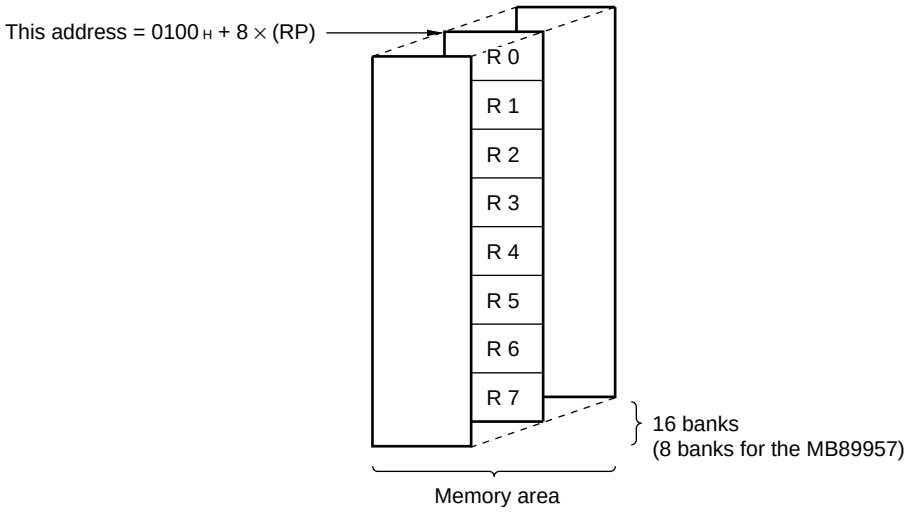
The following general-purpose registers are provided:

General-purpose registers: An 8-bit-long register for storing data

The general-purpose registers are 8 bits and located in register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89957 (RAM 128 × 8 bits). The bank currently in use is indicated by the register bank pointer. (RP)

Note: The number of register banks that can be used varies with the RAM size.

- **Register Bank Configuraiton**



■ I/O MAP

Address	Read/write	Register name	Register description
00_H	(R/W)	PDR0	Port 0 data register
01_H	(W)	DDR0	Port 0 data direction register
02_H to 07_H			Vacancy
08_H	(R/W)	STBC	Standby control register
09_H	(R/W)	WDTC	Watchdog timer control register
$0A_H$	(R/W)	TBTC	Timebase timer control register
$0B_H$			Vacancy
$0C_H$	(R/W)	PDR3	Port 3 data register
$0D_H$	(W)	DDR3	Port 3 data direction register
$0E_H$	(R/W)	PDR4	Port 4 data register
$0F_H$ to 13_H			Vacancy
14_H	(R/W)	RCR1	Remote-control register 1
15_H	(R/W)	RCR2	Remote-control register 2
16_H			Vacancy
17_H			Vacancy
18_H	(R/W)	T2CR	Timer 2 control register
19_H	(R/W)	T1CR	Timer 1 control register
$1A_H$	(R/W)	T2DR	Timer 2 data register
$1B_H$	(R/W)	T1DR	Timer 1 data register
$1C_H$ to 22_H			Vacancy
23_H	(R/W)	EIC1	External interrupt control register 1
24_H	(R/W)	EIC2	External interrupt control register 2
25_H to 31_H			Vacancy
32_H	(R/W)	EIE2	External interrupt 2 enable register
33_H	(R/W)	EIF2	External interrupt 2 flag register
34_H to $7B_H$			Vacancy
$7C_H$	(W)	ILR1	Interrupt level register 1
$7D_H$	(W)	ILR2	Interrupt level register 2
$7E_H$	(W)	ILR3	Interrupt level register 3
$7F_H$			Vacancy

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
EPROM program voltage	V_{PP}	V_{SS} – 0.3	V_{SS} + 13.0	V	Applicable to TEST pin of MB89P195.
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 0.3	V	
“L” level maximum output current	I_{OL1}	—	10	mA	Except P33 and P34
	I_{OL2}	—	20	mA	P33, P34
“L” level average output current	I_{OLAV1}	—	4	mA	Except P33 and P34 Average value (operating current × operation rate)
	I_{OLAV2}	—	8	mA	P33 and P34 Average value (operating current × operation rate)
“L” level total average output current	ΣI_{OLAV}	—	20	mA	Average value (operating current × operation rate)
“L” level maximum total output current	ΣI_{OL}	—	–100	mA	
“H” level maximum output current	I_{OH1}	—	–10	mA	Except P33, P34, and P37
	I_{OH2}	—	–20	mA	P33, P34, P37
“H” level average output current	I_{OHAV1}	—	–2	mA	Except P33, P34, and P37 Average value (operating current × operation rate)
	I_{OHAV2}	—	–4	mA	Except P33, P34, and P37 Average value (operating current × operation rate)
“H” level total average output current	ΣI_{OHAV}	—	–10	mA	Average value (operating current × operation rate)
“H” level total maximum output current	ΣI_{OH}	—	–30	mA	
Power consumption	P_D	—	200	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

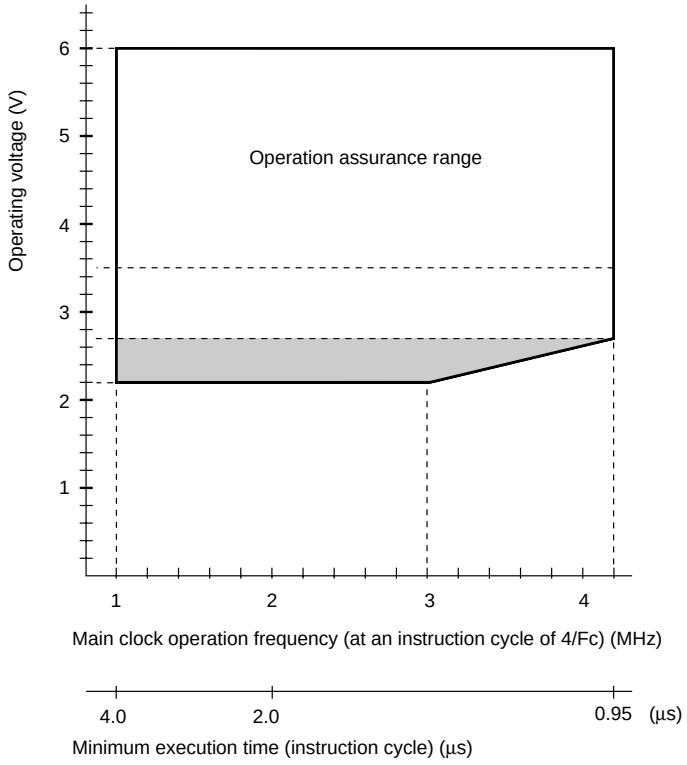
2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.2*	6.0*	V	Normal operation assurance range* MB89997
		2.7*	6.0*	V	Normal operation assurance range* MB89P195
		1.5	6.0	V	Retains the RAM state in stop mode
Operating temperature	T_A	–40	+85	°C	

* : The guaranteed normal operation range varies depending on the operation frequency and the guaranteed analog operation range. See Figure 1.

- **Figure 1 Operating Voltage vs. Main Clock Operating Frequency**



Note: The shaded area is assured only for the MB89997.

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/F_C.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

(V_{CC} = +5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P30 to P37, TEST	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, INT10 to INT12, EC, $\overline{INT20}$ to $\overline{INT27}$	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P03, P33 to P36, TEST	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, INT10 to INT12, EC, $\overline{INT 20}$ to $\overline{INT27}$	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P40 to P44	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
"H" level output voltage	V_{OH1}	P00 to P07, P30 to P32, P35, P36	I_{OH} = –2.0 mA	4.0	—	—	V	
	V_{OH2}	P33, P34	I_{OH} = –4.0 mA	4.0	—	—	V	
	V_{OH3}	P37	I_{OH} = –4.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P30 to P32, P35 to P37	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL3}	P33, P34	I_{OL} = 12 mA	—	—	0.4	V	
	V_{OL4}	P40 to P45	I_{OL} = 8 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	P00 to P07, P30 to P37, TEST	0.45 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Open-drain output leakage current (Off state)	I_{LD1}	P40 to P45	0.45 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P30 to P37, P40 to P45, RST	V_I = 0.0 V	25	50	100	kΩ	

(Continued)

(Continued)

(V_{CC} = 5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply voltage*	I_{CC}	V_{CC}	F_C = 4.2 MHz	—	5	10	mA	MB89997
				—	7	12	mA	MB89P195
	I_{CCS}		F_C = 4.2 MHz	—	3	7	mA	Sleep mode
	I_{CCH}		T_A = +25 °C	—	—	1	µA	Stop mode
Input capacitance	C_{IN}	Except AVR, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

* : For the MB89PV190, the current consumption of a connected EPROM and ICE is not included.
The mesurement condition of the power supply current are set as V_{CC} = 5.0 V with an external clock.

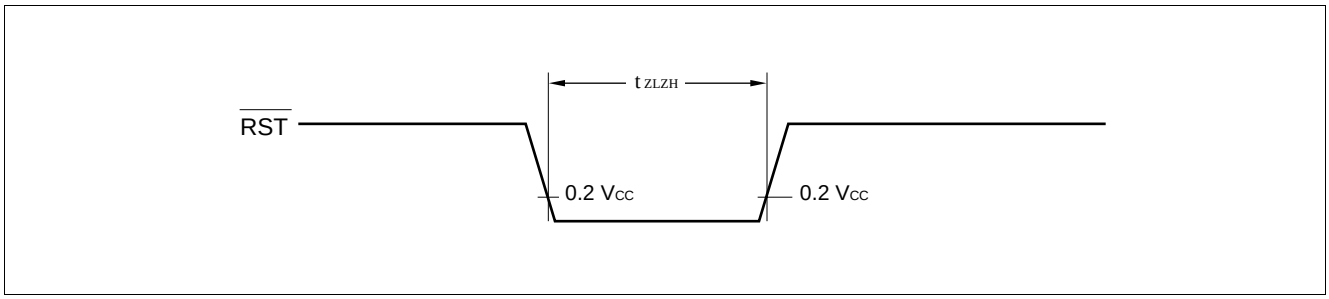
4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ “L” pulse width	t_{ZLZH}	—	16 t_{HCYL}	—	ns	

Note: t_{XCYL} is the oscillation period (1/F_C) input to the X0 pin.

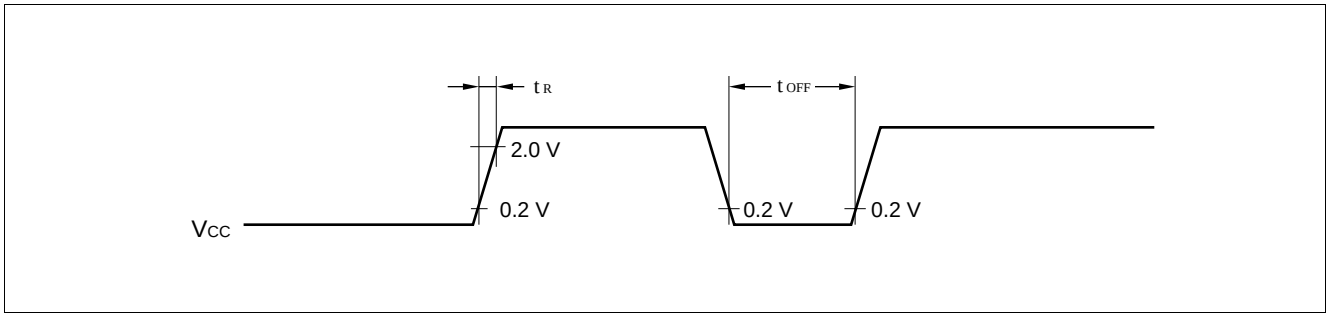


(2) Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

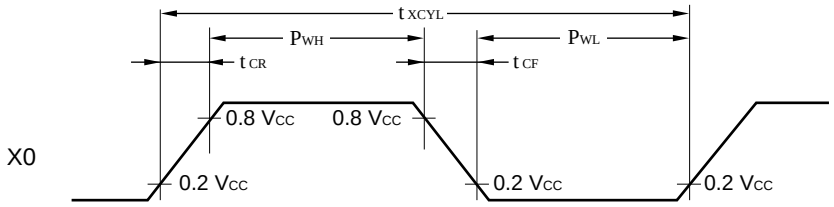


(3) Clock Timing

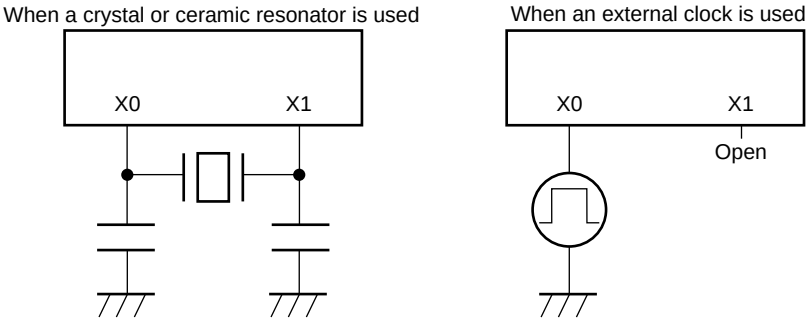
(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	F_C	X0, X1	—	1	4.2	MHz	
Clock cycle time	t_{XCYL}	X0, X1	—	238	1000	ns	
Input clock pulse width	P_{WH} P_{WL}	X0	—	20	—	ns	External clock
Input clock pulse risilng/falling time	t_{CR} t_{CF}	X0	—	—	10	ns	External clock

- **Timings Conditions**



- **Clock Configurations**



(4) Instruction Cycle

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_C$	µs	t_{inst} = 0.95 µs when operating at F_C = 4.2 MHz

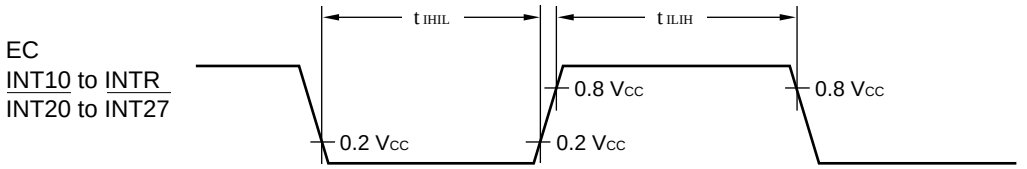
(5) Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	EC, INT10 to INT12, INT20 to INT27	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycles.”

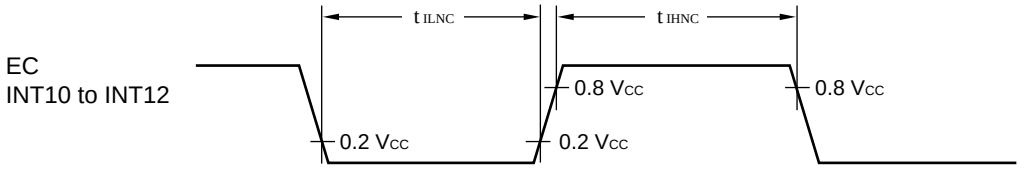
• **Peripheral Input Timing Diagram**



(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

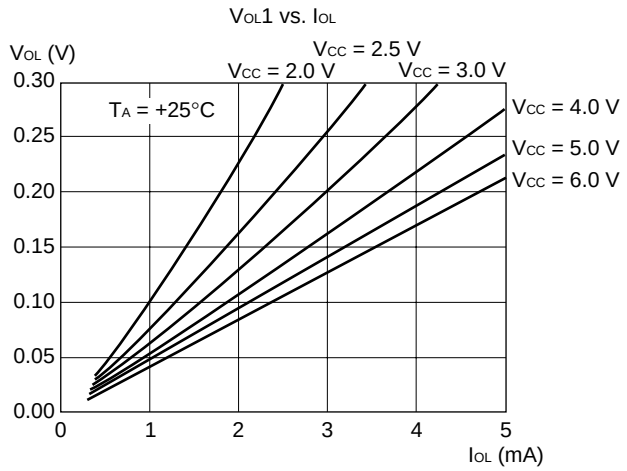
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Peripheral input “H” noise limit width	t_{IHNC}	EC, INT10 to INT12	7	15	23	ns	
Peripheral input “L” noise limit width	t_{ILNC}	EC, INT10 to INT12, INT20 to INT27	7	15	23	ns	

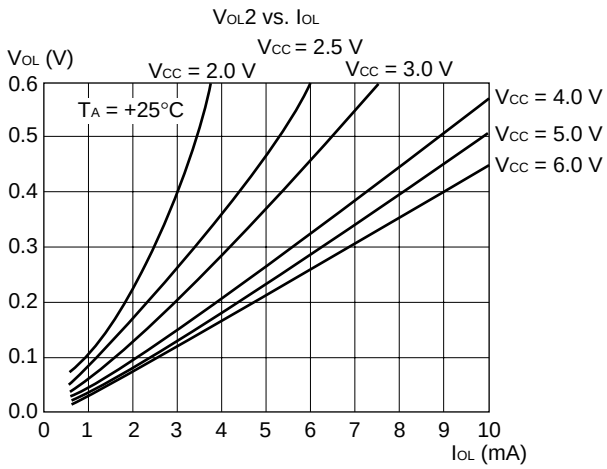
• **Peripheral Input Timing Diagram**

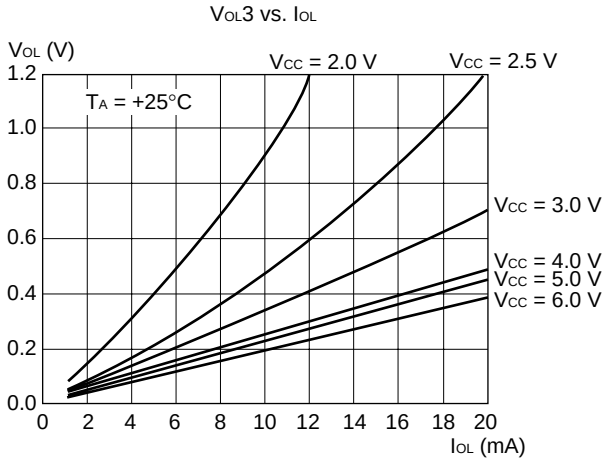


■ EXAMPLE CHARACTERISTICS

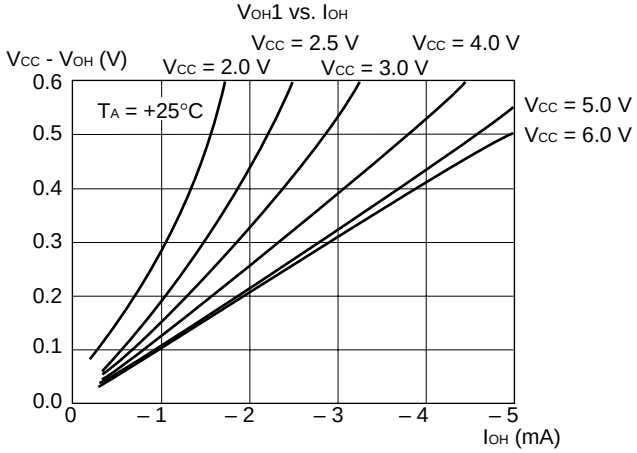
(1) “L” Level Output Voltage

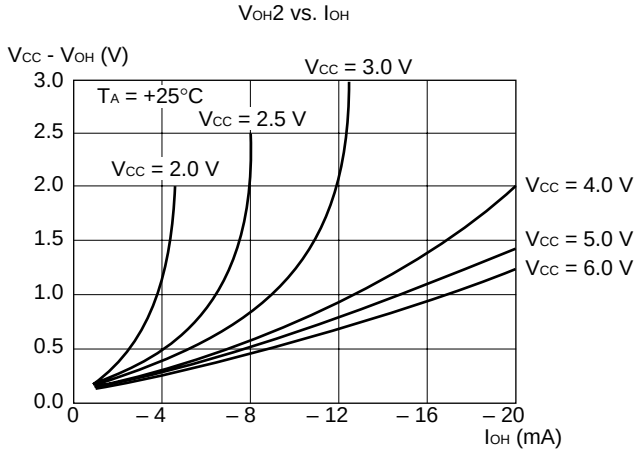


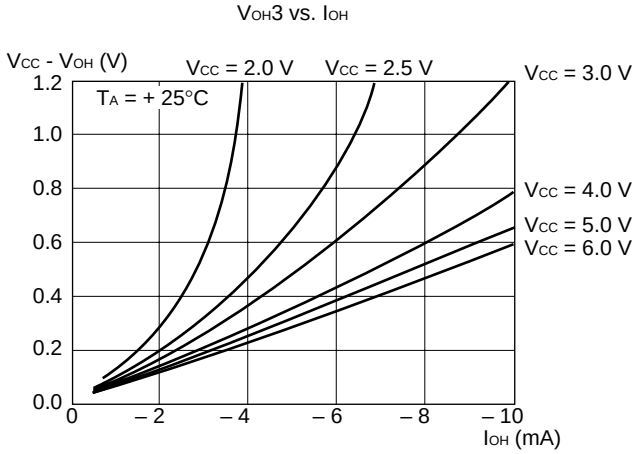




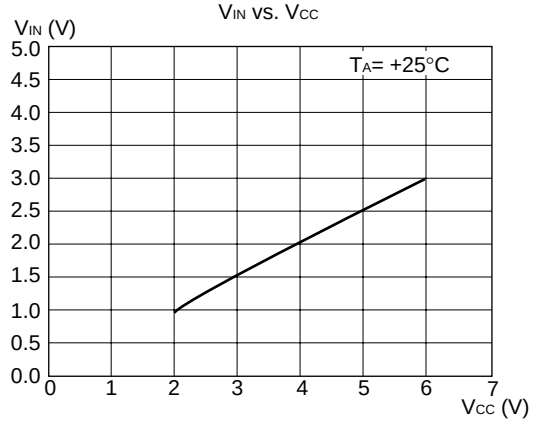
(2) “H” Level Output Voltage



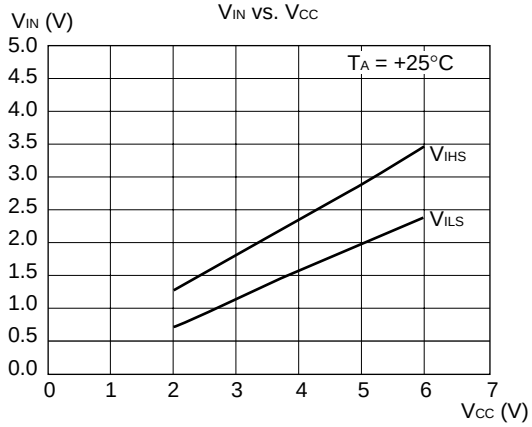




(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)



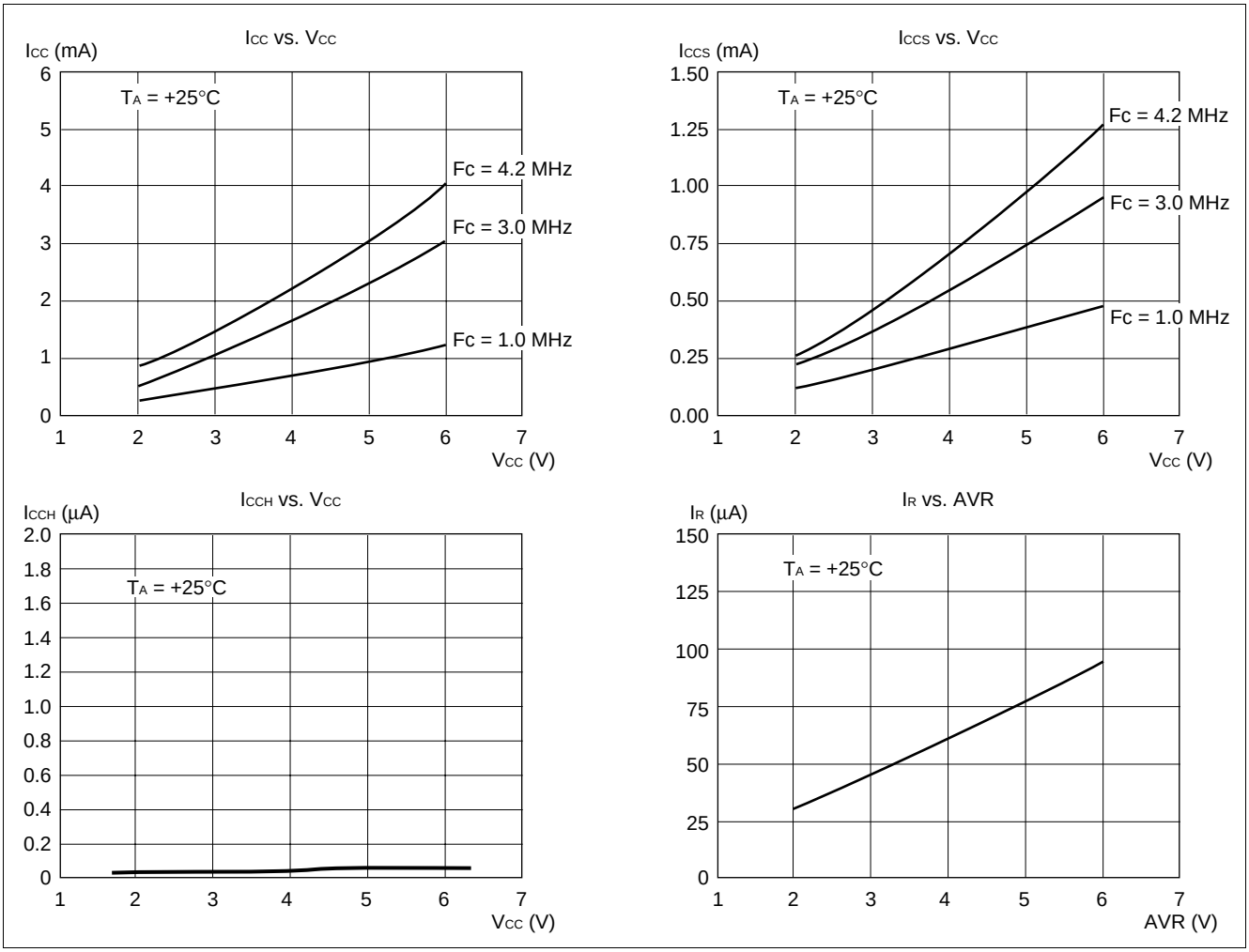
(4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)



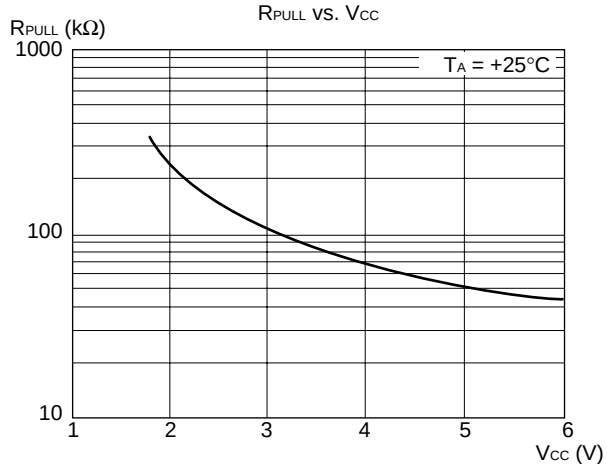
VIHS: Threshold when input voltage in hysteresis characteristics is set to “H” level

VILS: Threshold when input voltage in hysteresis characteristics is set to “L” level

(5) Power Supply Current (External Clock)



(3) Pull-up Resistance



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation for instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: The number of instructions

#: The number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- “-” indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH prior to the instruction executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

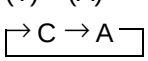
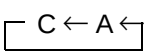
Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes:
- During byte transfer to A, T ← A is restricted to low bytes.
- Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 toDF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1		–	–	–	+ + – +	03
ROLC A	2	1		–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) –d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) +off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N= 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N= 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b)= 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b)= 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A@,IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTION LIST

No.	Part number		MB89997	MB89P195			MB89PV190
	Specifying procedure		Specify when ordering masking	–101*2	Specify when ordering masking	–201*2	Fixed
1	Port pull-up resistors	P00 to P07 P30 to P37 P40 to P45	Selectable by pin	None	Selectable by pin	None	Not available
2	Power-on reset selection Power-on reset provided No power-on reset		Selectable	Enabled	Enabled	Enabled	Enabled
3	Selection of oscillation stabilization wait time (at 4.2 MHz)*1 $2^{18}/F_C$ (Approx. 62.4 ms) $2^{16}/F_C$ (Approx. 15.6 ms) $2^{12}/F_C$ (Approx. 0.98 ms) $2^2/F_C$ (Approx. 0 ms)		Selectable	Fixed to $2^{16}/F_C$	Selectable	Fixed to $2^{16}/F_C$	Fixed to $2^{16}/F_C$
4	Reset pin output Reset output provided No reset output		Selectable	Enabled	Selectable	Enabled	Output enabled
5	Oscillation type of clock 1 Crystal and ceramic oscillators 2 CR		Selectable	"1" only	Selectable	"1" only	"1" only

*1: The oscillation stabilization delay time is generated by dividing the original clock oscillation. The time described in this item should be used as a guideline since the oscillation cycle is unstable immediately after oscillation starts. "F_C" indicates the original oscillation frequency.

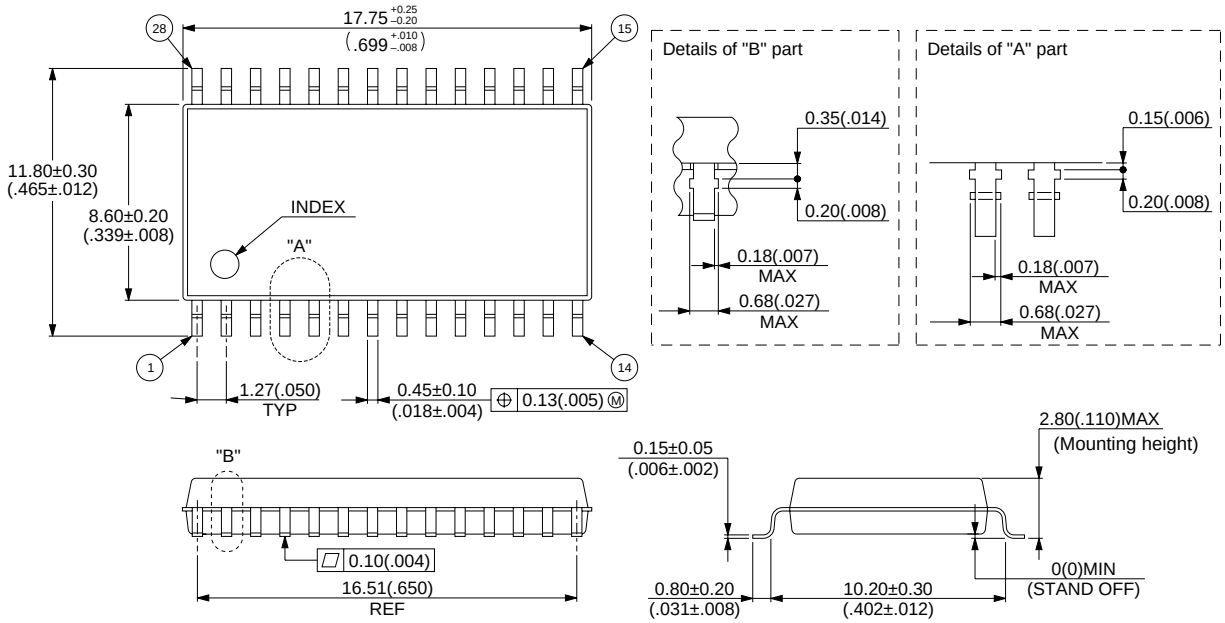
*2: –101 is provided respectively for the MB89P195 OTP versions as the standard product.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89997PF MB89P195PF-101	28-pin Plastic SOP (FPT-28P-M17)	
MB89997P-SH	28-pin Plastic SH-DIP (DIP-28C-M03)	
MB89PV190CF	48-pin Ceramic MQFP (MQP-48C-P01)	

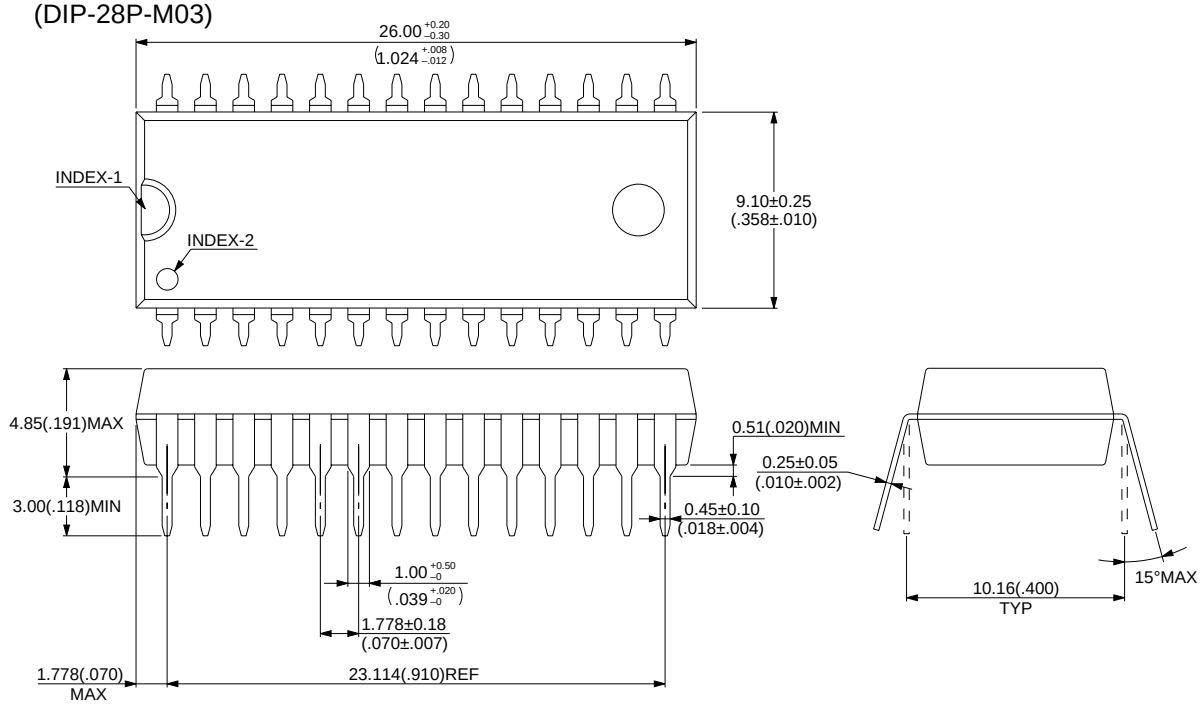
■ PACKAGE DIMENSIONS

28-pin Plastic SOP
(FPT-28P-M17)



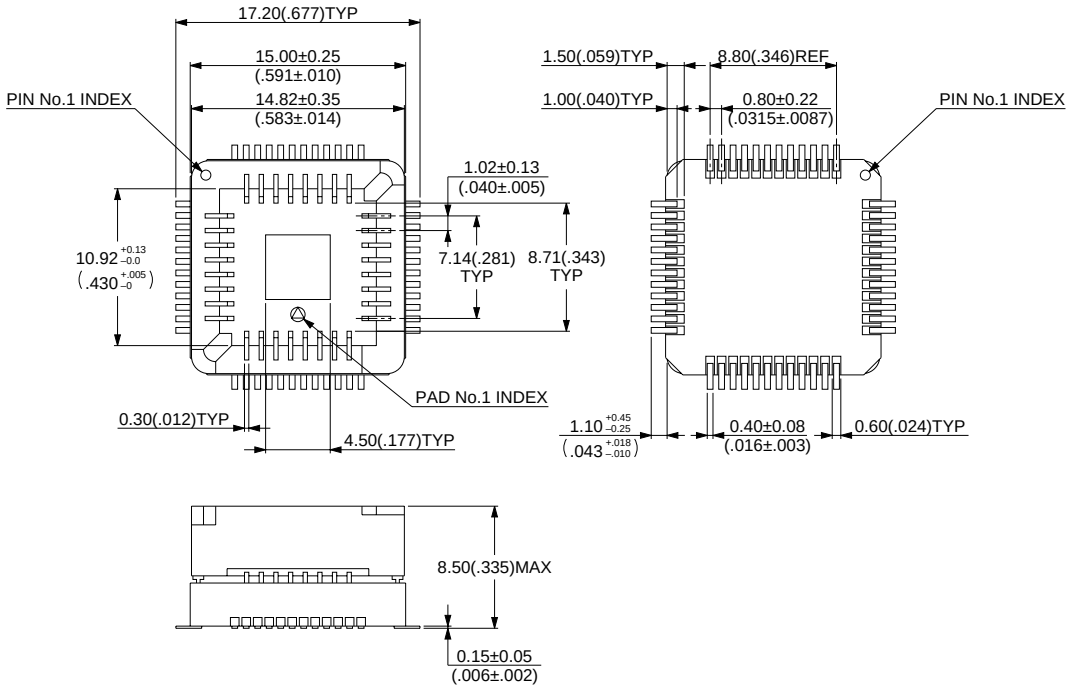
Dimensions in mm (inches)

28-pin Plastic SH-DIP
(DIP-28P-M03)



Dimensions in mm (inches)

48-pin Ceramic MQFP
(MQP-48C-P01)



Dimensions in mm (inches)

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